Contact us

128-/128-/64-/32-Mbit (8/8/4/2M × 16-Bit), 3 V, Flash with Enhanced VersatileIO™

Distinctive Characteristics

Architectural Advantages

- 128-/128-/64-/32-Mbit Page Mode devices
  - Page size of 8 words: Fast page read access from random locations within the page
- Single power supply operation
  - Full Voltage range: 2.7 to 3.6 V read, erase, and program operations for battery-powered applications
- Dual Chip Enable inputs (only in PL129J)
  - Two CE# inputs control selection of each half of the memory space
- Simultaneous Read/Write Operation
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency switching from write to read operations
- FlexBank Architecture (PL127J/PL064J/PL032J)
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A:
    PL127J -16 Mbit (4 Kw × 8 and 32 Kw × 31)
    PL064J - 8 Mbit (4 Kw × 8 and 32 Kw × 15)
    PL032J - 4 Mbit (4 Kw × 8 and 32 Kw × 7)
  - Bank B:
    PL127J - 48 Mbit (32 Kw × 96)
    PL064J - 24 Mbit (32 Kw × 48)
    PL032J - 12 Mbit (32 Kw × 24)
  - Bank C:
    PL127J - 48 Mbit (32 Kw × 96)
    PL064J - 24 Mbit (32 Kw × 48)
    PL032J - 12 Mbit (32 Kw × 24)
  - Bank D:
    PL127J -16 Mbit (4 Kw × 8 and 32 Kw × 31)
    PL064J - 8 Mbit (4 Kw × 8 and 32 Kw × 15)
    PL032J - 4 Mbit (4 Kw × 8 and 32 Kw × 7)
- FlexBank Architecture (PL129J)
  - 4 separate banks, with up to two simultaneous operations per device
  - CE#1 controlled banks:
    Bank 1A: PL129J - 16-Mbit (4Kw × 8 and 32Kw × 31)
    Bank 1B: PL129J - 48-Mbit (32Kw × 96)
  - CE#2 controlled banks:
    Bank 2A: PL129J - 48-Mbit (32 Kw × 96)
    Bank 2B: PL129J - 16-Mbit (4 Kw × 8 and 32 Kw × 31)
- Enhanced VersatileI/O (V$_{IO}$) Control

- Output voltage generated and input voltages tolerated on all control inputs and I/Os is determined by the voltage on the V$_{IO}$ pin
  - V$_{IO}$ options at 1.8 V and 3 V I/O for PL127J and PL129J devices
  - 3V V$_{IO}$ for PL064J and PL032J devices
- Secured Silicon Sector region
  - Up to 128 words accessible through a command sequence
  - Up to 64 factory-locked words
  - Up to 64 customer-lockable words
- Both top and bottom boot blocks in one device
- Manufactured on 110-nm process technology
- Data Retention: 20 years typical
- Cycling Endurance: 1 million cycles per sector typical

Performance Characteristics

- High Performance
  - Page access times as fast as 20 ns
  - Random access times as fast as 55 ns
- Power consumption (typical values at 10 MHz)
  - 45 mA active read current
  - 17 mA program/erase current
  - 0.2 µA typical standby mode current

Software Features

- Software command-set compatible with JEDEC 42.4 standard
  - Backward compatible with Am29F, Am29LV, Am29DL, and AM29PDL families and MBM29QM/RM, MBM29LV, MBM29DL, MBM29PDL families
- CFI (Common Flash Interface) compliant
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend / Erase Resume
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- Program Suspend / Program Resume
  - Suspends a program operation to allow read operation from sectors other than the one being programmed
- Unlock Bypass Program command
- Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/Busy# pin (RY/BY#)
  - Provides a hardware method of detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method to reset the device to reading array data
- WP#/ ACC (Write Protect/Acceleration) input
  - At V_{IL}, hardware level protection for the first and last two 4K word sectors.
  - At V_{IH}, allows removal of sector protection
  - At V_{HH}, provides accelerated programming in a factory setting
- Persistent Sector Protection
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at V_{CC} level

- Password Sector Protection
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-defined 64-bit password
- Package options
  - Standard discrete pinouts
    11 × 8 mm, 80-ball Fine-pitch BGA (PL127J) (VBG080)
    8.15 × 6.15 mm, 48-ball Fine pitch BGA (PL064J/PL032J) (VBK048)
  - MCP-compatible pinout
    8 × 11.6 mm, 64-ball Fine-pitch BGA (PL127J)
    7 × 9 mm, 56-ball Fine-pitch BGA (PL064J and PL032J)
    Compatible with MCP pinout, allowing easy integration of RAM into existing designs
  - 20 × 14 mm, 56-pin TSOP (PL127J) (TS056)

Contents

1. General Description

The PL127J/PL129J/PL064J/PL032J is a 128/128/64/32 Mbit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 8/8/4/2 Mwords. The devices are offered in the following packages:

- 11 mm × 8 mm, 80-ball Fine-pitch BGA standalone (PL127J)

- 8 mm × 11.6 mm, 64-ball Fine-pitch BGA multi-chip compatible (PL127J)

- 8.15 mm × 6.15 mm, 48-ball Fine-pitch BGA standalone (PL064J/PL032J)

- 7 mm × 9 mm, 56-ball Fine-pitch BGA multi-chip compatible (PL064J and PL032J)

- 20 mm × 14 mm, 56-pin TSOP (PL127J)

The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. A 12.0 V V_{PP} is not required for write or erase operations.

2. Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.

The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

Bank	PL127J Sectors	PL064J Sectors	PL032J Sectors
A	16 Mbit (4 Kw × 8 and 32 Kw × 31)	8 Mbit (4 Kw × 8 and 32 Kw × 15)	4 Mbit (4 Kw × 8 and 32 Kw × 7)
B	48 Mbit (32 Kw × 96)	24 Mbit (32 Kw × 48)	12 Mbit (32 Kw × 24)
C	48 Mbit (32 Kw × 96)	24 Mbit (32 Kw × 48)	12 Mbit (32 Kw × 24)
D	16 Mbit (4 Kw x 8 and 32 Kw × 31)	8 Mbit (4 Kw × 8 and 32 Kw × 15)	4 Mbit (4 Kw × 8 and 32 Kw × 7)

Bank	PL129J Sectors	CE# Control
1A	16 Mbit (4 Kw × 8 and 32 Kw × 31)	CE1#
1B	48 Mbit (32 Kw × 96)	CE1#
2A	48 Mbit (32 Kw × 96)	CE2#
2B	16 Mbit (4 Kw × 8 and 32 Kw × 31)	CE2#

2.1 Page Mode Features

The page size is 8 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

2.2 Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **Program Suspend/Program Resume** feature enables the user to hold the program operation to read data from any sector that is not selected for programming. If a read is needed from the Secured Silicon Sector area, Persistent Protection area, Dynamic Protection area, or the CFI area, after a program suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

3.   Ordering Information

The order number (Valid Combination) is formed by a valid combinations of the following:

S29PL-J   XX   XX   X   XX   X

Packing Type: X = 0 or 1 or 2 or 3
0 = Tray
1 = Tube
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

Model Number (Additional Ordering Options): XX = 00 or 01 or 02 or 12 or 13 or 14 or 15
00 = 3.0V V_{IO}, 80-ball 11 x 8 mm FBGA (VBG080)
01 = 1.8V V_{IO}, 80-ball 11 x 8 mm FBGA (VBG080)
02 = 3.0V V_{IO}, 64-ball 8 x 11.6 mm FBGA (VBH064)
12 = 3.0V V_{IO}, 48-ball 8 x 6 mm FBGA (VBK048)
13 = 3.0V V_{IO}, 56-pin 20 x 14 mm TSOP (TS056)
14 = 1.8V V_{IO}, 56-pin 20 x 14 mm TSOP (TS056)
15 = 3.0V V_{IO}, 56-ball 7 x 9 mm FBGA (VBU056)

Temperature Range: X = W or I
W = Wireless (–25°C to +85°C)
I = Industrial (–40°C to +85°C)

Package Type: XX = BF or TF
BF = Fine-Pitch Grid Array (FBGA)
     Lead (Pb)-free
TF = Thin Small Outline Package (TSOP) Standard Pinout
     Lead (Pb)-free

Clock Speed: XX = 55 or 60 or 65 or 70 or 80
55 = 55 ns (Contact factory for availability)
60 = 60 ns
65 = 65 ns
70 = 70 ns
80 = 80 ns

Device Number/Description
128 Mbit (8M x 16-Bit), 64 Megabit (4M x 16-Bit), 32 Megabit (2M x 16-Bit)
CMOS Flash Memory, Simultaneous-Read/Write, Page-Mode Flash Memory,
3.0 V-only Read, Program, and Erase

Valid Combinations to be Supported for this Device

128 Mb Products Based on 110 nm Floating Gate Technology					
Device Number/ Description	Speed (ns)	Package Type	Temperature Range	Additional Ordering Options	CE# Configuration
S29PL127J	60, 65, 70	BF, TF	W, I	00, 13	Single CE#
S29PL127J	80	BF	W, I	01	Single CE#
S29PL127J	80	TF	W, I	14	Single CE#

64 Mb Products Based on 110 nm Floating Gate Technology				
Device Number/ Description	Speed (ns)	Package Type	Temperature Range	Additional Ordering Options
S29PL064J	55, 60, 70	BF	W, I	12, 15

32 Mb Products Based on 110 nm Floating Gate Technology				
Device Number/ Description	Speed (ns)	Package Type	Temperature Range	Additional Ordering Options
S29PL032J	55, 60, 70	BF	W, I	12, 15

Valid Combinations for BGA Packages		
Order Number (Note 1)	Speed (ns)	V_{IO} Range
PL129J, PL127J,PL064J, PL032J	55, 60, 65, 70 (3)	2.7–3.6
PL129J, PL127J	80	1.65–1.95

Notes

1. Please contact the factory for PL129J availability.

2. BGA package marking omits leading S29 and packing type designator from ordering part number.

3. 55 ns speed only supported for PL032J and PL127J.

Valid Combinations for TSOP Packages		
Order Number	Speed (ns)	V_{IO} Range
S29PL127J	60, 70	2.7–3.6

Note
TSOP package markings omit packing type designator from ordering part number.

4. Product Selector Guide

Part Number →		S29PL032J/S29PL064J/S29PL0127J/S29PL129J				
Speed Option	V_{CC}, V_{IO} = 2.7 V – 3.6 V	55 (See Note)	60	65	—	70
	V_{CC} = 2.7 V – 3.6 V, V_{IO} = 1.65 V – 1.95 V (PL127J and PL129J only)	—	—	—	80	—
Max Access Time, ns (t_{ACC})		55 (See Note)	60	65	80	70
Max CE# Access, ns (t_{CE})						
Max Page Access, ns (t_{PACC})		20 (See Note)	25		30	30
Max OE# Access, ns (t_{OE})						

Note
55 ns speed bin only supported for PL032J and PL064J.

5. Block Diagram
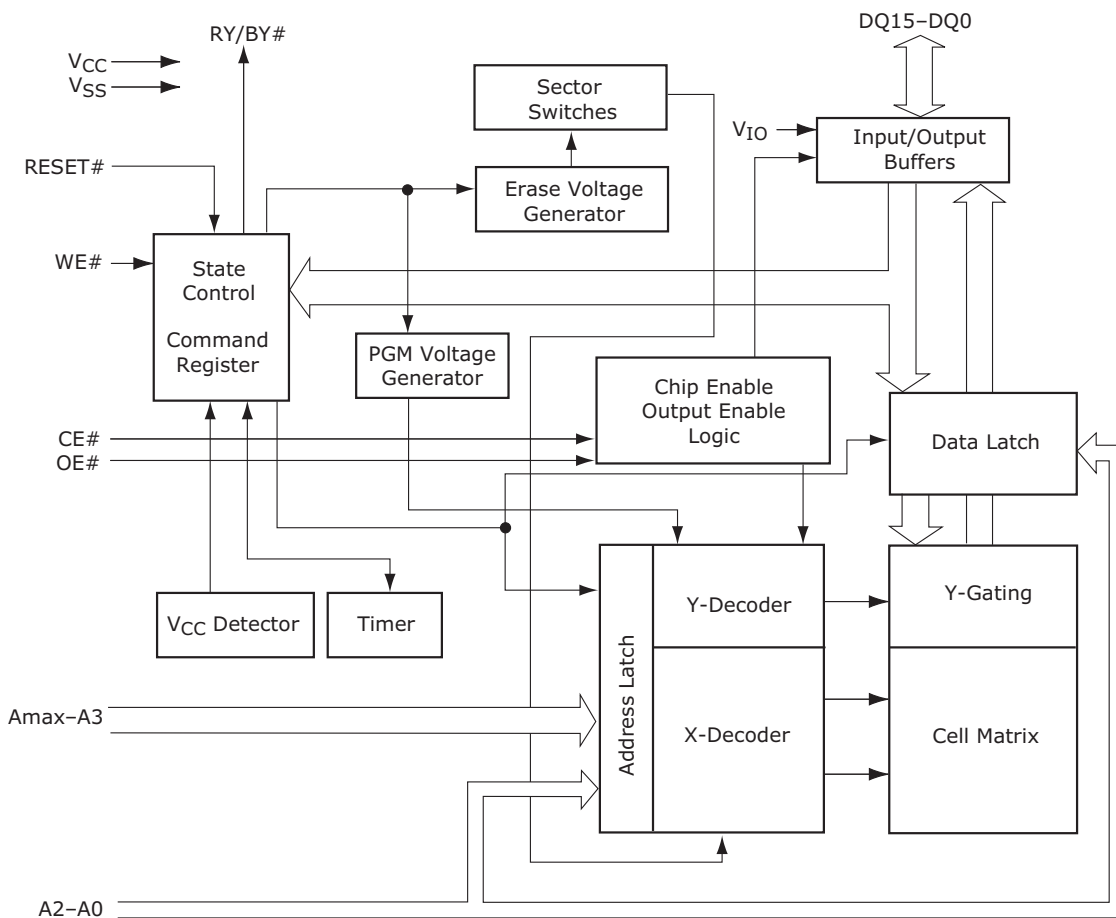
Notes
1. RY/BY# is an open drain output.
2. Amax = A22 (PL127J), A21 (PL129J and PL064J), A20 (PL032J).
3. For PL129J, there are two CE# (CE1# and CE2#).

6. Simultaneous Read/Write Block Diagram
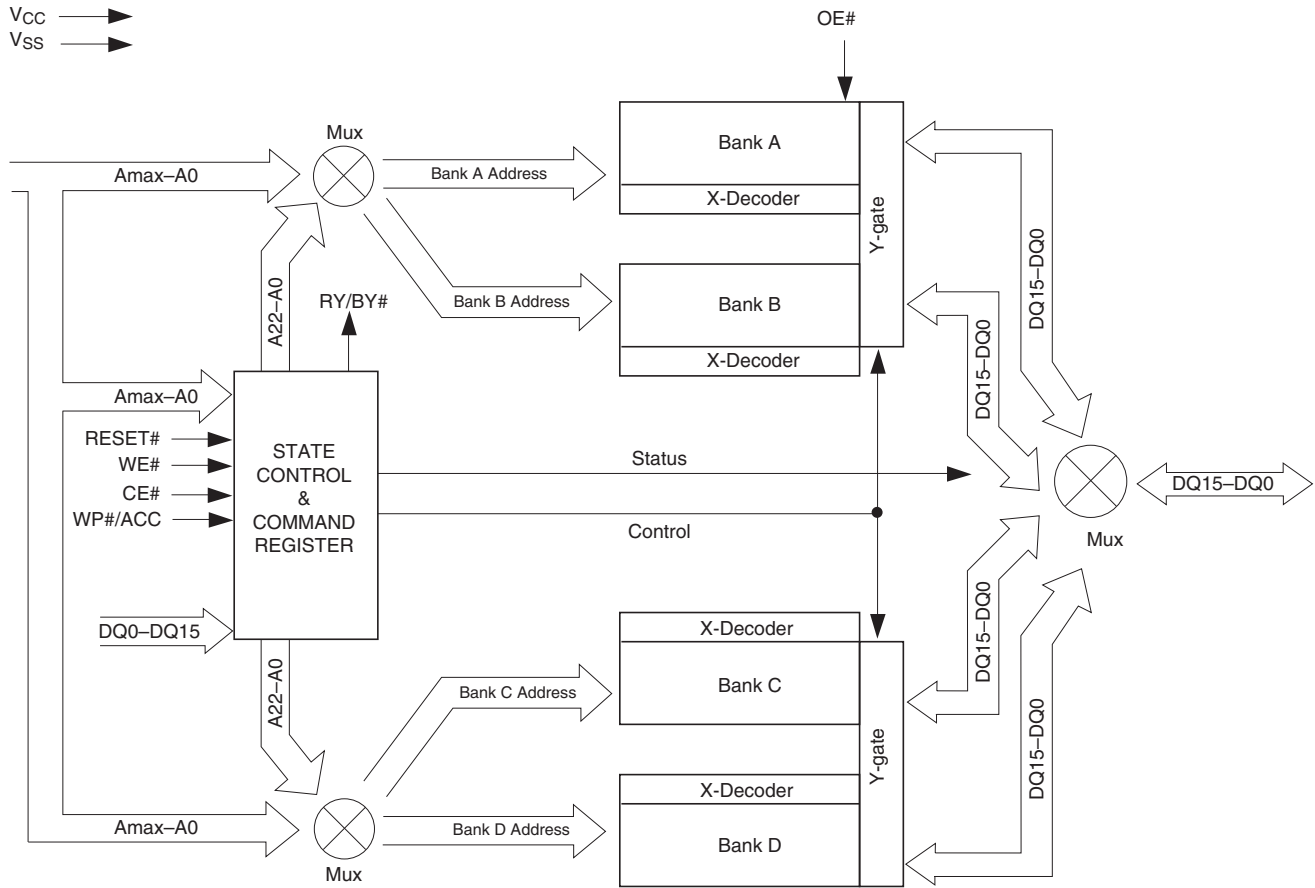
Note
Amax = A22 (PL127J), A21 (PL064J), A20 (PL032J)

7. Simultaneous Read/Write Block Diagram (PL129J)
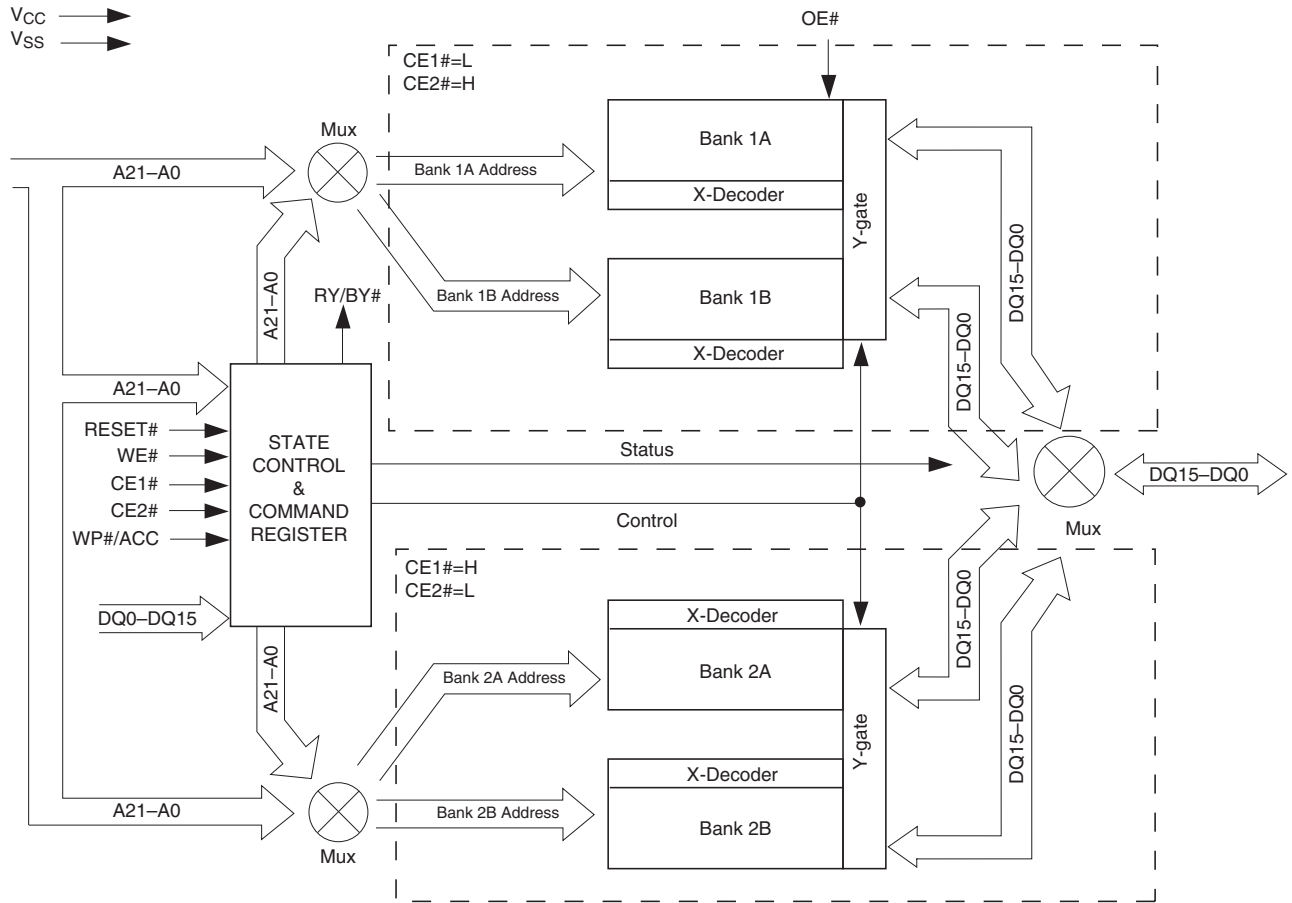
Note
Amax = A21 (PL129J)

8. Connection Diagrams

8.1 Special Package Handling Instructions

8.1.1 TSOP, BGA, PDIP, SSOP, and PLCC Packages

Special handling is required for Flash Memory products in molded packages.

The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

8.1.2 FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

8.2 80-Ball Fine-Pitch BGA—PL127J

Figure 8.1 80-Ball Fine-Pitch BGA, Top View, Balls Facing Down—PL127J
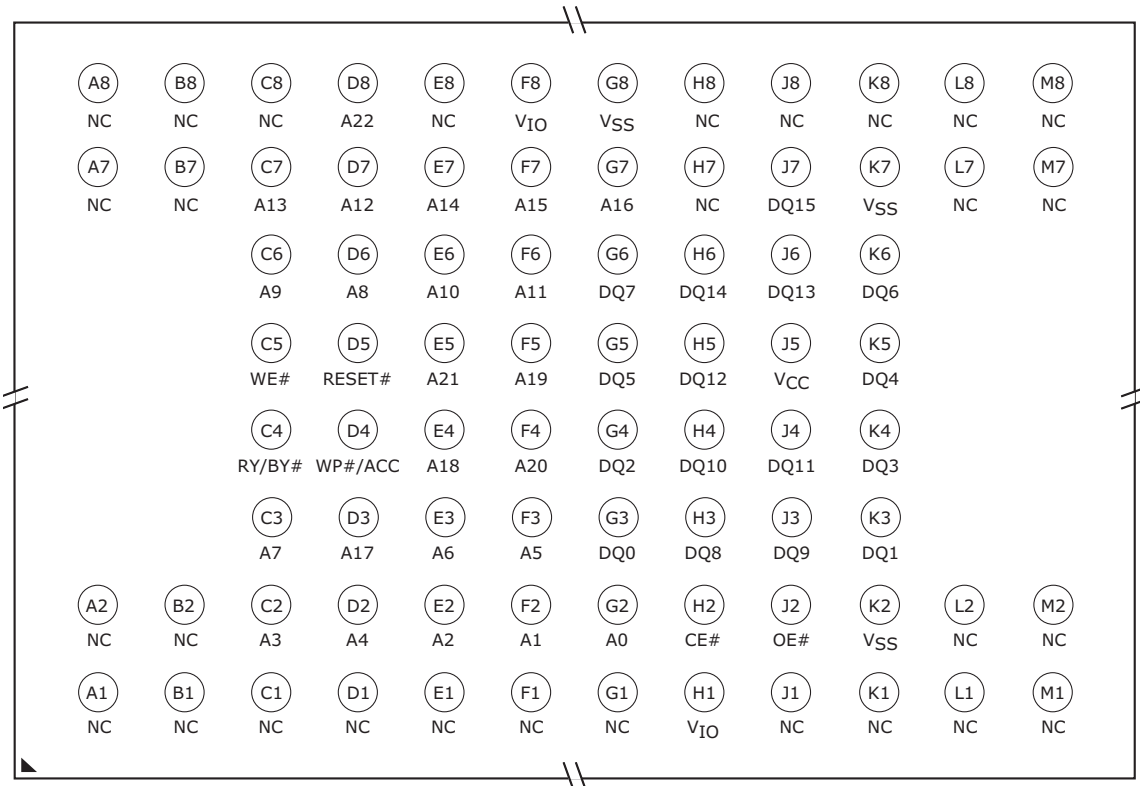
8.3   64-Ball Fine-Pitch BGA—MCP Compatible—PL127J

Figure 8.2 64-Ball Fine-Pitch BGA, MCP Compatible, Top View, Balls Facing Down—PL127J

A1 NC							**A10** NC
		B5 RFU	**B6** RFU				
	C3 A7	**C4** RFU	**C5** WP#/ACC	**C6** WE#	**C7** A8	**C8** A11	
D2 A3	**D3** A6	**D4** RFU	**D5** RESET#	**D6** RFU	**D7** A19	**D8** A12	**D9** A15
E2 A2	**E3** A5	**E4** A18	**E5** RY/BY #	**E6** A20	**E7** A9	**E8** A13	**E9** A21
F2 A1	**F3** A4	**F4** A17			**F7** A10	**F8** A14	**F9** A22
G2 A0	**G3** VSS	**G4** DQ1			**G7** DQ6	**G8** RFU	**G9** A16
H2 CE#f1	**H3** OE#	**H4** DQ9	**H5** DQ3	**H6** DQ4	**H7** DQ13	**H8** DQ15	**H9** VCCf
J2 RFU	**J3** DQ0	**J4** DQ10	**J5** VCCf	**J6** RFU	**J7** DQ12	**J8** DQ7	**J9** VSS
	K3 DQ8	**K4** DQ2	**K5** DQ11	**K6** RFU	**K7** DQ5	**K8** DQ14	
		L5 RFU	**L6** RFU				
M1 NC							**M10** NC

8.4   48-Ball Fine-Pitch BGA, PL064J and PL032J

Figure 8.3 48-Ball Fine-Pitch BGA, Top View, Balls Facing Down—PL064J—PL032J: C4(A21)=NC

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	NC	DQ15	V_{SS}

A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6

A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	A21	A19	DQ5	DQ12	V_{CC}	DQ4

A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	WP#/ACC	A18	A20	DQ2	DQ10	DQ11	DQ3

A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1

A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}
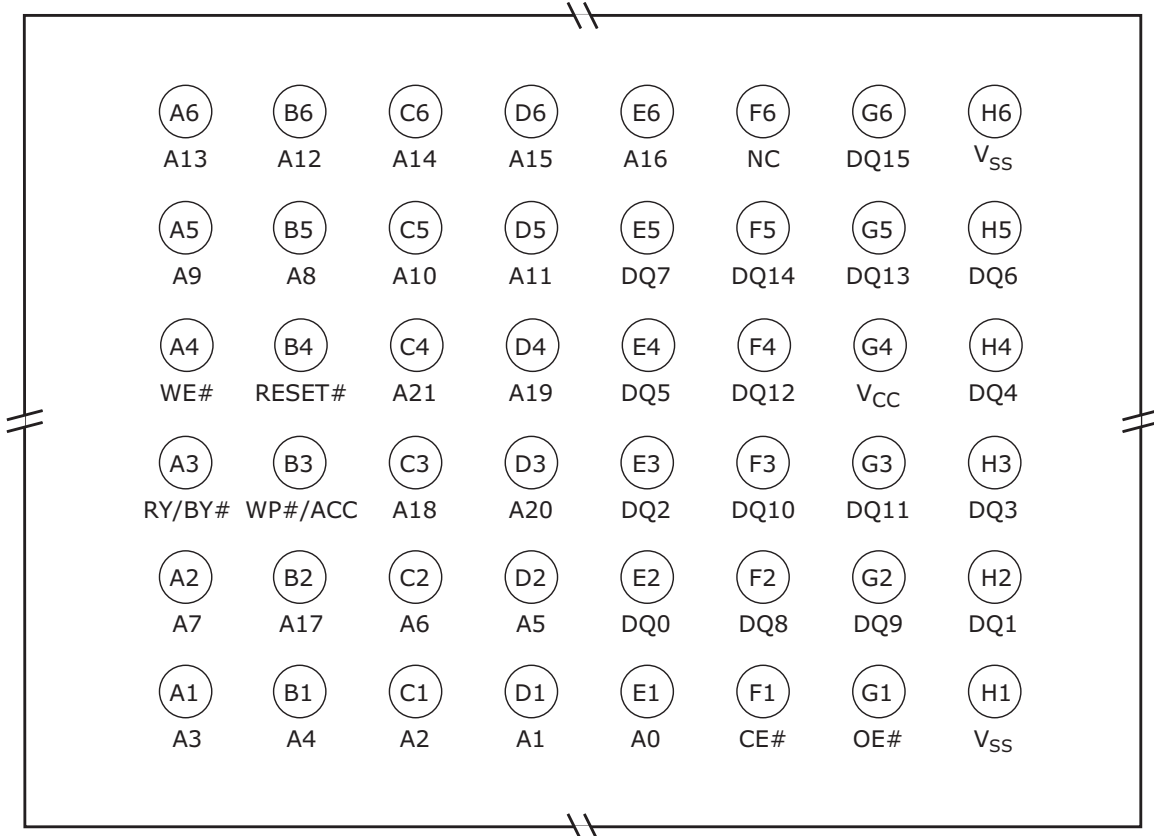
8.5   56-Pin TSOP 20 x 14 mm

Figure 8.4 56-Pin TSOP 20 x 14 mm Configuration—PL127J

Pin	Left Signal		Pin	Right Signal
1	RESET#		56	WP#/ACC
2	RY/BY#		55	WE#
3	A0		54	NC
4	A1		53	A22
5	A2		52	A21
6	A3		51	A20
7	A4		50	OE#
8	A5		49	NC
9	V_{CC}		48	CE#
10	DQ0		47	V_{SS}
11	DQ1		46	DQ15
12	DQ2		45	DQ14
13	DQ3		44	DQ13
14	V_{SSQ}		43	DQ12
15	V_{CCQ}		42	V_{SSQ}
16	DQ4		41	V_{CCQ}
17	DQ5		40	DQ11
18	DQ6		39	DQ10
19	DQ7		38	DQ9
20	V_{SS}		37	DQ8
21	NC		36	V_{CC}
22	A6		35	A19
23	A7		34	A18
24	A8		33	A17
25	A9		32	A16
26	A10		31	A15
27	A11		30	A14
28	A12		29	A13
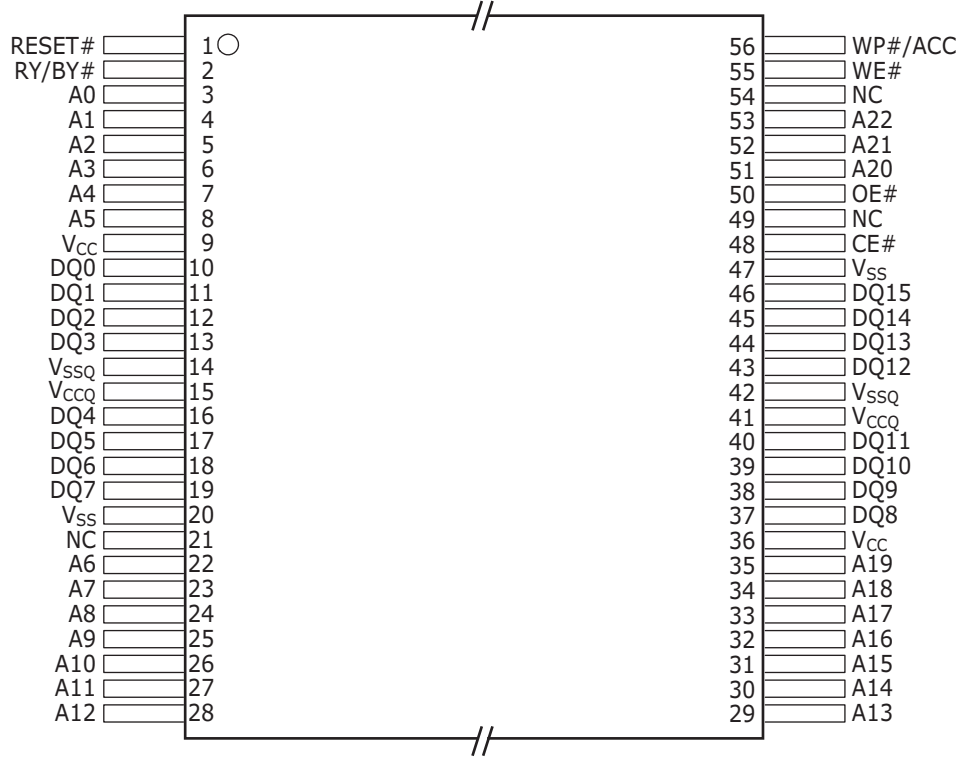
For this family of products, a single multi-chip compatible package (TSOP) is offered for each density to allow both standalone and multi-chip qualification using a single, adaptable package. This new methodology allows package standardization resulting in faster development. The multi-chip compatible package includes all the pins required for standalone device operation and verification. In addition, extra pins are included for insertion of common data storage or logic devices to be used for multi-chip products. If a standalone device is required, the extra multi-chip specific pins are not connected and the standalone device operates normally. The multi-chip compatible package sizes were chosen to serve the largest number of combinations possible. There are only a few cases where a larger package size would be required to accommodate the multi-chip combination. This multi-chip compatible package set does not allow for direct package migration from the Am29BDS128H, Am29BDS128G, Am29BDS640G products, which use legacy standalone packages.

8.6   56-Ball Fine-Pitch Ball Grid Array, PL064J and PL032J

Figure 8.5 56-ball Fine-Pitch BGA, Top View, Balls Facing Down,—PL064J and PL032J,

	A2	A3	A4	A5	A6	A7	
	A7	RFU	WP/ACC	WE#	A8	A11	
B1	B2	B3	B4	B5	B6	B7	B8
A3	A6	RFU	RST#	RFU	A19	A12	A15
C1	C2	C3	C4	C5	C6	C7	C8
A2	A5	A18	RY/BY#	A20	A9	A13	A21
D1	D2	D3			D6	D7	D8
A1	A4	A17			A10	A14	RFU
E1	E2	E3			E6	E7	E8
A0	VSS	DQ1			DQ6	RFU	A16
F1	F2	F3	F4	F5	F6	F7	F8
CE1#f	OE#	DQ9	DQ3	DQ4	DQ13	DQ15	RFU
G1	G2	G3	G4	G5	G6	G7	G8
RFU	DQ0	DQ10	VCCf	RFU	DQ12	DQ7	VSS
	H2	H3	H4	H5	H6	H7	
	DQ8	DQ2	DQ11	RFU	DQ5	DQ14	
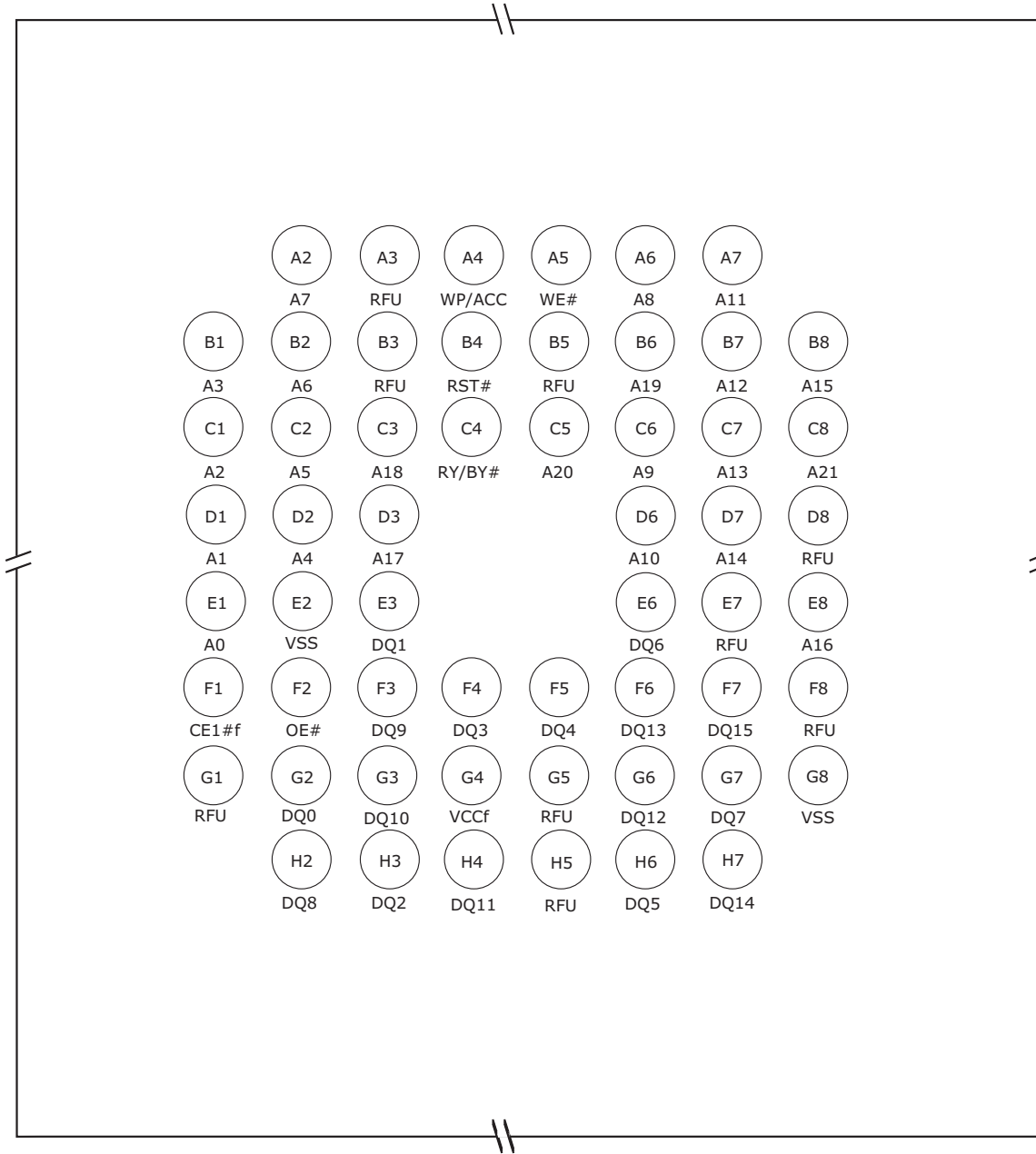
9. Pin Description

Table 9.1 Pin Description

Amax–A0	Address bus
DQ15–DQ0	16-bit data inputs/outputs/float
CE#	Chip Enable Inputs
OE#	Output Enable Input
WE#	Write Enable
V_{SS}	Device Ground
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).
RFU	Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.
RY/BY#	Ready/Busy output and open drain. When RY/BY#= V_{IH}, the device is ready to accept read operations and commands. When RY/BY#= V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
WP#/ACC	Write Protect/Acceleration Input. When WP#/ACC= V_{IL}, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP#/ACC= V_{IH}, these sector are unprotected unless the DYB or PPB is programmed. When WP#/ACC= V_{HH}, program and erase operations are accelerated.
V_{IO}	Input/Output Buffer Power Supply (1.65 V to 1.95 V (for PL127J and PL129J) or 2.7 V to 3.6 V (for all PLxxxJ devices))
V_{CC}	Chip Power Supply (2.7 V to 3.6 V or 2.7 to 3.3 V)
RESET#	Hardware Reset Pin
CE1#, CE2#	Chip Enable Inputs. CE1# controls the 64Mb in Banks 1A and 1B. CE2# controls the 64 Mb in Banks 2A and 2B. (Only for PL129J)

Note
Amax = A22 (PL127J), A21 (PL129J and PL064J), A20 (PL032J)

10. Logic Symbol
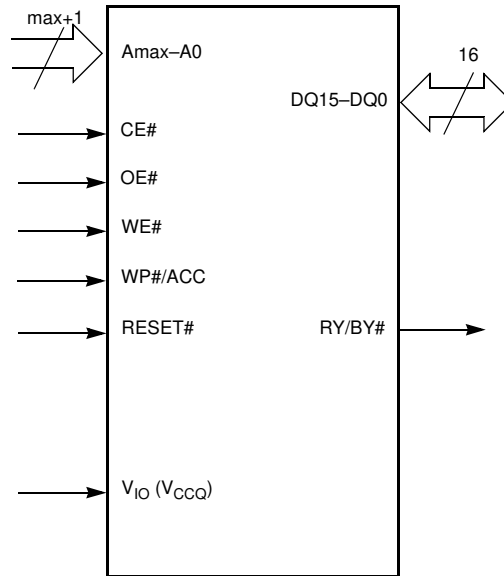
11. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 11.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 11.1 PL127J Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ ACC	Addresses (Amax–A0)	DQ15–DQ0
Read	L	L	H	H	X	A_{IN}	D_{OUT}
Write	L	H	L	H	X (Note 2)	A_{IN}	D_{IN}
Standby	$V_{IO}\pm0.3$ V	X	X	$V_{IO} \pm0.3$ V	X (Note 2)	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Table 11.2 PL129J Device Bus Operations

Operation	CE1#	CE2#	OE#	WE#	RESET#	WP#/ACC	Addresses (A21–A0)	DQ15–DQ0
Read	L	H	L	H	H	X	A_{IN}	D_{OUT}
	H	L						
Write	L	H	H	L	H	X (Note 2)	A_{IN}	D_{IN}
	H	L						
Standby	$V_{IO} \pm 0.3$ V	$V_{IO} \pm 0.3$ V	X	X	$V_{IO} \pm 0.3$ V	X	X	High-Z
Output Disable	L	L	H	H	H	X	X	High-Z
Reset	X	X	X	X	L	X	X	High-Z
Temporary Sector Unprotect (High Voltage)	X	X	X	X	V_{ID}	X	A_{IN}	D_{IN}

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 8.5–9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes
1. The sector protect and sector unprotect functions may also be implemented via programming equipment. See High Voltage Sector Protection on page 53.

2. WP#/ACC must be high when writing to upper two and lower two sectors.

11.1 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins (For PL129J - CE1#/CE2# pins) to V_{IL}. In PL129J, CE1# and CE2# are the power control and select the lower (CE1#) or upper (CE2#) halves of the device. CE# is the power control. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to Table 22.3 on page 91 for timing specifications and to Figure 21.3 on page 81 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

11.1.1 Random Read (Non-Page Read)

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

11.1.2 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A3 select an 8 word page, and address bits A2–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# (CE1# and CE#2 in PL129J) is deasserted (=V_{IH}), the reassertion of CE# (CE1# or CE#2 in PL129J) for subsequent access has access time of t_{ACC} or t_{CE}. Here again, CE# (CE1# /CE#2 in PL129J)selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping Amax–A3 constant and changing A2–A0 to select the specific word within that page.

Table 11.3 Page Select

Word	A2	A1	A0
Word 0	0	0	0
Word 1	0	0	1
Word 2	0	1	0
Word 3	0	1	1
Word 4	1	0	0
Word 5	1	0	1
Word 6	1	1	0
Word 7	1	1	1

11.2   Simultaneous Read/Write Operation

In addition to the conventional features (read, program, erase-suspend read, erase-suspend program, and program-suspend read), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (PL127J: A22–A20, PL129J and PL064J: A21–A19, PL032J: A20–A18) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

Table 11.4 Bank Select

Bank	PL127J: A22–A20, PL064J: A21–A19, PL032J: A20–A18
Bank A	000
Bank B	001, 010, 011
Bank C	100, 101, 110
Bank D	111

Bank	CE1#	CE2#	PL129J: A21–A20
Bank 1A	0	1	00
Bank 1B	0	1	01, 10, 11
Bank 2A	1	0	00, 01, 10
Bank 2B	1	0	11

11.3   Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# (CE1# or CE#2 in PL129J) to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. *Word Program Command Sequence on page 63* has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 11.4 on page 19 indicates the set of address space that each sector occupies. A "bank address" is the set of address bits required to uniquely select a bank. Similarly, a "sector address" refers to the address bits required to uniquely select a sector. *Command Definitions on page 61* has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

I_{CC2} in the *DC Characteristics on page 78* represents the active current specification for the write mode. See the timing specification tables and timing diagrams in section *Reset on page 82* for write operations.

11.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to V_{CC} when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

11.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Table 11.9, *Secured Silicon Sector Addresses on page 42* and *Autoselect Command Sequence on page 62* for more information.

11.4 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# (CE1#,CE#2 in PL129J) and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# (CE1#,CE#2 in PL129J) and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

ICC3 in *DC Characteristics on page 78* represents the CMOS standby current specification.

11.5 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC} + 30$ ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at V_{IH} before the device reduces current to the stated sleep mode specification. I_{CC5} in *DC Characteristics on page 78* represents the automatic sleep mode current specification.

11.6 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (ICC4). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3$ V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the tables in *AC Characteristic on page 79* for RESET# parameters and to Figure 21.5 on page 82 for the timing diagram.

11.7 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

Table 11.5 PL127J Sector Architecture

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank A	SA0	00000000000	4	000000h–000FFFh
	SA1	00000000001	4	001000h–001FFFh
	SA2	00000000010	4	002000h–002FFFh
	SA3	00000000011	4	003000h–003FFFh
	SA4	00000000100	4	004000h–004FFFh
	SA5	00000000101	4	005000h–005FFFh
	SA6	00000000110	4	006000h–006FFFh
	SA7	00000000111	4	007000h–007FFFh
	SA8	00000001XXX	32	008000h–00FFFFh
	SA9	00000010XXX	32	010000h–017FFFh
	SA10	00000011XXX	32	018000h–01FFFFh
	SA11	00000100XXX	32	020000h–027FFFh
	SA12	00000101XXX	32	028000h–02FFFFh
	SA13	00000110XXX	32	030000h–037FFFh
	SA14	00000111XXX	32	038000h–03FFFFh
	SA15	00001000XXX	32	040000h–047FFFh
	SA16	00001001XXX	32	048000h–04FFFFh
Bank A	SA17	00001010XXX	32	050000h–057FFFh
	SA18	00001011XXX	32	058000h–05FFFFh
	SA19	00001100XXX	32	060000h–067FFFh
	SA20	00001101XXX	32	068000h–06FFFFh
	SA21	00001110XXX	32	070000h–077FFFh
	SA22	00001111XXX	32	078000h–07FFFFh
	SA23	00010000XXX	32	080000h–087FFFh
	SA24	00010001XXX	32	088000h–08FFFFh
	SA25	00010010XXX	32	090000h–097FFFh
	SA26	00010011XXX	32	098000h–09FFFFh
	SA27	00010100XXX	32	0A0000h–0A7FFFh
	SA28	00010101XXX	32	0A8000h–0AFFFFh
	SA29	00010110XXX	32	0B0000h–0B7FFFh
	SA30	00010111XXX	32	0B8000h–0BFFFFh
	SA31	00011000XXX	32	0C0000h–0C7FFFh
	SA32	00011001XXX	32	0C8000h–0CFFFFh
	SA33	00011010XXX	32	0D0000h–0D7FFFh
	SA34	00011011XXX	32	0D8000h–0DFFFFh
	SA35	00011100XXX	32	0E0000h–0E7FFFh
	SA36	00011101XXX	32	0E8000h–0EFFFFh
	SA37	00011110XXX	32	0F0000h–0F7FFFh
	SA38	00011111XXX	32	0F8000h–0FFFFFh

Table 11.5 PL127J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank B	SA39	00100000XXX	32	100000h–107FFFh
	SA40	00100001XXX	32	108000h–10FFFFh
	SA41	00100010XXX	32	110000h–117FFFh
	SA42	00100011XXX	32	118000h–11FFFFh
	SA43	00100100XXX	32	120000h–127FFFh
	SA44	00100101XXX	32	128000h–12FFFFh
	SA45	00100110XXX	32	130000h–137FFFh
	SA46	00100111XXX	32	138000h–13FFFFh
	SA47	00101000XXX	32	140000h–147FFFh
	SA48	00101001XXX	32	148000h–14FFFFh
	SA49	00101010XXX	32	150000h–157FFFh
	SA50	00101011XXX	32	158000h–15FFFFh
	SA51	00101100XXX	32	160000h–167FFFh
	SA52	00101101XXX	32	168000h–16FFFFh
	SA53	00101110XXX	32	170000h–177FFFh
	SA54	00101111XXX	32	178000h–17FFFFh
	SA55	00110000XXX	32	180000h–187FFFh
	SA56	00110001XXX	32	188000h–18FFFFh
	SA57	00110010XXX	32	190000h–197FFFh
	SA58	00110011XXX	32	198000h–19FFFFh
	SA59	00110100XXX	32	1A0000h–1A7FFFh
	SA60	00110101XXX	32	1A8000h–1AFFFFh
	SA61	00110110XXX	32	1B0000h–1B7FFFh
	SA62	00110111XXX	32	1B8000h–1BFFFFh
	SA63	00111000XXX	32	1C0000h–1C7FFFh
	SA64	00111001XXX	32	1C8000h–1CFFFFh
	SA65	00111010XXX	32	1D0000h–1D7FFFh

Table 11.5 PL127J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
	SA66	00111011XXX	32	1D8000h–1DFFFFh
	SA67	00111100XXX	32	1E0000h–1E7FFFh
	SA68	00111101XXX	32	1E8000h–1EFFFFh
	SA69	00111110XXX	32	1F0000h–1F7FFFh
	SA70	00111111XXX	32	1F8000h–1FFFFFh
	SA71	01000000XXX	32	200000h–207FFFh
	SA72	01000001XXX	32	208000h–20FFFFh
	SA73	01000010XXX	32	210000h–217FFFh
	SA74	01000011XXX	32	218000h–21FFFFh
	SA75	01000100XXX	32	220000h–227FFFh
	SA76	01000101XXX	32	228000h–22FFFFh
	SA77	01000110XXX	32	230000h–237FFFh
	SA78	01000111XXX	32	238000h–23FFFFh
	SA79	01001000XXX	32	240000h–247FFFh
	SA80	01001001XXX	32	248000h–24FFFFh
	SA81	01001010XXX	32	250000h–257FFFh
	SA82	01001011XXX	32	258000h–25FFFFh
	SA83	01001100XXX	32	260000h–267FFFh
	SA84	01001101XXX	32	268000h–26FFFFh
	SA85	01001110XXX	32	270000h–277FFFh
	SA86	01001111XXX	32	278000h–27FFFFh
	SA87	01010000XXX	32	280000h–287FFFh
	SA88	01010001XXX	32	288000h–28FFFFh
Bank B	SA89	01010010XXX	32	290000h–297FFFh
	SA90	01010011XXX	32	298000h–29FFFFh
	SA91	01010100XXX	32	2A0000h–2A7FFFh
	SA92	01010101XXX	32	2A8000h–2AFFFFh
	SA93	01010110XXX	32	2B0000h–2B7FFFh
	SA94	01010111XXX	32	2B8000h–2BFFFFh
	SA95	01011000XXX	32	2C0000h–2C7FFFh
	SA96	01011001XXX	32	2C8000h–2CFFFFh
	SA97	01011010XXX	32	2D0000h–2D7FFFh
	SA98	01011011XXX	32	2D8000h–2DFFFFh
	SA99	01011100XXX	32	2E0000h–2E7FFFh
	SA100	01011101XXX	32	2E8000h–2EFFFFh
	SA101	01011110XXX	32	2F0000h–2F7FFFh
	SA102	01011111XXX	32	2F8000h–2FFFFFh
	SA103	01100000XXX	32	300000h–307FFFh
	SA104	01100001XXX	32	308000h–30FFFFh
	SA105	01100010XXX	32	310000h–317FFFh
	SA106	01100011XXX	32	318000h–31FFFFh
	SA107	01100100XXX	32	320000h–327FFFh
	SA108	01100101XXX	32	328000h–32FFFFh
	SA109	01100110XXX	32	330000h–337FFFh
	SA110	01100111XXX	32	338000h–33FFFFh
	SA111	01101000XXX	32	340000h–347FFFh

Table 11.5 PL127J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank B	SA115	01101100XXX	32	360000h–367FFFh
	SA116	01101101XXX	32	368000h–36FFFFh
	SA117	01101110XXX	32	370000h–377FFFh
	SA118	01101111XXX	32	378000h–37FFFFh
	SA119	01110000XXX	32	380000h–387FFFh
	SA120	01110001XXX	32	388000h–38FFFFh
	SA121	01110010XXX	32	390000h–397FFFh
	SA122	01110011XXX	32	398000h–39FFFFh
	SA123	01110100XXX	32	3A0000h–3A7FFFh
	SA124	01110101XXX	32	3A8000h–3AFFFFh
	SA125	01110110XXX	32	3B0000h–3B7FFFh
	SA126	01110111XXX	32	3B8000h–3BFFFFh
	SA127	01111000XXX	32	3C0000h–3C7FFFh
	SA128	01111001XXX	32	3C8000h–3CFFFFh
	SA129	01111010XXX	32	3D0000h–3D7FFFh
	SA130	01111011XXX	32	3D8000h–3DFFFFh
	SA131	01111100XXX	32	3E0000h–3E7FFFh
	SA132	01111101XXX	32	3E8000h–3EFFFFh
	SA133	01111110XXX	32	3F0000h–3F7FFFh
	SA134	01111111XXX	32	3F8000h–3FFFFFh

Table 11.5 PL127J Sector Architecture (Continued)

Bank	Sector	Sector Address (A22-A12)	Sector Size (Kwords)	Address Range (x16)
Bank C	SA135	10000000XXX	32	400000h–407FFFh
	SA136	10000001XXX	32	408000h–40FFFFh
	SA137	10000010XXX	32	410000h–417FFFh
	SA138	10000011XXX	32	418000h–41FFFFh
	SA139	10000100XXX	32	420000h–427FFFh
	SA140	10000101XXX	32	428000h–42FFFFh
	SA141	10000110XXX	32	430000h–437FFFh
	SA142	10000111XXX	32	438000h–43FFFFh
	SA143	10001000XXX	32	440000h–447FFFh
	SA144	10001001XXX	32	448000h–44FFFFh
	SA145	10001010XXX	32	450000h–457FFFh
	SA146	10001011XXX	32	458000h–45FFFFh
	SA147	10001100XXX	32	460000h–467FFFh
	SA148	10001101XXX	32	468000h–46FFFFh
	SA149	10001110XXX	32	470000h–477FFFh
	SA150	10001111XXX	32	478000h–47FFFFh
	SA151	10010000XXX	32	480000h–487FFFh
	SA152	10010001XXX	32	488000h–48FFFFh
	SA153	10010010XXX	32	490000h–497FFFh
	SA154	10010011XXX	32	498000h–49FFFFh
	SA155	10010100XXX	32	4A0000h–4A7FFFh
	SA156	10010101XXX	32	4A8000h–4AFFFFh
	SA157	10010110XXX	32	4B0000h–4B7FFFh
	SA158	10010111XXX	32	4B8000h–4BFFFFh
	SA159	10011000XXX	32	4C0000h–4C7FFFh
	SA160	10011001XXX	32	4C8000h–4CFFFFh
	SA161	10011010XXX	32	4D0000h–4D7FFFh
	SA162	10011011XXX	32	4D8000h–4DFFFFh
	SA163	10011100XXX	32	4E0000h–4E7FFFh