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EPSON
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S2D13515 Display Controller

S5U13515P00C100 Evaluation Board User Manual

SEIKO EPSON CORPORATION

Rev 1.1

NOTICE

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Chapter 1 Introduction

This manual describes the setup and operation of the S5U13515P00C100 Evaluation Board. The evaluation board is designed as an evaluation platform for the S2D13515 Display Controller.

The S5U13515P00C100 evaluation board can be used with many native platforms via the host connector which provides the appropriate signals to support a variety of CPUs. The S5U13515P00C100 evaluation board can also connect to the S5U13U00P00C100 USB Adapter board so that it can be used with a laptop or desktop computer, via USB 2.0.

This user manual is updated as appropriate. Please check the Epson Research and Development Website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

Chapter 2 Features

The S5U13515P00C100 Evaluation Board includes the following features:

- 256-pin PBGA S2D13515 Display Controller
- On-board SDRAM, configurable as 32MB (32-bit wide) or 16MB (16-bit wide)
- On-board Serial Flash Memory, 32Mbit
- Headers for connection to various Host Bus Interfaces (includes all S2D13515 Host Bus Interface signals)
- Headers for connection to the S5U13U00P00C100 USB Adapter board
- Headers for connection to various LCD panels (includes all S2D13515 FP1IO and FP2IO interface signals)
- Header for connection to cameras
- Header for I2S outputs
- On-board 3x3 keypad
- On-board 20MHz crystal
- 14-pin DIP socket (if an oscillator for CLKI input is required)
- 3.3V input power
- On-board voltage regulator with 1.8V output
- On-board voltage regulator with adjustable 12~25V output, 60~100mA max., to provide power for LED back-light of LCD panels.

Chapter 3 Installation and Configuration

The S5U13515P00C100 evaluation board incorporates a DIP switch, jumpers, and 0 ohm resistors which allow it to be used with a variety of different configurations.

3.1 CNF[7:0] Configuration Inputs

The S2D13515 has 8 configuration inputs (CNF[7:0]), which can be configured through a combination of a DIP switch and 0 ohm resistors. CNF[2:0] are dedicated inputs and are configured using DIP switch SW1. CNF[7:3] are multiplexed with some host interface signals and are configured by 0 ohm resistors.

3.1.1 CNF[2:0]

CNF[2:0] are configured using DIP switch SW1 as described below.

Table 3-1: CNF[2:0] Configuration Settings

CNF[2:0]	1 (connected to HIOVDD)	0 (connected to VSS)
CNF2	CNF[2:1] are used in combination with CNF[7:3] to select the host bus interface. For a summary of the possible host bus interfaces, see Section Table 3-3 :, “Host Interface Configuration Settings” on page 9.	
CNF1		
CNF0	OSCI is the source for Input Clock 1	CLKI is the source for Input Clock 1

= suggested settings

The following figure shows the location of DIP switch SW1 on the S5U13515P00C100 evaluation board.

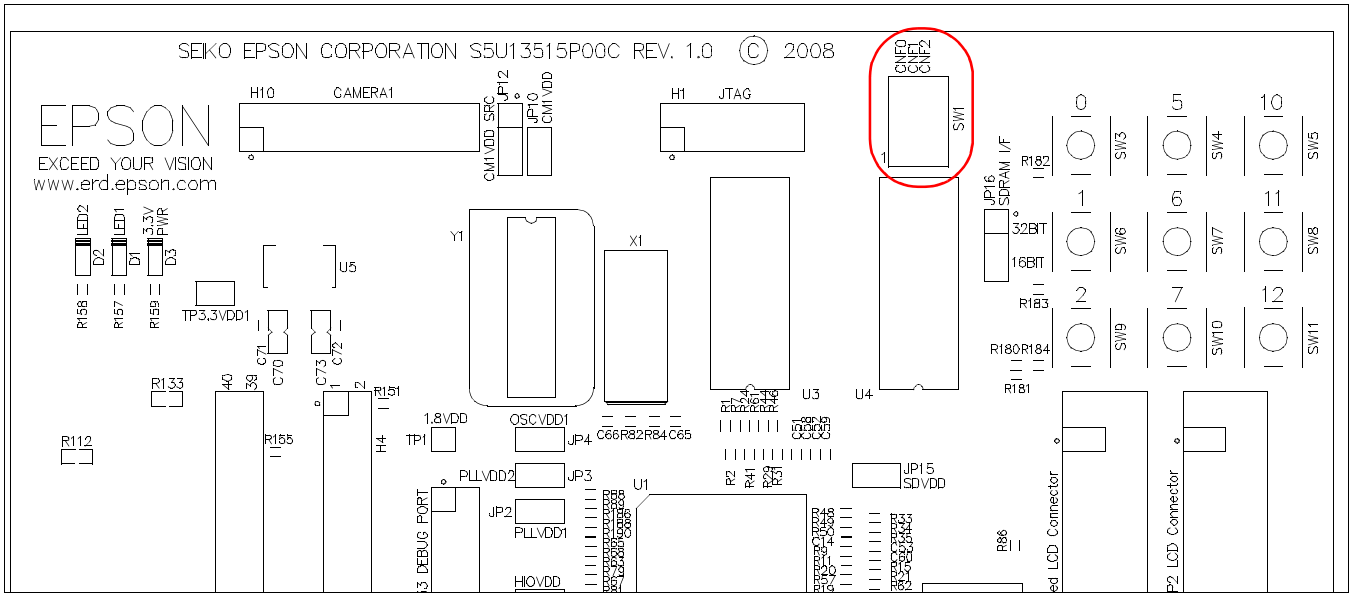

Figure 3-1: Configuration DIP Switch (SW1) Location

3.1.2 CNF[7:3]

CNF[7:3] are configured using 0 Ohm resistors as described below.

Table 3-2: CNF[7:3] Configuration Settings

CNF	Pin	1 (connected to HIOVDD)	0 (connected to VSS)
CNF3 (see Note)	TEA#	R100 populated R107 not populated	R100 not populated R107 populated
	AB0	R99 populated R106 not populated	R99 not populated R106 populated
CNF4	BDIP#	R95 populated R102 not populated	R95 not populated R102 populated
CNF5	BURST#	R96 populated R103 not populated	R96 not populated R103 populated
CNF6 (see Note)	AB3	R98 populated R105 not populated	R98 not populated R105 populated
	BE1#	R97 populated R104 not populated	R97 not populated R104 populated
	AB0	R99 populated R106 not populated	R99 not populated R106 populated
CNF7	AB4	R101 populated R108 not populated	R101 not populated R108 populated

= default settings, required settings when using S5U13U00P00C100 USB Adapter Board

Note
CNF3 and CNF6 are mapped to different pins depending on the combination of the other CNF inputs.

The following figure shows the location of the 0 Ohm resistors used to configure CNF[7:3].

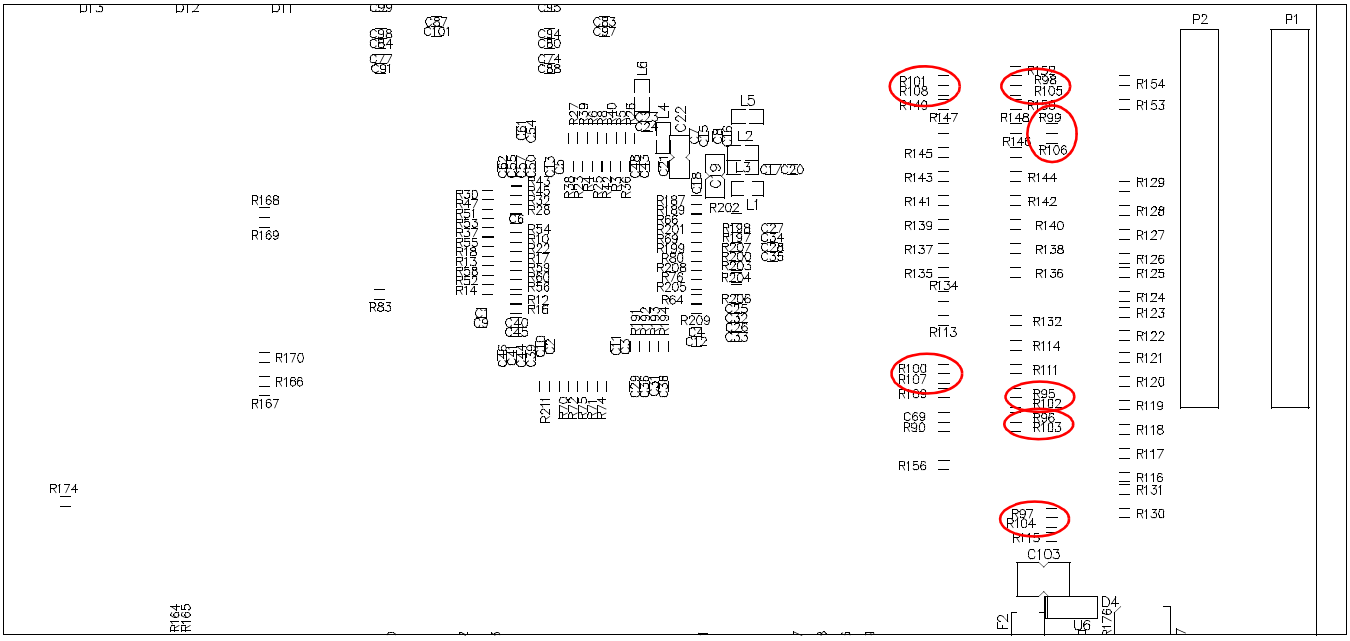

Figure 3-2: CNF[7:3] 0 Ohm Resistor Locations

3.1.3 Host Interface Configuration

The host bus interface used by the S5U13515P00C100 evaluation board is selected using a combination of the CNF[2:1] pins and unused host interface pins. Many host bus interfaces have unused pins that can be used as configuration pins (CNF[7:3]) to select the host bus interface. The following table summarizes the available settings.

Table 3-3 : Host Interface Configuration Settings

CNF1	CNF2	CNF3	CNF4	CNF5	CNF6	CNF7	Host Interface
0	0	0 (TEA#)	0 (BDIP#)	0 (BURST#)	0 (AB3)	X	Indirect, 8-bit, Intel80 Type1
0	0	0 (TEA#)	0 (BDIP#)	0 (BURST#)	1 (AB3)	X	Indirect, 8-bit, Intel80 Type2
0	0	0 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (AB3)	0 (AB4)	SPI
0	0	0 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (AB3)	1 (AB4)	I2C
0	0	0 (TEA#)	1 (BDIP#)	0 (BURST#)	0 (AB3)	X	Indirect, 8-bit, NEC V850 Type1
0	0	0 (TEA#)	1 (BDIP#)	0 (BURST#)	1 (AB3)	X	Indirect, 8-bit, NEC V850 Type2
0	0	0 (TEA#)	1 (BDIP#)	1 (BURST#)	0 (AB3)	X	Indirect, 8-bit, Renesas SH4
0	1	0 (TEA#)	0 (BDIP#)	0 (BURST#)	0 (AB3)	X	Indirect, 16-bit, Intel80 Type1
0	1	0 (TEA#)	0 (BDIP#)	0 (BURST#)	1 (AB3)	X	Indirect, 16-bit, Intel80 Type2
0	1	0 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (AB3)	0 (AB4)	SPI (2-stream)
0	1	0 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (AB3)	1 (AB4)	I2C
0	1	0 (TEA#)	1 (BDIP#)	0 (BURST#)	0 (AB3)	X	Indirect, 16-bit, NEC V850 Type1
0	1	0 (TEA#)	1 (BDIP#)	0 (BURST#)	1 (AB3)	X	Indirect, 16-bit, NEC V850 Type2
0	1	0 (TEA#)	1 (BDIP#)	1 (BURST#)	0 (AB3)	X	Indirect, 16-bit, Renesas SH4
0	0	1 (TEA#)	0 (BDIP#)	0 (BURST#)	0 (BE1#)	X	Direct, 8-bit, Intel80 Type1
0	0	1 (TEA#)	0 (BDIP#)	0 (BURST#)	1 (BE1#)	X	Direct, 8-bit, Intel80 Type2
0	0	1 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (BE1#)	0 (AB4)	SPI
0	0	1 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (BE1#)	1 (AB4)	I2C
0	0	1 (TEA#)	1 (BDIP#)	0 (BURST#)	0 (BE1#)	X	Direct, 8-bit, NEC V850 Type1
0	0	1 (TEA#)	1 (BDIP#)	0 (BURST#)	1 (BE1#)	X	Direct, 8-bit, NEC V850 Type2
0	0	1 (TEA#)	1 (BDIP#)	1 (BURST#)	0 (BE1#)	X	Direct, 8-bit, Renesas SH4
0	1	1 (TEA#)	0 (BDIP#)	0 (BURST#)	0 (AB0)	X	Direct, 16-bit, Intel80 Type1
0	1	1 (TEA#)	0 (BDIP#)	0 (BURST#)	1 (AB0)	X	Direct, 16-bit, Intel80 Type2
0	1	1 (TEA#)	0 (BDIP#)	1 (BURST#)	0 (AB0)	X	Direct, 16-bit, Intel PXA3xxs
0	1	1 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (AB0)	0 (AB4)	SPI
0	1	1 (TEA#)	0 (BDIP#)	1 (BURST#)	1 (AB0)	1 (AB4)	I2C
0	1	1 (TEA#)	1 (BDIP#)	0 (BURST#)	0 (AB0)	X	Direct, 16-bit, NEC V850 Type1
0	1	1 (TEA#)	1 (BDIP#)	0 (BURST#)	1 (AB0)	X	Direct, 16-bit, NEC V850 Type2
0	1	1 (TEA#)	1 (BDIP#)	1 (BURST#)	0 (AB0)	X	Direct, 16-bit, Renesas SH4
1	0	0 (AB0)	X	X	X	X	Indirect, 16-bit, TI EBI
1	0	1 (AB0)	X	X	X	X	Direct, 16-bit, TI EBI
1	1	0 (BE1#)	X	X	X	X	Indirect, 16-bit, MPC555
1	1	1 (BE1#)	X	X	X	X	Direct, 16-bit, MPC555

= default settings, required settings when using S5U13U00P00C100 USB Adapter Board

X = don't care

3.2 Configuration Jumpers

The S5U13515P00C100 has 16 jumpers which configure various evaluation board settings. The jumper positions for each function are shown below.

Table 3-4: Configuration Jumper Settings

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	COREVDD	Normal	—	COREVDD current measurement
JP2	PLL1VDD	Normal	—	PLL1VDD current measurement
JP3	PLL2VDD	Normal	—	PLL2VDD current measurement
JP4	OSCVDD	Normal	—	OSCVDD current measurement
JP5	PIO1VDD	Normal	—	PIO1VDD current measurement
JP6	HIOVDD	Normal	—	HIOVDD current measurement
JP7	HIOVDD Source	H4 connector, pin 31	3.3VDD	—
JP8	PIO1VDD Source	H9 connector, pin 9	3.3VDD	—
JP9	PIO2VDD Source	H9 connector, pin 10	3.3VDD	—
JP10	CM1VDD	Normal	—	CM1VDD current measurement
JP11	PIO2VDD	Normal	—	PIO2VDD current measurement
JP12	CM1DD Source	H9 connector, pin 8	3.3VDD	—
JP13	IOVDD Source	H9 connector, pin 7	3.3VDD	—
JP14	IOVDD	Normal	—	IOVDD current measurement
JP15	SDVDD	Normal	—	SDVDD current measurement
JP16	SDRAM Width Select (see Note)	32-bit wide SDRAM	16-bit wide SDRAM	—

= Required settings when using S5U13U00P00C100 USB Adapter board

JP1, JP2, JP3, JP4, JP5, JP6, JP10, JP11, JP14, JP15 - Power Supplies for the S2D13515

JP1, JP2, JP3, JP4, JP5, JP6, JP10, JP11, JP14, and JP15 can be used to measure the current consumption of each S2D13515 power supply.
When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, the current consumption for each power supply can be measured by connecting an ammeter to pin 1 and 2 of the jumper.

The jumper associated with each power supply is as follows:

JP1 for COREVDD	JP2 for PLL1VDD
JP3 for PLL2VDD	JP4 for OSCVDD
JP5 for PIO1VDD	JP6 for HIOVDD
JP10 for CM1VDD	JP11 for PIO2VDD
JP14 for IOVDD	JP15 for SDVDD

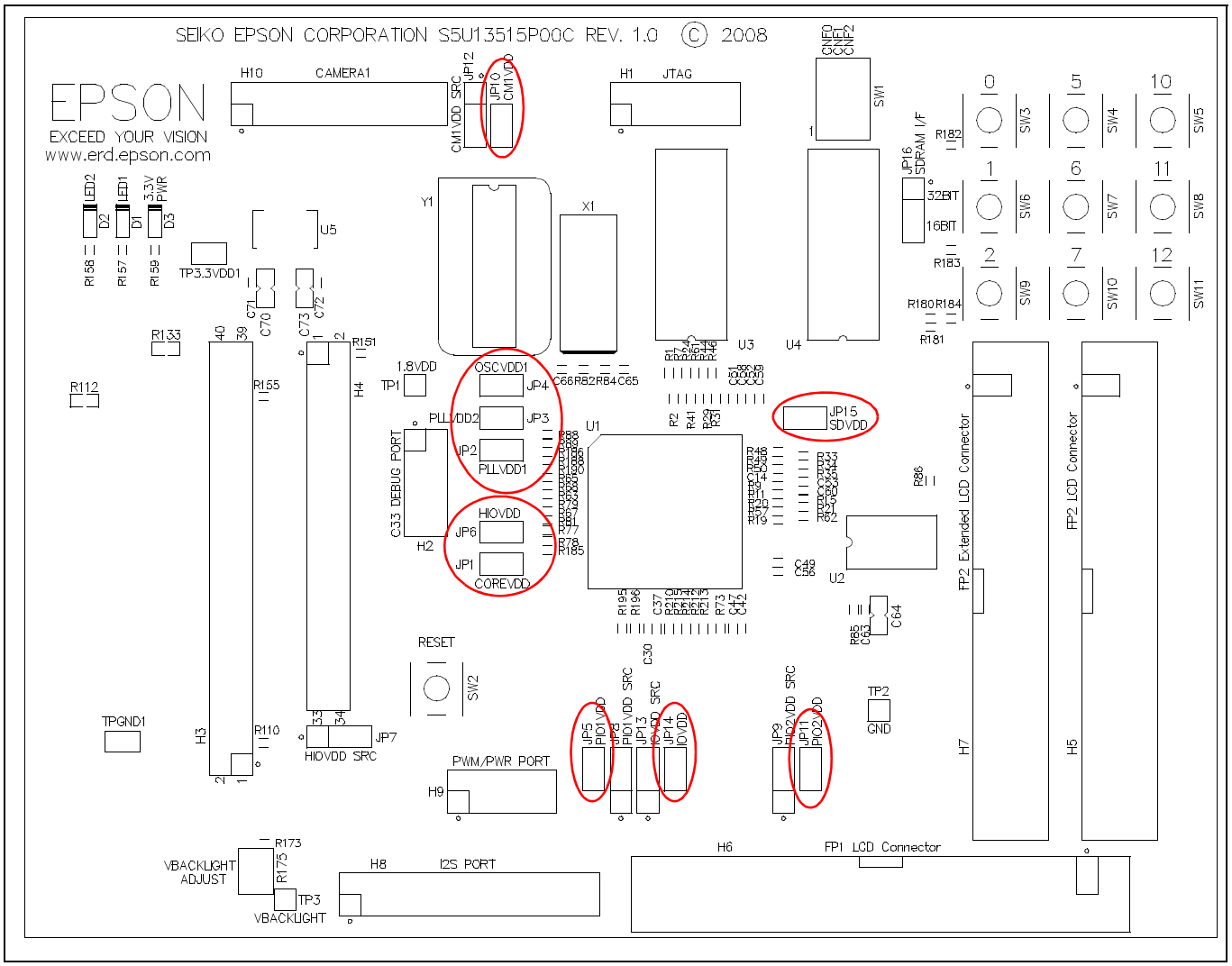

Figure 3-3: Configuration Jumper Locations (JP1, JP2, JP3, JP4, JP5, JP6, JP10, JP11, JP14, JP15)

JP7 - HIOVDD Source

JP7 is used to select the source for the HIOVDD supply voltage.
When the jumper is at position 1-2, the HIOVDD voltage must be provided to pin 31 on the H4 connector.
When the jumper is at position 2-3, the HIOVDD voltage is provided by the 3.3V power supply of the board.

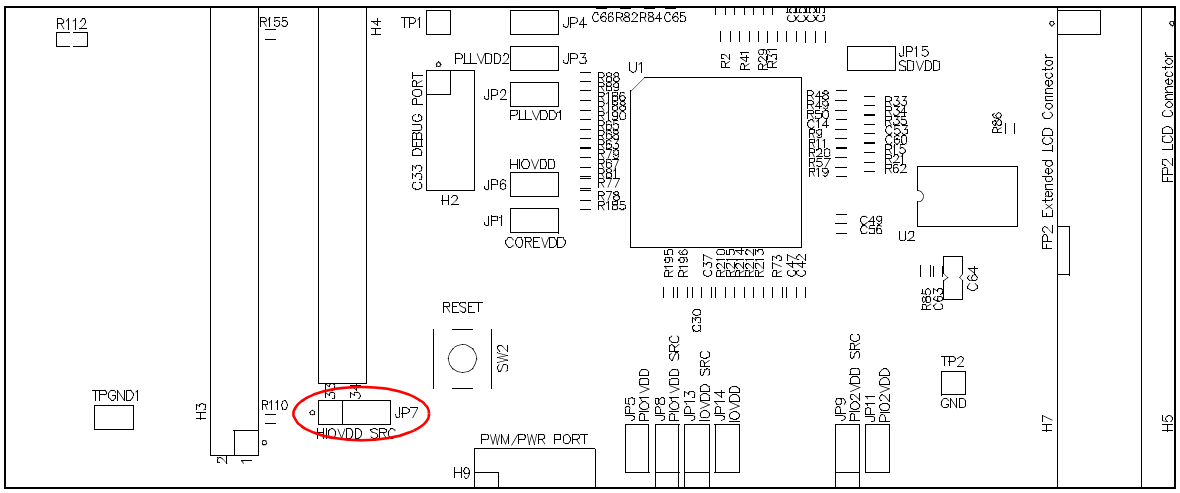

Figure 3-4: Configuration Jumper Location (JP7)

JP8 - PIO1VDD Source

JP8 is used to select the source for the PIO1VDD supply voltage.
When the jumper is at position 1-2, the PIO1VDD voltage must be provided to pin 9 on the H9 connector.
When the jumper is at position 2-3, the PIO1VDD voltage is provided by the 3.3V power supply of the board.

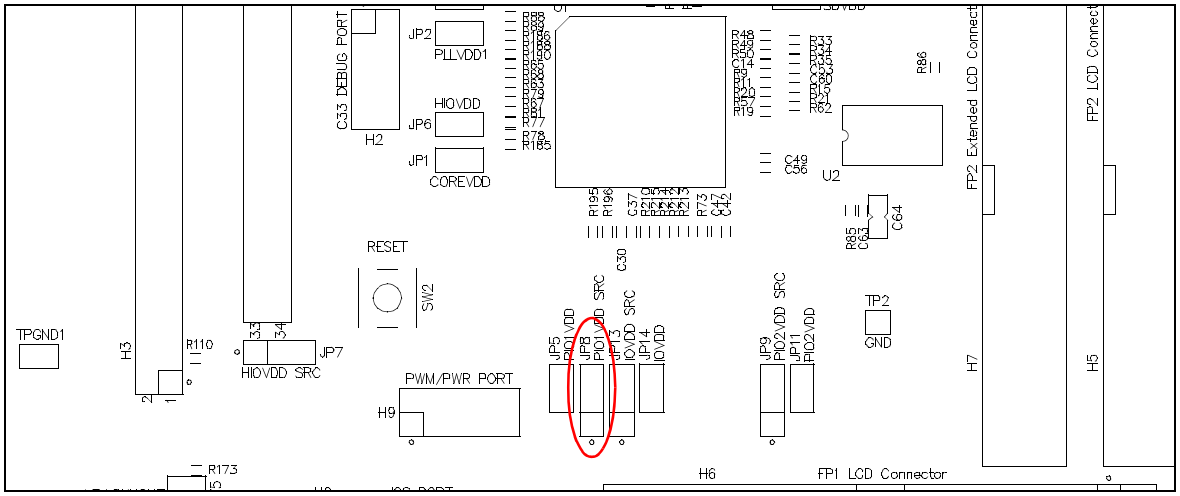

Figure 3-5: Configuration Jumper Location (JP8)

JP9 - PIO2VDD Source

JP9 is used to select the source for the PIO2VDD supply voltage.
When the jumper is at position 1-2, the PIO2VDD voltage must be provided to pin 10 on the H9 connector.
When the jumper is at position 2-3, the PIO2VDD voltage is provided by the 3.3V power supply of the board.

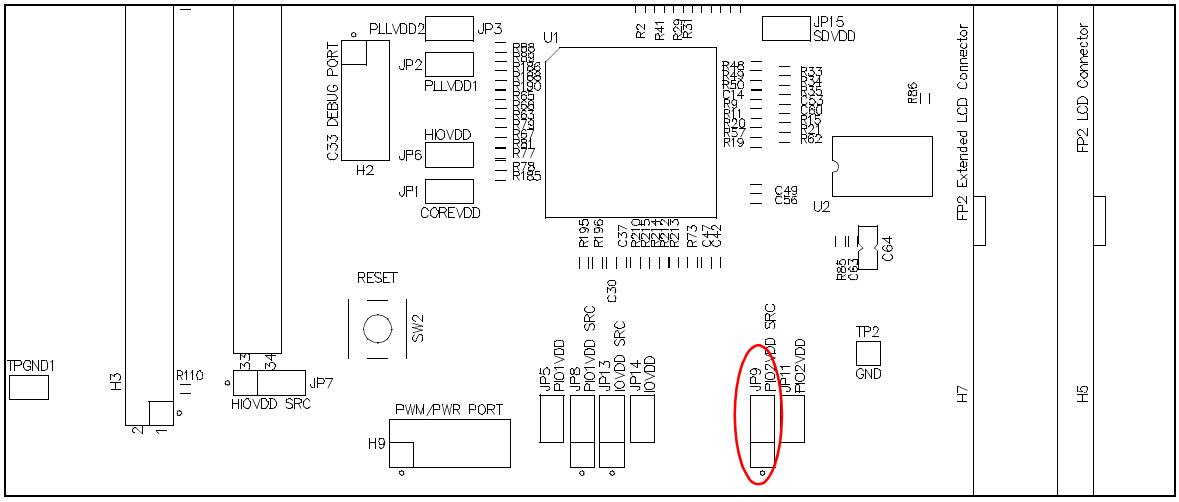

Figure 3-6: Configuration Jumper Location (JP9)

JP12 - CM1VDD Source

JP12 is used to select the source for the CM1VDD supply voltage.
When the jumper is at position 1-2, the CM1VDD voltage must be provided to pin 8 on the H9 connector.
When the jumper is at position 2-3, the CM1VDD voltage is provided by the 3.3V power supply of the board.

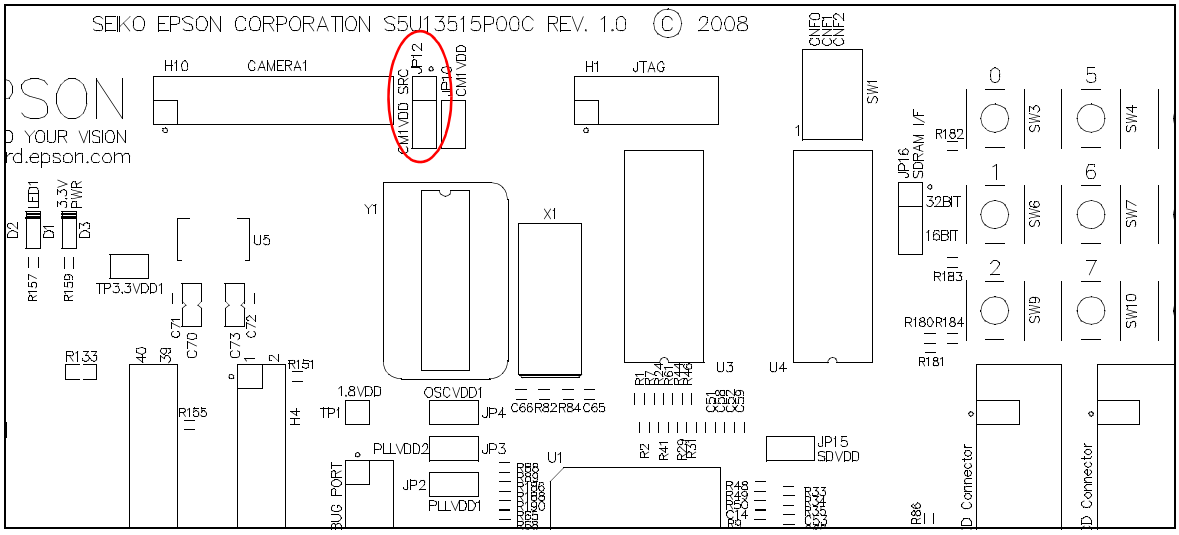

Figure 3-7: Configuration Jumper Location (JP12)

JP13 - IOVDD Source

JP13 is used to select the source for the IOVDD supply voltage.
When the jumper is at position 1-2, the IOVDD voltage must be provided to pin 7 on the H9 connector.
When the jumper is at position 2-3, the IOVDD voltage is provided by the 3.3V power supply of the board.

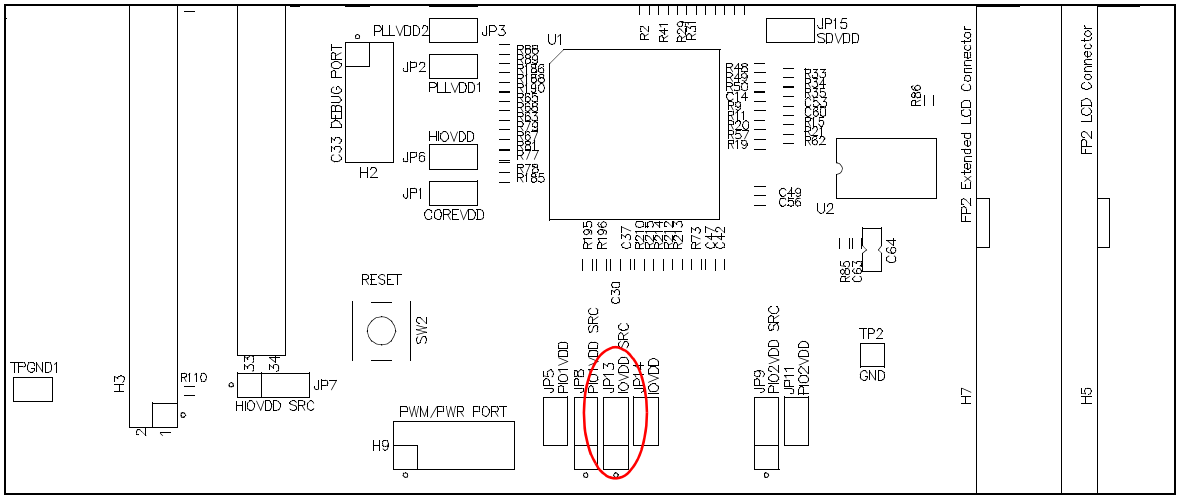

Figure 3-8: Configuration Jumper Location (JP13)

JP16 - SDRAM Width Select

JP16 is used to select the bus width of the external SDRAM.
When the jumper is at position 1-2, the external SDRAM is 32 bits wide and the memory size is 32M bytes. In this configuration, the memory consists of 2 chips in parallel, each16M bytes and 16 bits wide.
When the jumper is at position 2-3, the external SDRAM is 16 bits wide and the memory size is 16M bytes. In this configuration, one memory chip is disabled and only one chip is active (16M bytes and 16 bits wide).

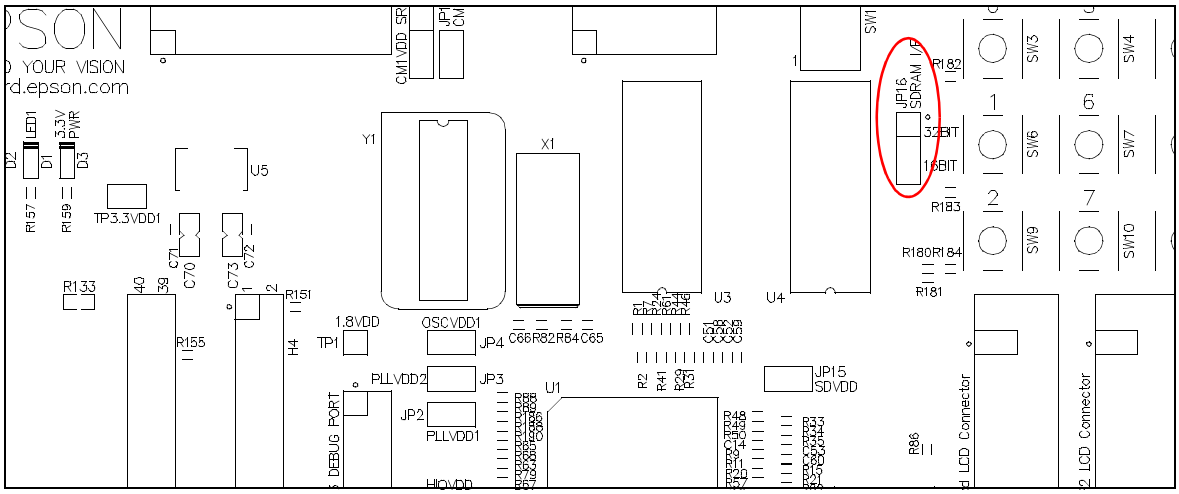

Figure 3-9: Configuration Jumper Location (JP16)

Chapter 4 Technical Description

4.1 Power

4.1.1 Power Requirements

The S5U13515P00C100 evaluation board requires an external regulated power supply (3.3V / 1A). The power is supplied to the evaluation board through pin 33 of the H4 header, or pin 5 of the P2 header.

The green LED “3.3V Power” is turned on when 3.3V power is applied to the board.

4.1.2 Voltage Regulators

The S5U13515P00C100 evaluation board has an on-board linear regulator to provide the 1.8V power required by the S2D13515 Display Controller. It also has a step-up switching voltage regulator to generate adjustable 12~25V, which can be used to power the LED backlight on some LCD panels.

4.1.3 S2D13515 Power

The S2D13515 Display Controller requires 1.8V power and 2.3~2.7V or 3.0~3.6V power.

COREVDD, PLL1VDD, PLL2VDD, and OSCVDD require 1.8V power which is provided by an on-board linear voltage regulator.

HIOVDD, PIO1VDD, PIO2VDD, CM1VDD, and IOVDD input power may be in the range 2.3V~2.7V or 3.0V~3.6V. When JP7, JP8, JP9, JP12, or JP13 are set to the 2-3 position, the corresponding power input is connected to 3.3V. If a different voltage is required, set the corresponding jumper to the 1-2 position and connect the external power supply to the evaluation board as indicated in Table 3-4: “Configuration Jumper Settings,” on page 10.

SDVDD input power may be in the range 2.3V~2.7V or 3.0V~3.6V. On the evaluation board, SDVDD is connected to 3.3V.

4.1.4 LCD Backlight Power

On the evaluation board there is an adjustable 12~25V power supply. At 12V, the maximum current available is 100mA. At 25V, the maximum current available is 60mA. This power supply is intended for use to power the LED backlight on some LCD panels. The voltage is adjusted by the R175 pot.

Note
For LCD panels that use a CCFL backlight, an external power supply must be used to provide power to the inverter for the CCFL backlight. Usually, the inverter current consumption is higher than the maximum 100mA current available from the on-board voltage regulator.

4.2 Clocks

The clock for the S2D13515 Display Controller is provided by a 20MHz crystal connected to the OSCI and OSCO pins.

Additionally, the S5U13515P00C100 evaluation board can also use an oscillator if the DIP14 footprint is populated. If populated, the oscillator is connected to the CLKI input clock of the S2D13515 Display controller.

Note
For details on the S2D13515 clock structure, refer to the *S2D13515 Hardware Functional Specification*, document number X83A-A-001-xx.

4.3 Reset

The S2D13515 Display Controller on the S5U13515P00C100 evaluation board can be reset using a push-button switch (SW2), or via an active low reset signal from the host development platform (pin 30 on the H4 connector).

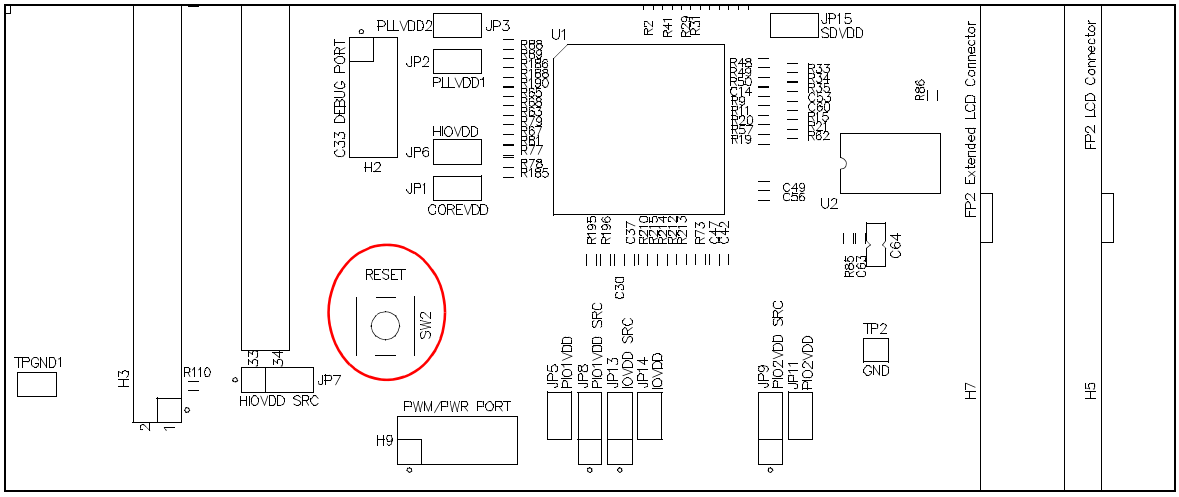

Figure 4-1: Reset Switch (SW2) Location

4.4 Memory

4.4.1 SDRAM

The S5U13515P00C100 evaluation board has 2 SDRAM ICs, each 128Mbit x16-bit, CL=2 in a TSOP54 package. When the S2D13515 Display Controller is configured for 32-bit wide DRAM bus, both SDRAM ICs are used. When the S2D13515 Display Controller is configured for 16-bit wide DRAM bus, only one of the SDRAM ICs is used and the other SDRAM ICs is disabled by having its chip select input pulled high to inactive state, by putting jumper JP16 in 2-3 position.

4.4.2 Serial Flash Memory with SPI interface

The S2D13515 Display Controller has a SPI Flash Memory interface which is connected to a 32Mbit Flash EPROM.

4.5 Host Interface

4.5.1 Direct Host Bus Interface Support

All S2D13515 host interface pins are available on connectors H3 and H4. This allows the S5U13515P00C100 evaluation board to be connected to a variety of development platforms. For S2D13515 host interface pin mapping, refer to the *S2D13515 Hardware Functional Specification*, document number X83A-A-001-xx.

The following figure shows the location of host bus connectors H3 and H4. H3 is a 0.1” x 0.1” 40-pin header (20x2) and H4 is a 0.1” x 0.1” 34-pin header (17 x 2).

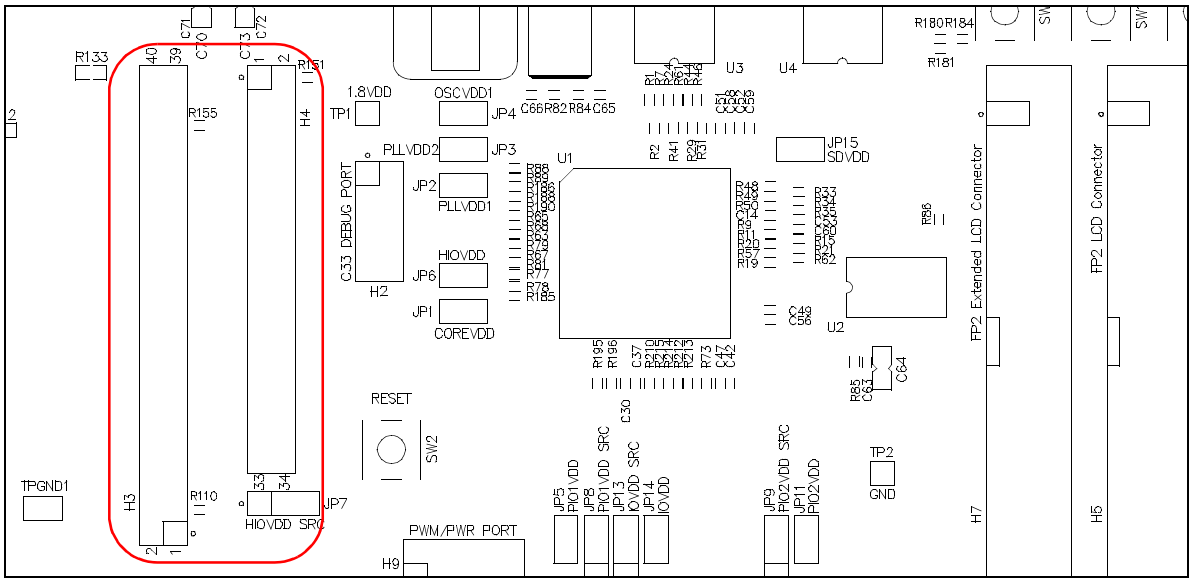

Figure 4-2: Host Bus Connector Location (H3 and H4)

For the pinout of connectors H3 and H4, see Section Chapter 6, “Schematic Diagrams” on page 29.

4.5.2 Connecting to the Epson S5U13U00P00C100 USB Adapter Board

The S5U13515P00C100 evaluation board is designed to connect to a S5U13U00P00C100 USB Adapter Board. The USB adapter board provides a simple connection to any computer via a USB 2.0 connection. The S5U13515P00C100 directly connects to the USB adapter board through connectors P1 and P2.

The USB adapter board also supplies the 3.3V power required by the S5U13515P00C100 evaluation board. HIOVDD should be configured for 3.3V and JP7 should be set to the 2-3 position.

When the S5U13515P00C100 is connected to the S5U13U00P00C100 USB Adapter board, there are 2 LEDs on the S5U13515P00C100 which provide a quick visual status of the USB adapter. LED1 blinks to indicate that the USB adapter board is active. LED2 turns on to indicate that the USB has been enumerated by the PC.

The following diagram shows the location of connectors P1 and P2. P1 and P2 are 2mm x 2mm, 40-pin headers (20 x 2) located on the underside of the board.

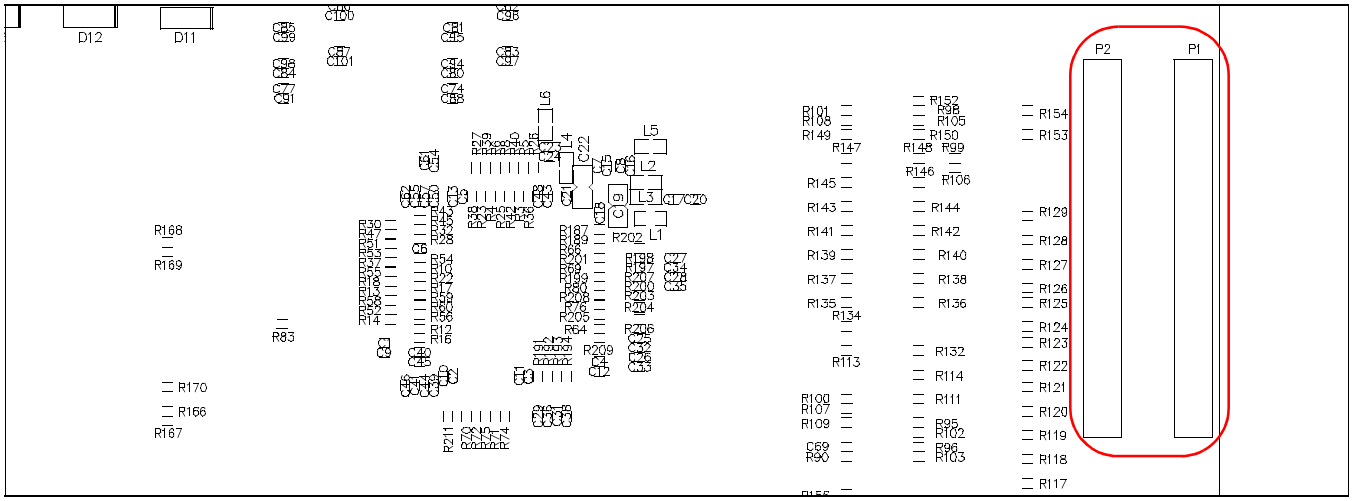

Figure 4-3: USB Adapter Connector Locations (P1 and P2)

For the pinout of connectors P1 and P2, see Section Chapter 6, “Schematic Diagrams” on page 29.

Note
A windows driver must be installed on the PC when the S5U13515P00C100 is used with the S5U13U00P00C100 USB Adapter Board. The S1D13xxxUSB driver is available at www.erd.epson.com.

4.6 LCD Interface

The LCD interface uses the FP1IO[23:0] and FP2IO[27:0] pins. All signals on these pins are available on connectors H5, H6, and H7.

Connectors H5, H6, and H7 are 0.1” x 0.1”, 40-pin headers (20 x 2). The following diagram shows the location of these connectors.

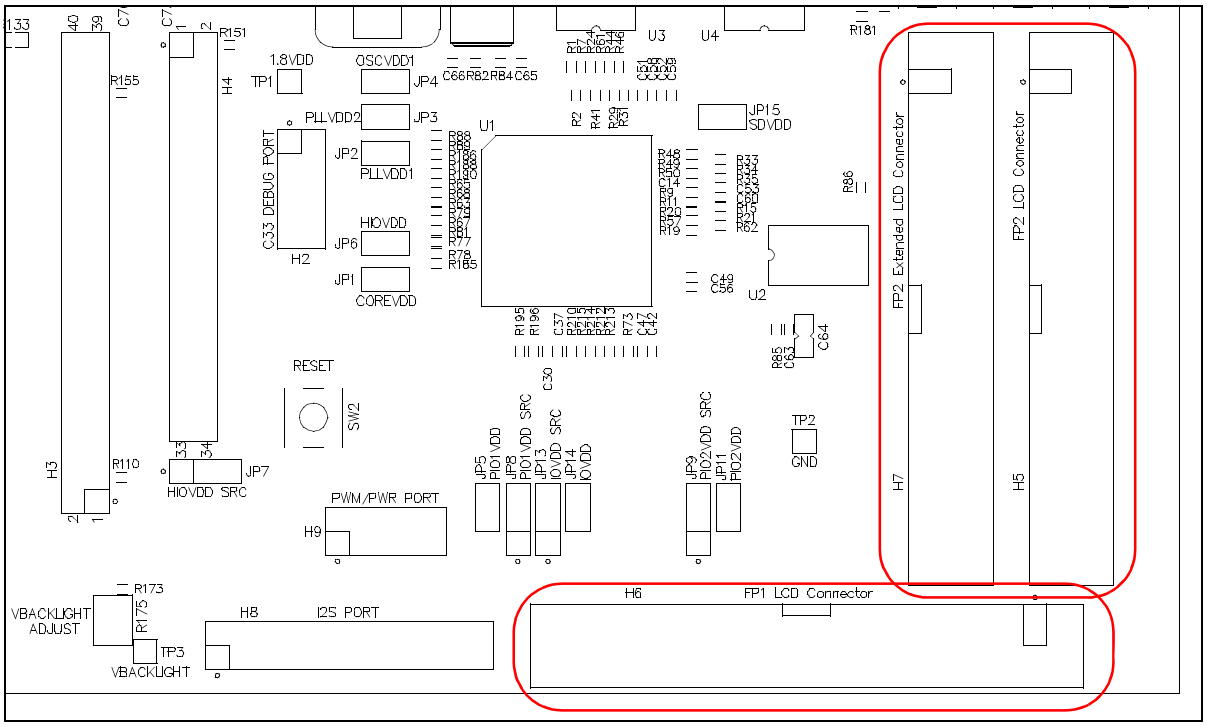

Figure 4-4: FP1IO and FP2IO Connectors Location (H5, H6, H7)

For the pinout of connectors H5, H6, and H7, see Section Chapter 6, “Schematic Diagrams” on page 29.

4.6.1 FP1IO Interface

The FP1IO interface signals have multiplexed functions. All FP1IO interface signals, except FP1IO18 and FP1IO19, are available on connector H6. FP1IO18 and FP1IO19 signals go through 0 ohm resistors and are available on connector H7.

The FP1IO interface can be configured as a LCD interface, 18-bit RGB input stream interface, or 8-bit YUV camera interface and keyboard interface. For S2D13515 FP1IO interface pin mapping, refer to the *S2D13515 Hardware Functional Specification*, document number X83A-A-001-xx.

4.6.2 FP2IO Interface

All FP2IO interface signals are available on connectors H5 and H7. For S2D13515 FP2IO interface pin mapping, refer to the *S2D13515 Hardware Functional Specification*, document number X83A-A-001-xx.

4.7 Camera / I2C Interface

The S2D13515 Display Controller has a Camera interface. All the camera interface signals are available on connector H10. To control the camera, the S2D13515 Display Controller has an I2C master interface. The SDA and SCL signals are pulled high to CM1VDD by 2.2 kΩ resistors and are available on connector H10. The reset signal provided on H10 is active low and is pulled to HIOVDD when inactive.

Connector H10 is a 0.1” x 0.1”, 20-pin header (10 x 2). The following figure shows the location of the connector H10.

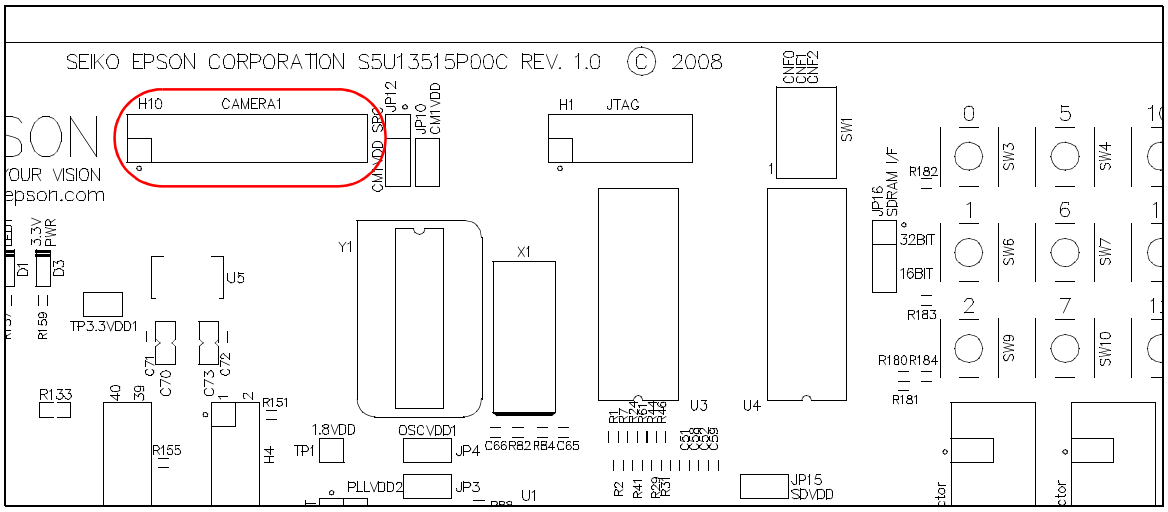

Figure 4-5: Camera Connector Location (H10)

For the pinout of connector H10, see Section Chapter 6, “Schematic Diagrams” on page 29.

4.8 Keypad Interface

Note
The keyboard is non-operational with the buttons SW3-SW11, mounted as they are on the board. In order to make the keyboard operational, the user must remove the buttons SW3-SW11 from the board and mount them back on the board, but rotated by 90 degrees or 270 degrees. The buttons will not match the footprint on the PCB, but this is how they must be mounted on the board.

The S2D13515 Display Controller can support up to a 5x5 matrix keypad, but the S5U13515P00C100 evaluation board includes only a 3x3 keypad. The keypad interface can be configured to use either the FPIO1 interface or Host interface pins. For S2D13515 pin mapping, refer to the *S2D13515 Hardware Functional Specification*, document number X83A-A-001-xx. The keypad interface is configured for either the FPIO1 interface or Host Interface pins using 0 ohm resistors.

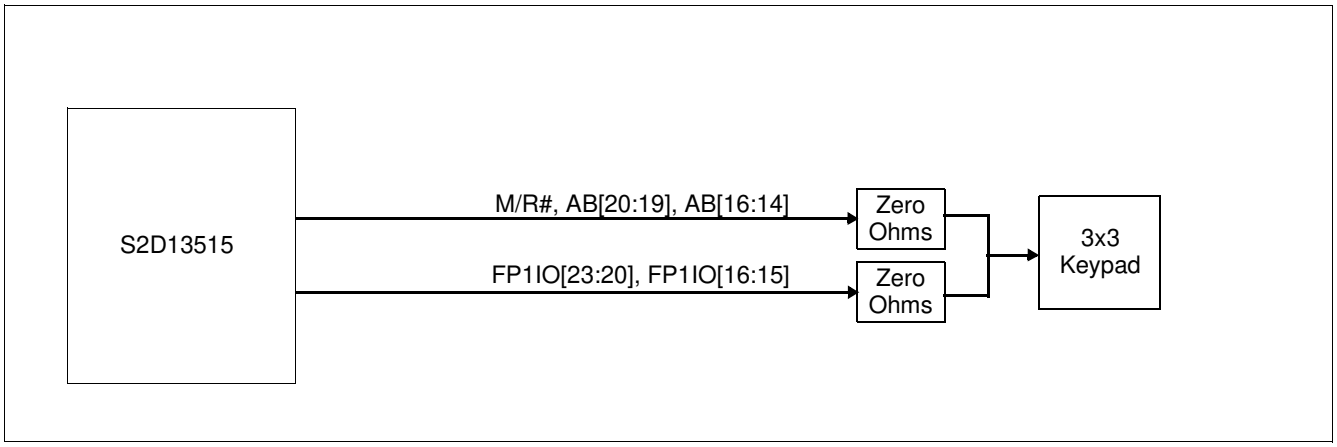

Figure 4-6: Keypad Interface Zero Ohm Resistor Overview Diagram

The keypad can be configured to connect to 1 of 2 source pins on the S2D13515. Depending of the configuration, the input lines must be pulled high to corresponding power supply. The source connection for the keypad is determined by populating the correct set of zero ohm resistors as described below.

Table 4-1: Keypad Zero Ohm Resistor Summary

Keypad Pin Function	Populate only 1 set of the zero ohm resistors below	
	Zero Ohm For FP1IO	Zero Ohm For Host Interface
KBR0	R191	R185
KBR1	R192	R186
KBR2	R193	R187
KBC0	R194	R188
KBC1	R195	R190
KBC2	R196	R189
Power (HIOVDD or PIO1VDD)	R181	R180

S5U13515P00C100 evaluation board comes configured with the keyboard interface from the Host Interface pins, so resistors R185 ~ R190 and R180 are populated and R191 ~ R196 and R181 are not populated.

4.9 I2S Interface

The S2D13515 Display Controller has an I2S Audio output interface. All of the I2S interface signals are available on connector H8. The I2C signals, available on the same connector, can be used to program an external I2S Audio DAC IC.

Connector H8 is a 0.1” x 0.1”, 24-pin header (12x2). The following figure shows the location of the connector H8.

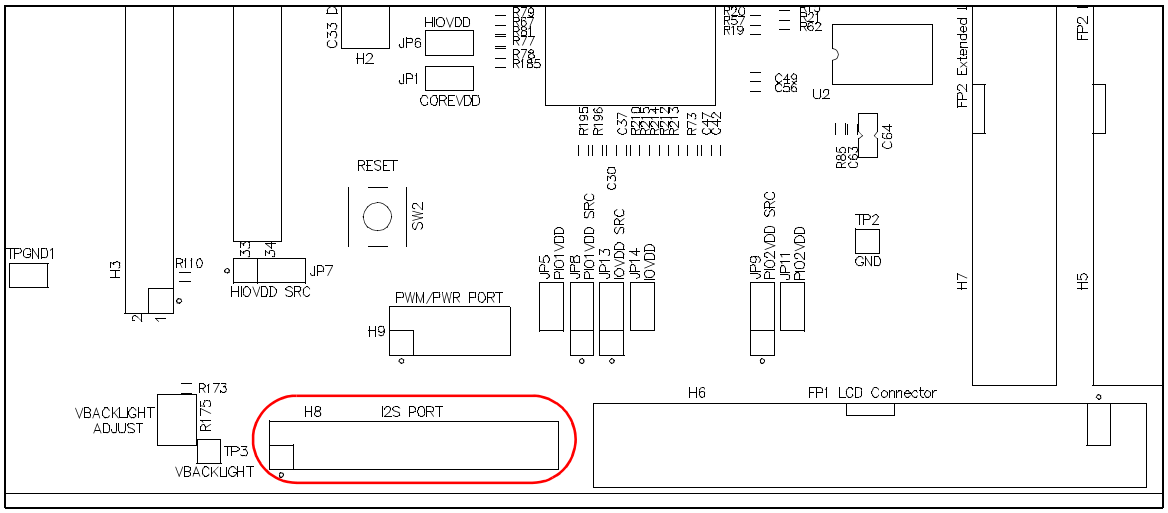

Figure 4-7: I2S Connector Location (H8)

For the pinout of connector H8, see Section Chapter 6, “Schematic Diagrams” on page 29.

4.10 PWM Connector

The S2D13515 Display Controller has two PWM outputs which are available on connector H9. The other pins on connector H9 are used to connect the external power supplies to CM1VDD, IOVDD, PIO1VDD, and PIO2VDD, if a voltage level different than 3.3V is required. Note that connector H9 is not populated on the S5U13515P00C100 evaluation board.

Connector H9 is a 0.1” x 0.1”, 10-pin header (5x2). The following figure shows the location of the connector H9.

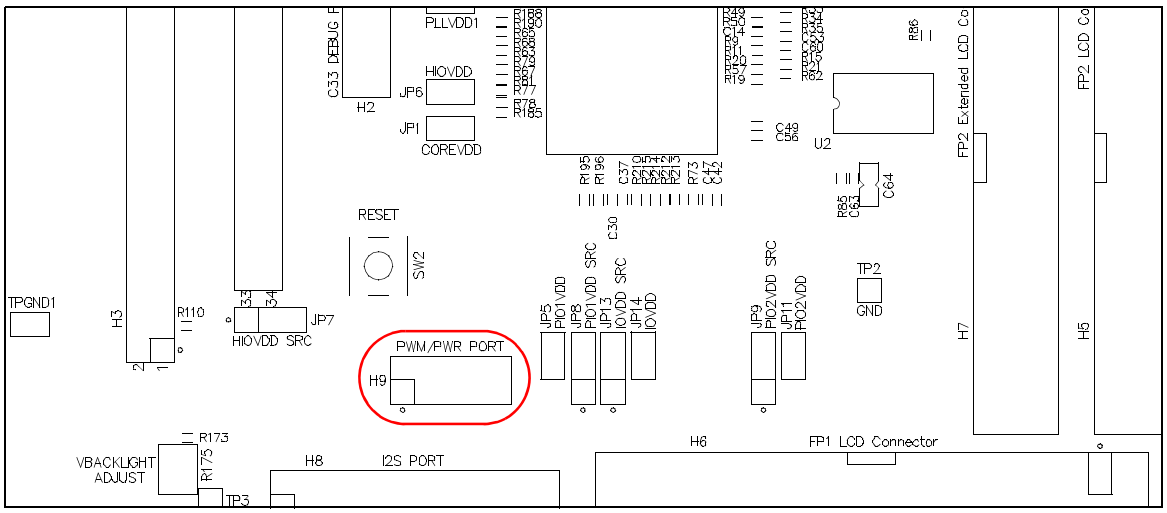

Figure 4-8: PWM Connector Location (H9)

For the pinout of connector H9, see Section Chapter 6, “Schematic Diagrams” on page 29.

4.11 C33 Debugger Port

The S2D13515 contains an embedded C33 microprocessor core. The debug monitor interface is available on connector H2 for firmware debugging using C33 Debugger. In order to use connector H2, zero ohm resistors must be configured depending on the desired S2D13515 configuration.

The C33 debugger function can be sourced from 2 sets of the host interface pins or from a set of FP2IO pins.

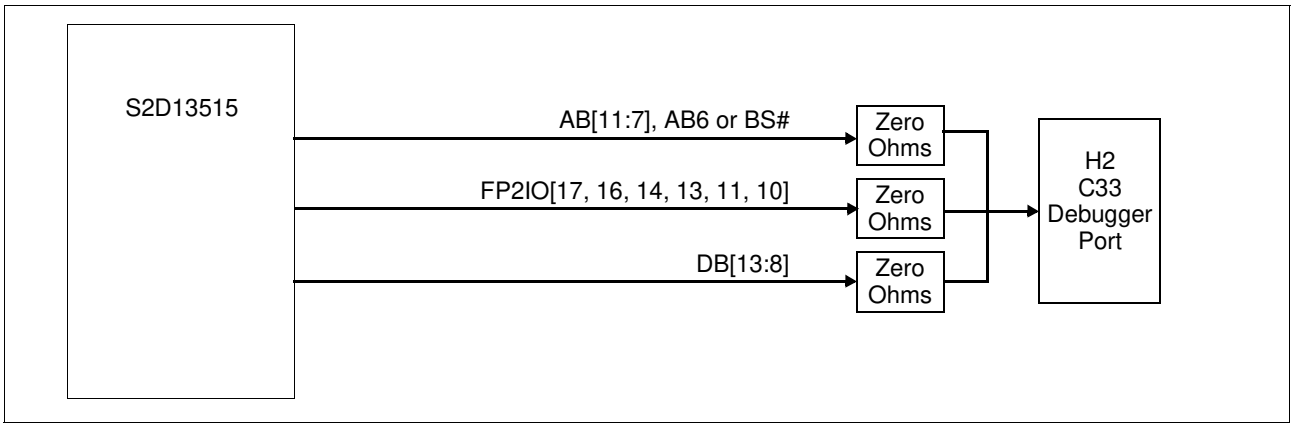

Figure 4-9: C33 Debugger Zero Ohm Resistor Overview Diagram

The connection to the C33 Debugger port is determined by populating the correct set of zero ohm resistors as described below.

Table 4-2: C33 Debugger Port H7 Zero Ohm Selection

C33 Pin Function	Populate only 1 set of the zero ohm resistors below		
	C33 Debugger port from FP2IO pins	**C33 Debugger port from AB[11:7], AB6 or BS# pins**	**C33 Debugger port from DB[13:8] pins**
PEDST0	R74 populated R210 not populated	R65 populated R202 not populated	R80 populated R208 not populated
PEDST1	R73 populated R211 not populated	R66 populated R201 not populated	R79 populated R207 not populated
PEDST2	R72 populated R212 not populated	R67 populated R200 not populated	R78 populated R206 not populated
PEDCLK	R70 populated R213 not populated	R69 populated R199 not populated	R76 populated R205 not populated
PEDSIO	R71 populated R215 not populated	R68 populated R198 not populated	R77 populated R204 not populated
PEDCPCO	R75 populated R214 not populated	R63 populated (from AB6) R64, R197 not populated	R81 populated R203 not populated
		R64 populated (from BS#) R63, R209 not populated	

S5U13515P00C100 board comes configured for the C33 Debugger port from the Host Interface AB[11:6] pins, so resistors R63, R65 ~ R69 are populated and R197 ~ R202 are not populated, R203 ~ R215 are populated and R64, R70 ~ R81 are not populated.

Connector H2 is a 0.1” x 0.1”, 10-pin header (5x2). The following figure shows the location of the connector H2.

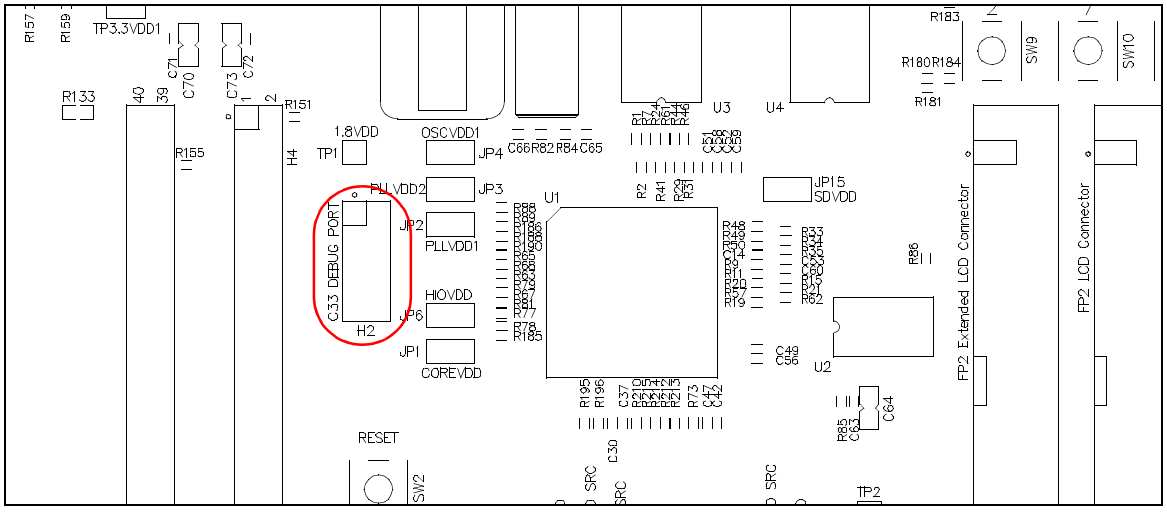

Figure 4-10: C33 Debugger Connector Location (H2)

For the pinout of connector H2, see Section Chapter 6, “Schematic Diagrams” on page 29.

4.12 JTAG Interface

The S2D13515 Display Controller has a JTAG interface. All the JTAG signals are available on connector H1. Note that connector H1 is not populated on the S5U13515P00C100 evaluation board.

Connector H1 is a 0.1” x 0.1”, 12-pin header (6x2). The following figure shows the location of the connector H1.

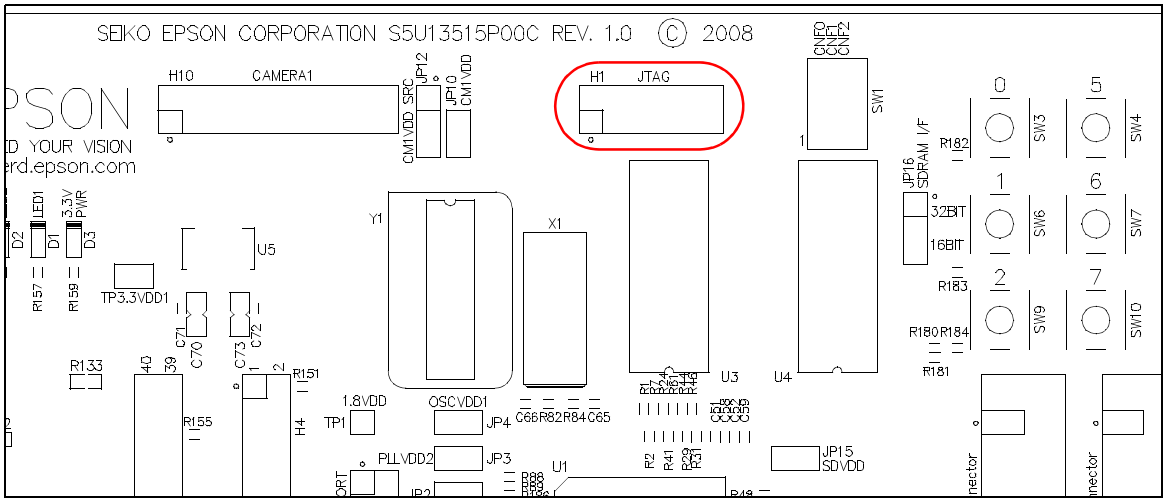

Figure 4-11: JTAG Connector Location (H1)

For the pinout of connector H1, see Section Chapter 6, “Schematic Diagrams” on page 29.