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S1D13746 TV-Out Mobile Graphics Engine

S5U13746P00C100 Evaluation Board User Manual

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NOTICE

Table of Contents

1 Introduction 5
2 Features 6
3 Installation and Configuration 7
3.1 Configuration DIP Switch 7
3.2 Configuration Jumpers 8
4 Technical Description 12
4.1 Power 12
4.1.1 Power Requirements 12
4.1.2 Voltage Regulators 12
4.1.3 S1D13746 Power 12
4.2 Clocks 13
4.3 Reset 13
4.4 Power Save 13
4.5 Host Interface 14
4.5.1 Direct Host Bus Interface Support 14
4.5.2 Connecting to the Epson S5U13U00P00C100 USB Adapter Board 15
4.6 TV Output 16
4.7 GPIO Connections 18
5 Parts List 19
6 Schematic Diagrams 21
7 S5U13746P00C100 Board Layout 24
8 References 26
8.1 Documents 26
8.2 Document Sources 26
9 Technical Support 27
9.1 EPSON Display Controllers (S1D13746) 27
9.2 Ordering Information 27

1 Introduction

This manual describes the setup and operation of the S5U13746P00C100 Evaluation Board. The evaluation board is designed as an evaluation platform for the S1D13746 TV-Out Mobile Graphics Engine.

The S5U13746P00C100 evaluation board can be used with many other native platforms via the host connectors which provide the appropriate signals to support a variety of CPUs. The S5U13746P00C100 evaluation board can also connect to the S5U13U00P00C100 USB Adapter board so that it can be used with a laptop or desktop computer, via USB 2.0.

This user manual is updated as appropriate. Please check the Epson Research and Development Website at www.erd.epson.com for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

2 Features

The S5U13746P00C100 Evaluation Board includes the following features:

- 100-pin PFBGA S1D13746 TV-Out Mobile Graphics Engine
- Headers for connecting to various Host Bus Interfaces or a Parallel RGB Interface
- Headers for connecting to the S5U13U00P00C100 USB Adapter board
- Output connectors for analog composite video and S-video
- Header for GPIO pins
- On-board 27MHz oscillator
- 14-pin DIP socket (if a clock different than 27MHz must be used)
- 3.3V input power
- On-board voltage regulators

3 Installation and Configuration

The S5U13746P00C100 evaluation board incorporates a DIP switch, jumpers, and 0 ohm resistors which allow it to be used with a variety of different configurations.

3.1 Configuration DIP Switch

The S1D13746 has configuration inputs (CNF[3:0]) and a 4-position DIP switch (SW1) which is used to configure the S1D13746 for any of the Host Bus Interfaces. The following figure shows the location of DIP switch SW1 on the S5U13746P00C100.

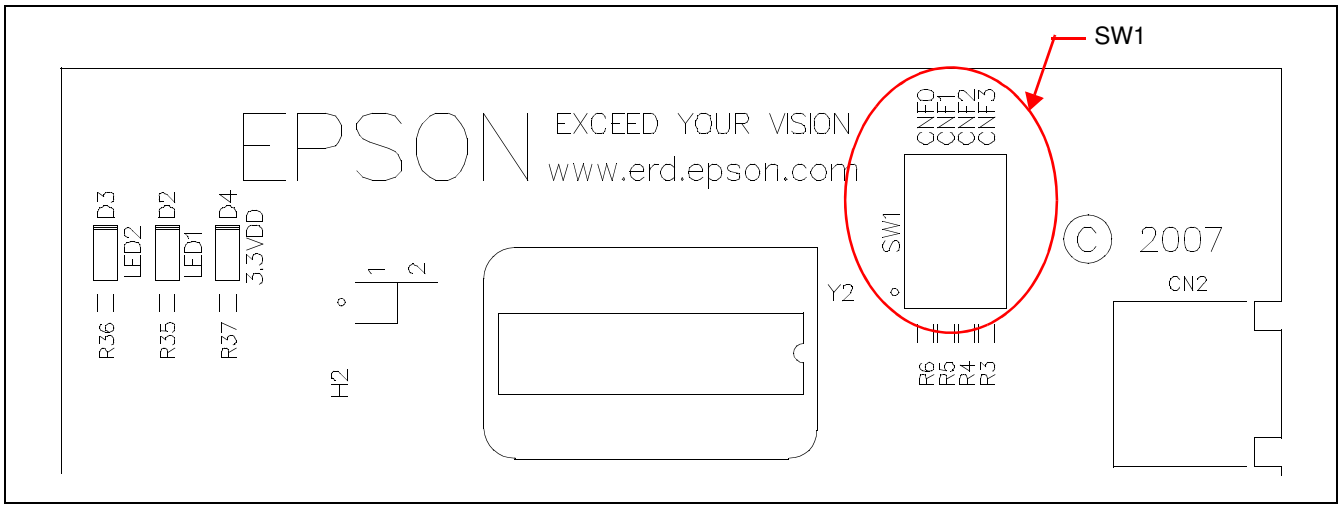

Figure 3-1: Configuration DIP Switch (SW1) Location

All S1D13746 configuration inputs (CNF[3:0]) are fully configurable using DIP switch SW1 as described below.

Table 3-1: Summary of Power-On/Reset Options

SDU13746P00C100 SW1-[4:1] Config	S1D13746 CNF[3:0] Config	Power-On/Reset State	
		1 (ON)	0 (OFF)
SW1-[2:1]	CNF[1:0]	00b	3-Wire Serial Host Interface with Parallel RGB Interface
		01b	8-Bit Intel 80
		10b	SPI Host Interface with Parallel RGB Interface
		11b	16-Bit Intel 80
SW1-[3]	CNF2	Crystal used as input clock	Oscillator used as input clock
SW1-[4]	CNF3	Reset Filter = 5us	Reset Filter = 43ns

= Required settings when using S5U13U00P00C100 USB Adapter board (SW1-[4:1] = 1011b)

3.2 Configuration Jumpers

The S5U13746P00C100 has 7 jumpers which configure various board settings. The jumper positions for each function are shown below.

Jumper	Function	Position 1-2	Position 2-3	No Jumper
JP1	COREVDD	Normal	—	COREVDD current measurement
JP2	PLLVDD	Normal	—	PLLVDD current measurement
JP3	DACVCC	Normal	—	DACVCC current measurement
JP4	IOVDD	Normal	—	IOVDD current measurement
JP5	SIOVDD	Normal	—	SIOVDD current measurement
JP6	IOVDD Source	H2 connector, pin 32	3.3VDD	—
JP7	SIOVDD Source	H3 connector, pin 4	3.3VDD	—

= Required settings when using S5U13U00P00C100 USB Adapter board

JP1-JP5 - S1D13746 Power Supplies

JP1-JP5 can be used to measure the current consumption of each S1D13746 power supply. When the jumper is at position 1-2, normal operation is selected.
When no jumper is installed, the current consumption for each power supply can be measured by connecting an ammeter to pins 1 and 2 of the jumper.

The jumper associated to each power supply is as follows:

JP1 for COREVDD
JP2 for PLLVDD
JP3 for DACVCC
JP4 for IOVDD
JP5 for SIOVDD

Note

Because the crystal input of the S1D13746 is not used on this board, there is no provision to measure OSCVDD current consumption.

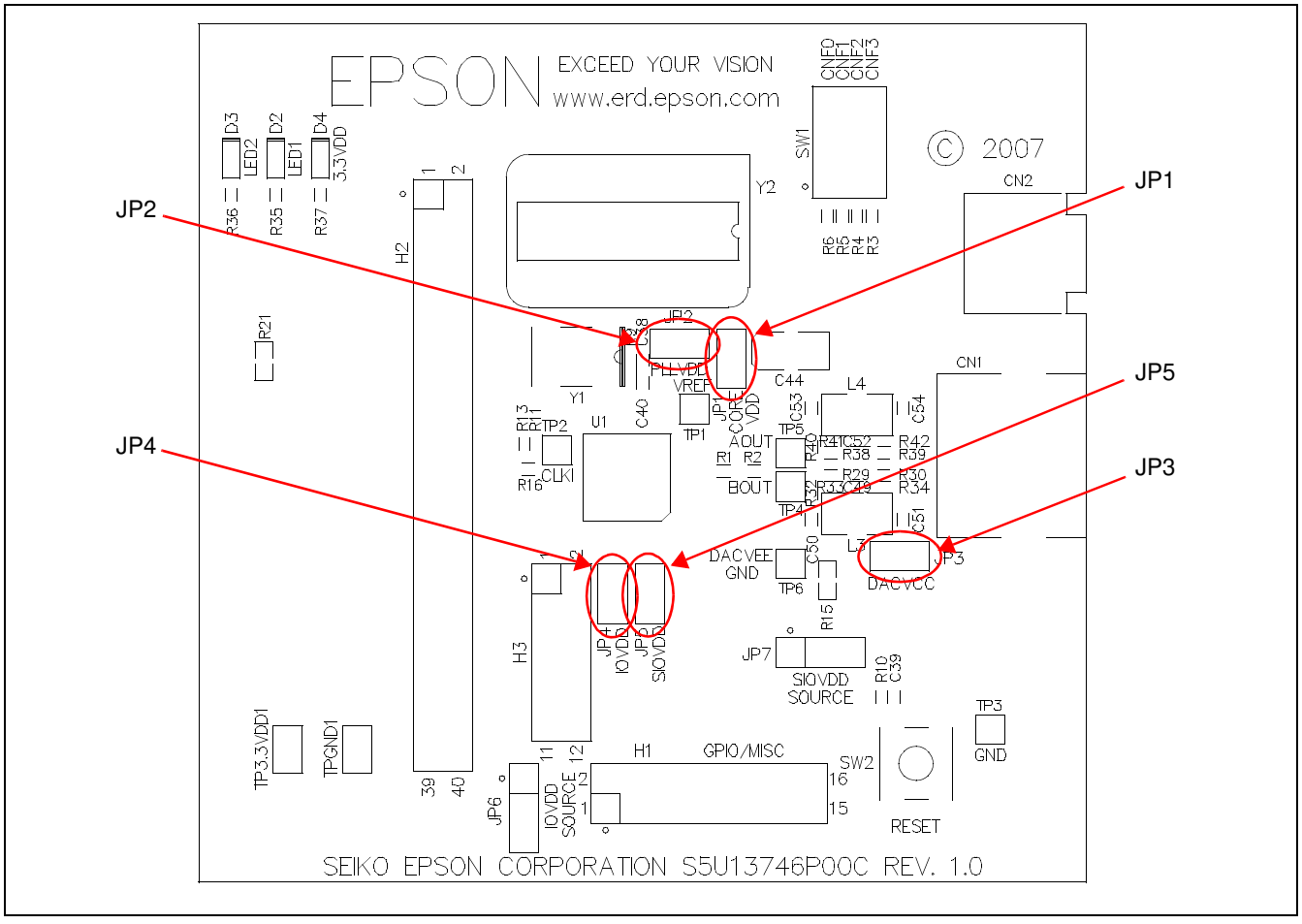

Figure 3-2: Configuration Jumper Locations (JP1-JP5)

JP6 - IOVDD Source

JP6 is used to select the source for the IOVDD supply voltage.
When the jumper is at position 1-2, the IOVDD voltage must be provided to H2 connector, pin 32.
When the jumper is at position 2-3, the IOVDD voltage is provided by the 3.3V power supply of the board.

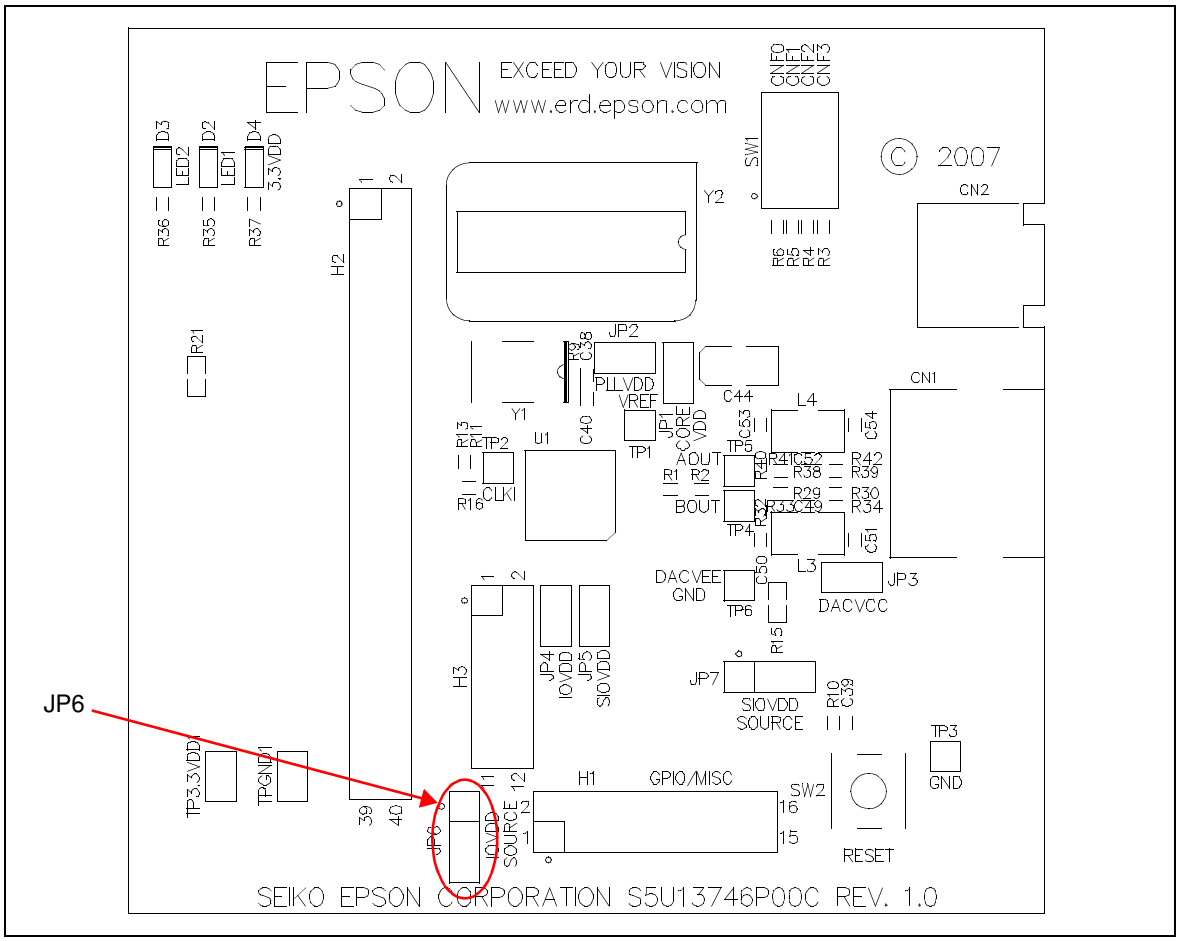

Figure 3-3: Configuration Jumper Location (JP6)

JP7 - SIOVDD Source

JP7 is used to select the source for the SIOVDD supply voltage.
When the jumper is at position 1-2, the SIOVDD voltage must be provided to H3 connector, pin 4.
When the jumper is at position 2-3, the SIOVDD voltage is provided by the 3.3V power supply of the board.

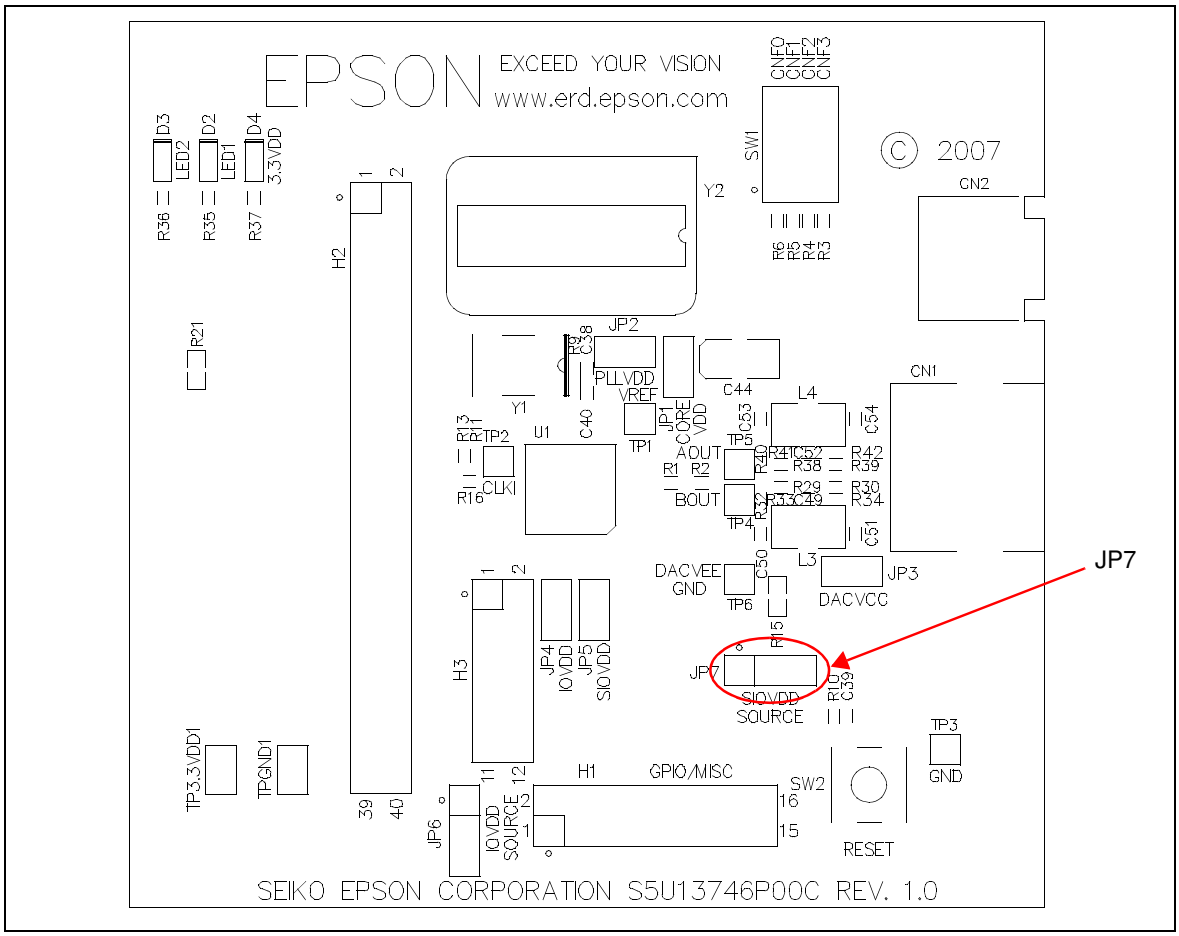

Figure 3-4: Configuration Jumper Location (JP7)

4 Technical Description

4.1 Power

4.1.1 Power Requirements

The S5U13746P00C100 evaluation board requires an external regulated power supply (3.3V / 0.5A). The power is supplied to the evaluation board through pin 5 of the P2 header, or pin 2 of the H3 header.

The green LED '3.3V Power' is turned on when 3.3V power is applied to the board.

4.1.2 Voltage Regulators

The S5U13746P00C100 evaluation board has on-board linear regulators to provide the 1.5V power and 3.0V power required by the S1D13746 TV-Out Mobile Graphics Engine.

4.1.3 S1D13746 Power

The S1D13746 TV Out Mobile Graphics Engine requires 1.5V, 3.0V and 1.65-3.6V power supplies.

1.5V power is provided by the on-board linear voltage regulator. It is used for COREVDD and PLLVDD.

3.0V power is provided by the on-board linear voltage regulator. It is used for DACVCC.

3.3V power is provided by the external power supply. It is used for OSCVDD (even if the internal oscillator is not used, power must be provided to the OSCVDD pin).

IOVDD can be in the range 1.65-3.6V. IOVDD is connected to 3.3V when JP6 is in 2-3 position. If it is desired to have a different voltage for IOVDD, set JP6 in the 1-2 position and connect the desired supply to pin 32 of connector H2.

Note
If IOVDD voltage is less than 3.0V, an oscillator working at the selected IOVDD voltage must be used.

SIOVDD can be in the range 1.65-3.6V. SIOVDD is connected to 3.3V when JP7 is in 2-3 position. If it is desired to have a different voltage for SIOVDD, set JP7 in the 1-2 position and connect the desired supply to pin 4 of connector H3.

OSCVDD is connected directly to 3.3V.

4.2 Clocks

The clock for the S1D13746 chip is provided by a 27MHz oscillator.

The board has the footprint for a second oscillator, Y2, with a DIP14 footprint. This can be used if a different clock frequency must be used for the S1D13746 chip.

To use the Y2 oscillator, an oscillator must be populated in the Y2 footprint. Then remove R11 (33 ohm resistor, size 0402) to cut the output of Y1 and populate R13 with a 33 ohm resistor, size 0402, to connect the output of Y2 to the CLKI input of the S1D13746 chip.

Note
If the board is configured for IOVDD voltage below 3.0V, an oscillator working at the selected IOVDD voltage must be used as Y2. The on-board 27MHz oscillator is not specified to work below a 3.0V supply voltage.

The S1D13746 chip can use a crystal to provide the clock, but this feature is not used on the board.

The S1D13746 chip can output the input clock on the CLKOUT pin depending on the state of the CLKOUTEN input. Both these signals are available on the H1 connector: CLKOUT on pin 1 of H1 connector and CLKOUTEN on pin 4 of H1 connector. On the board the CLKOUTEN pin is pulled down which disables the CLKOUT signal.

4.3 Reset

The S1D13746 chip on the S5U13746P00C100 evaluation board can be reset using a push-button, or via an active low reset signal from the host development platform (pin 10 on the H3 connector).

4.4 Power Save

The S1D13746 chip has an input called PWRSVE that will enable (when high) or disable (when low) the power save mode. This signal is available on pin 10 of the H1 connector. On the board the PWRSVE pin is pulled down which means power save mode is controlled only by the S1D13746 register setting.

4.5 Host Interface

4.5.1 Direct Host Bus Interface Support

The S1D13746 TV-Out Mobile Graphics Engine supports several host bus interfaces. For detailed S1D13746 pin mapping, refer to the *S1D13746 Hardware Functional Specification*, document number X74B-A-001-xx.

All S1D13746 host interface pins are available on connectors H2 and H3 which allow the S5U13746P00C100 evaluation board to be connected to a variety of development platforms.

The S1D13746 supports the Parallel RGB interface. All the signals used by the Parallel RGB interface are grouped on the H2 connector. All the Parallel RGB interface signals must match the IOVDD voltage level of the S1D13746 chip.

When the S1D13746 is configured for the Parallel RGB interface, it is controlled by the host through a serial interface (3-wire or SPI). All the host serial interface signals are available on the H3 connector. The serial interface signals must match the SIOVDD voltage level of the S1D13746 chip.

The following diagram shows the location of the host bus connectors H2 and H3. H2 is a 0.1x0.1" 40-pin header (20x2) and H3 is a 0.1x0.1" 12-pin header (6x2).

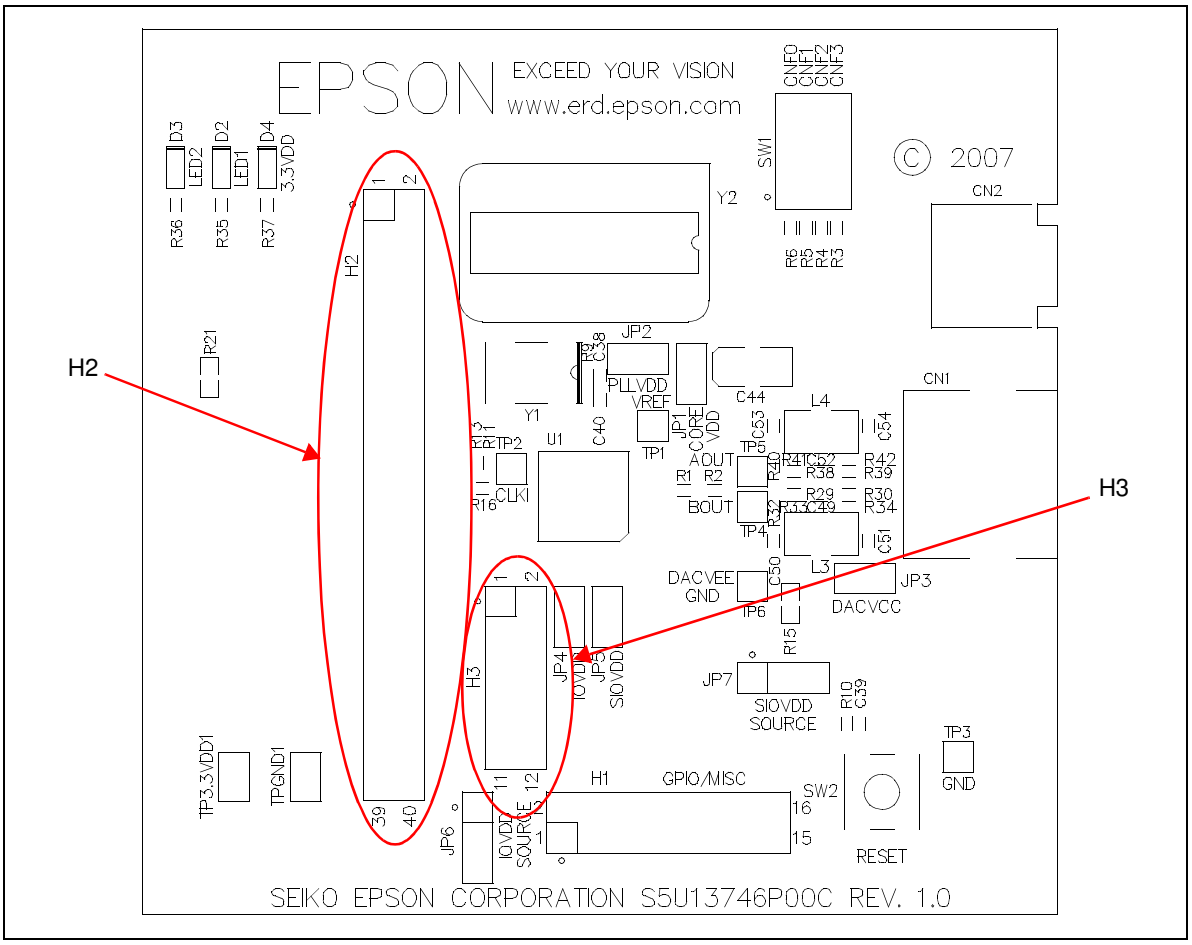

Figure 4-1: Host Bus Connector Locations (H2 and H3)

For the pinout of connectors H2 and H3, see "Schematic Diagrams" on page 21.

4.5.2 Connecting to the Epson S5U13U00P00C100 USB Adapter Board

The S5U13746P00C100 evaluation board is designed to connect to a S5U13U00P00C100 USB Adapter Board. The USB adapter board provides a simple connection to any computer via a USB 2.0 connection. The S5U13746P00C100 directly connects to the adapter board through connectors P1 and P2.

The USB adapter board also supplies the 3.3V power required by the S5U13746P00C100. IOVDD and SIOVDD should be selected to be 3.3V and both JP6 and JP7 should be in the 2-3 position.

4.6 TV Output

The S1D13746 chip can output a S-Video TV signal or a Composite Video signal. The S5U13746P00C100 evaluation board includes a standard TV composite video connector and a standard S-Video connector.

The S-Video output use 2 separate outputs for the luminance and chrominance signals. The TV image quality is much higher when using S-Video output. The composite output uses only one output for the complete TV signal.

The S5U13746P00C100 board design includes an external TV output filter for each of the 2 analog outputs, as described in the *S1D13746 Hardware Functional Specification*, document number X74B-A-001-xx.

The filter for the luminance or composite video signals consists of C52, C53, C54, and L6. To bypass the filter, remove resistors R41 and R42 (0 ohm resistors) and populate resistors R38 and R39 with 0 ohm resistors, size 0402. For circuit configuration, refer to “Schematic Diagrams” on page 21.

The filter for the chrominance signal consists of C49, C50, C51, and L5. To bypass the filter, remove resistors R33 and R34 (0 ohm resistors) and populate resistors R29 and R30 with 0 ohm resistors, size 0402. For circuit configuration, refer to “Schematic Diagrams” on page 21.

By default, the S1D13746 DAC is configured to use internal VREF. For further information, refer to the *S1D13746 Hardware Functional Specification*, document number X74A-A-001-xx. If an external VREF must be used, then a 1.23V reference must be provided to TP1 (the VREF test point on the board).

The following diagram shows the location of the TV out connectors.

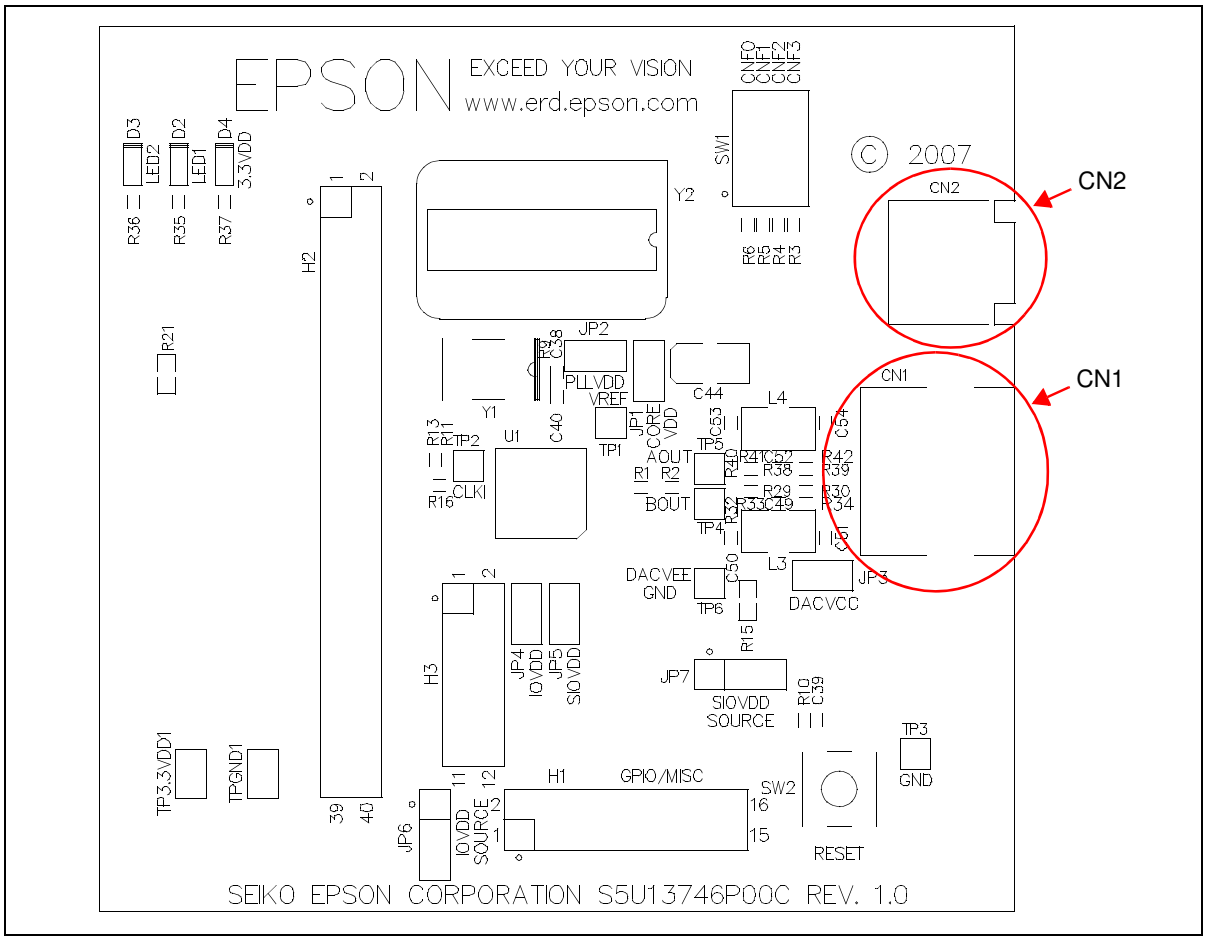

Figure 4-2: TV Out Connectors Locations (CN1, CN2)

4.7 GPIO Connections

The S1D13746 chip has 8 GPIO pins. All the GPIO pins are routed to the H1 connector. However, the H1 connector is not populated on the S5U13746P00C100 evaluation board.

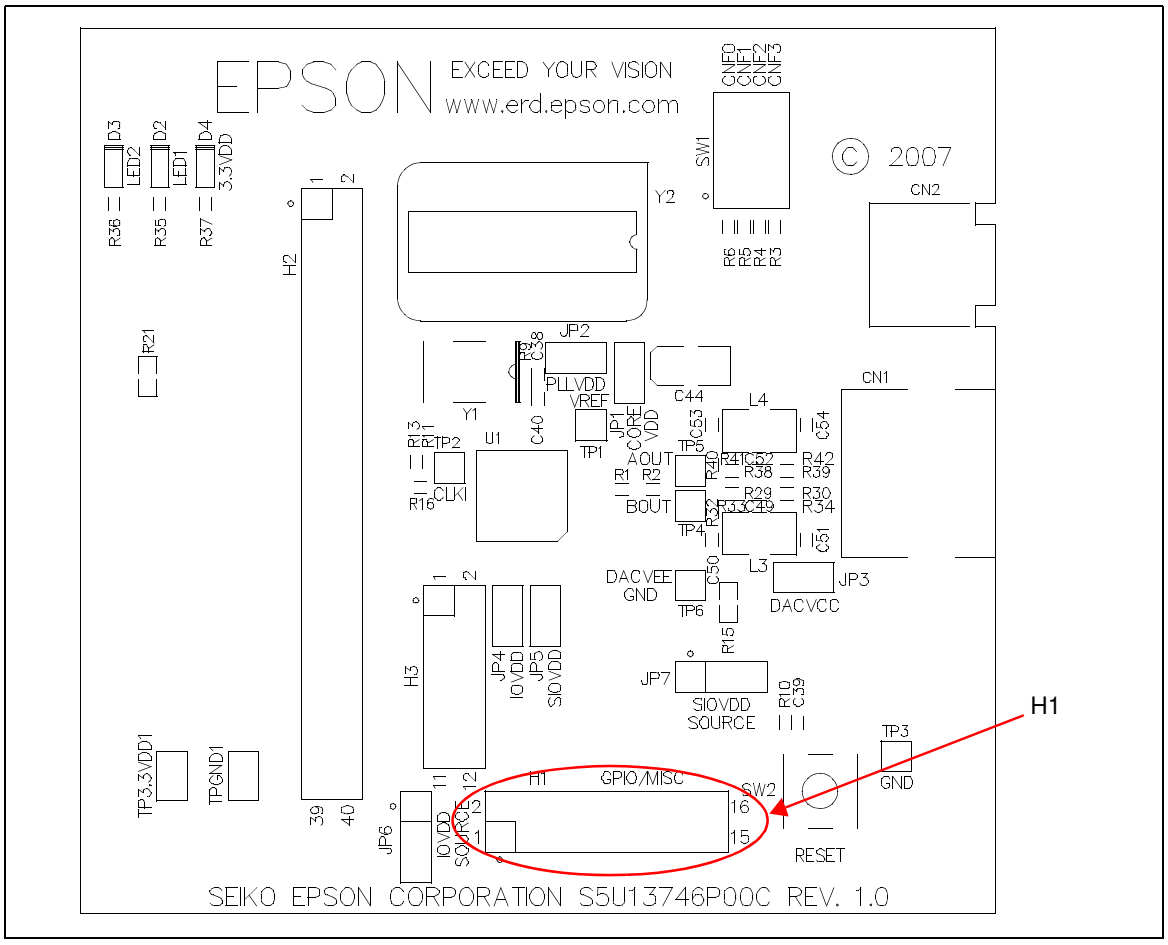

Figure 4-3: H1 Connector Location

5 Parts List

Table 5-1: Parts List

Item	Quantity	Reference	Part	PCB Footprint	Notes
1	1	CN1	M-DIN_4-R		CUI Inc. MD-40SM CONN MINI-DIN 4 PIN FEMALE PCB
2	1	CN2	VIDEO		CUI Inc. RCJ-044 CONN RCA JACK R/A YELLOW PCB
3	22	C1,C2,C3,C4,C5,C12, C13,C14,C15,C16, C17,C24,C25,C26, C27,C28,C30,C32, C38,C41,C42,C43	0.1uF	C0402	Yageo America 04022F104Z7B20D
4	1	C6	1nF	C0402	Yageo America 04022R102K9B20D
5	2	C7,C46	10uF	C0805	Panasonic - ECG ECJ-CV50J106M
6	12	C8,C9,C10,C11,C29, C31,C33,C34,C35, C36,C37,C39	0.01uF	C0402	Yageo America 0402ZRY5V7BB103
7	6	C18,C19,C20,C21, C22,C23	22uF		Rohm TCA0J226M8R CAP TANT 22UF 6.3V 20% SMD
8	2	C40,C45	0.01uF	C0402	Kemet C0402C103K4RACTU
9	1	C44	100uF 4V T	C3528	Kemet T494B107M004AS
10	1	C47	1uF	C0805	Murata Electronics GRM21BR71H105KA12L
11	1	C48	0.01uF	C0603	TDK C1608C0G1E103J
12	2	C49,C52	33pF	C0402	Panasonic-ECG ECJ-0EC1H330J
13	2	C50,C53	100pF	C0402	Murata Electronics GRM1555C1H101JZ01D
14	2	C51,C54	270pF	C0402	Murata Electronics GRM155R71H271KA01D
15	2	D1,D5	BAT54S	SOT-23	ON Semiconductor BAT54SLT1G DIODE SCHOTTKY DUAL 30V SOT23
16	1	D4	3.3V Power	LED0603	Panasonic - SSG LNJ308G8LRA LED GREEN SS TYPE LOW CUR SMD
17	0	H1	HEADER 8X2		
18	1	H2	HEADER 20X2		Samtec TSW-120-05-G-D
19	1	H3	HEADER 6X2		Samtec TSW-106-05-G-D
20	1	JP1	COREVDD	SIP2	CONN HEADER VERT 2POS .100 TIN or GENERIC
21	1	JP2	PLLVDD	SIP2	CONN HEADER VERT 2POS .100 TIN or GENERIC
22	1	JP3	DACVCC	SIP2	CONN HEADER VERT 2POS .100 TIN or GENERIC
23	1	JP4	IOVDD	SIP2	CONN HEADER VERT 2POS .100 TIN or GENERIC
24	1	JP5	SIOVDD	SIP2	CONN HEADER VERT 2POS .100 TIN or GENERIC
25	1	JP6	IOVDD SOURCE	SIP3	CONN HEADER VERT 3POS .100 TIN or GENERIC
26	1	JP7	SIOVDD SOURCE	SIP3	CONN HEADER VERT 3POS .100 TIN or GENERIC
27	2	L1,L2	Ferrite	R0603	Steward HZ0603B751R-10 FERRITE 200MA 938 OHMS 0603 SMD
28	2	L3,L4	1.8uH	L1210	Epcos B82422A1182K100 INDUCTOR 1.8UH 290MA 1210 10%

Table 5-1: Parts List

Item	Quantity	Reference	Part	PCB Footprint	Notes
29	2	P1,P2	HEADER_20X2	HDR2X20/2MM	3M 151240-8422-RB
30	2	R1,R10	1.5k 1%	R0402	
31	1	R2	560 1%	R0402	
32	4	R3,R4,R5,R6	10k	R0402	
33	11	R9,R14,R25,R26,R27, R28,R31,R33,R34, R41,R42	0	R0402	
34	1	R11	33 1%	R0402	
35	6	R12,R13,R29,R30, R38,R39	NP	R0402	
36	3	R15,R21,R24	0	R0603	
37	7	R16,R17,R18,R19, R20,R22,R23	47k	R0402	
38	2	R32,R40	75 1%	R0402	
39	1	R37	270 1%	R0402	
40	7	SH1,SH2,SH3,SH4, SH5,SH6,SH7	.100 in. Jumper Shunt	Not Applicable	Sullins Electronics Corp. STC02SYAN JUMPER SHORTING TIN
41	1	SW1	SW4_DIPSW4	DIPSW4	CTS Corp 218-4LPST SWITCH DIP HALF PITCH 4POS
42	1	SW2	SW TACT-SPST	SW_EVQQW	ITT Industries KSC241GLFS SWITCH TACT SILVER PLT GULLWING
43	2	TPGND1,TP3.3VDD1	TP_SMT	TP_1206	Keystone 5015 PC TEST POINT MINIATURE SMT
44	6	TP1,TP2,TP3,TP4, TP5,TP6	T POINT F	SIP1	
45	1	U1	S1D13746PFBGA 100	PFBGA100	
46	1	U2	TPS76915DBVT	SOT23-5	Texas Instruments TPS76915DBVT IC 1.5V 100MA LDO REG SOT-23-5
47	1	U3	LP3985	SOT23-5	National Semiconductor LP3985IM5-3.0/NOPB
48	1	Y1	27M OSC		Connor-Winfield CWX813-27.0M OSC 27MHz 3.3V +/-25ppm SMD
49	0	Y2	14-Pin DIP		AMP 2-641609-1

6 Schematic Diagrams

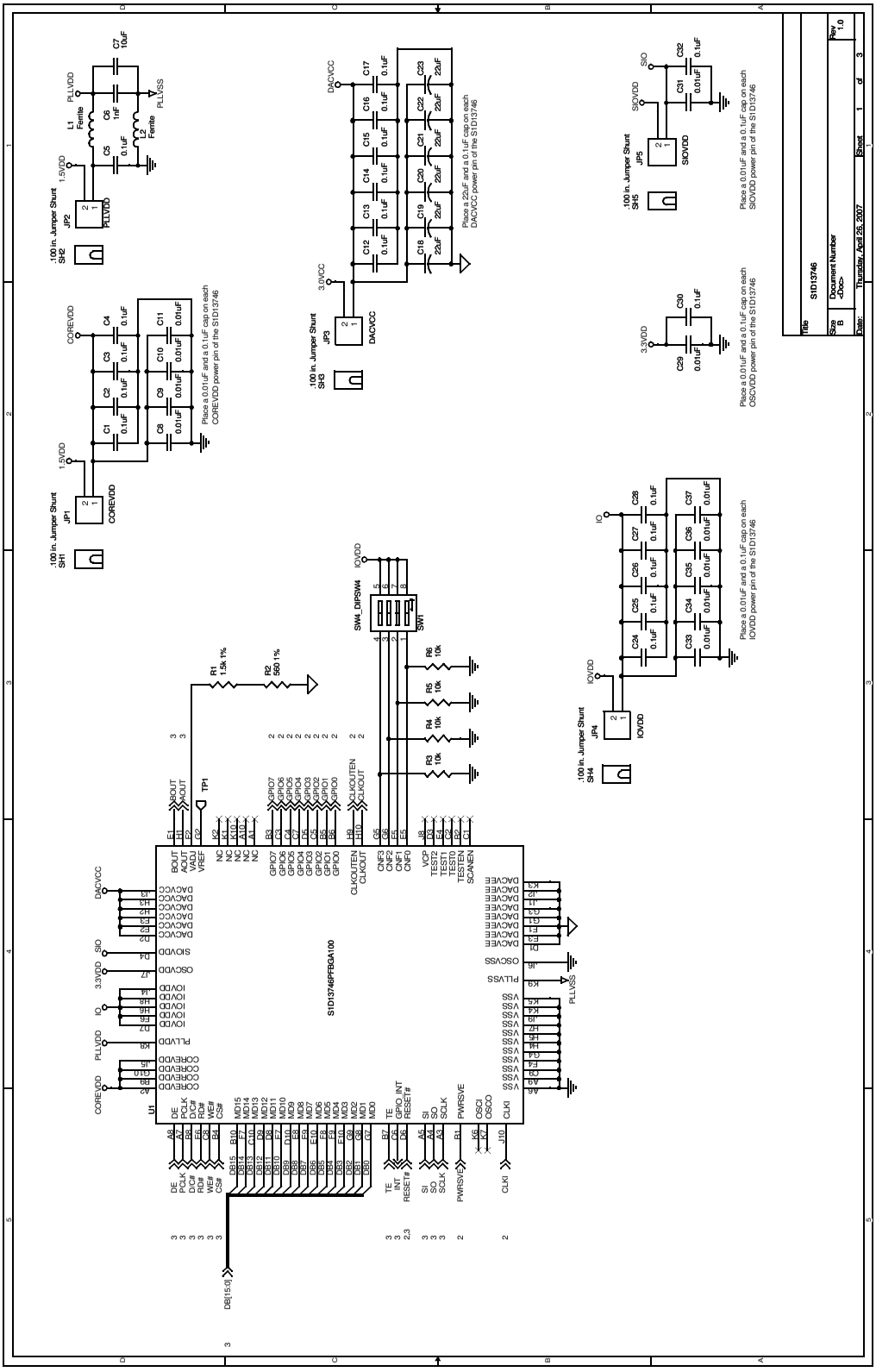

Figure 6-1: S5U13746P00C100 Schematics (1 of 3)

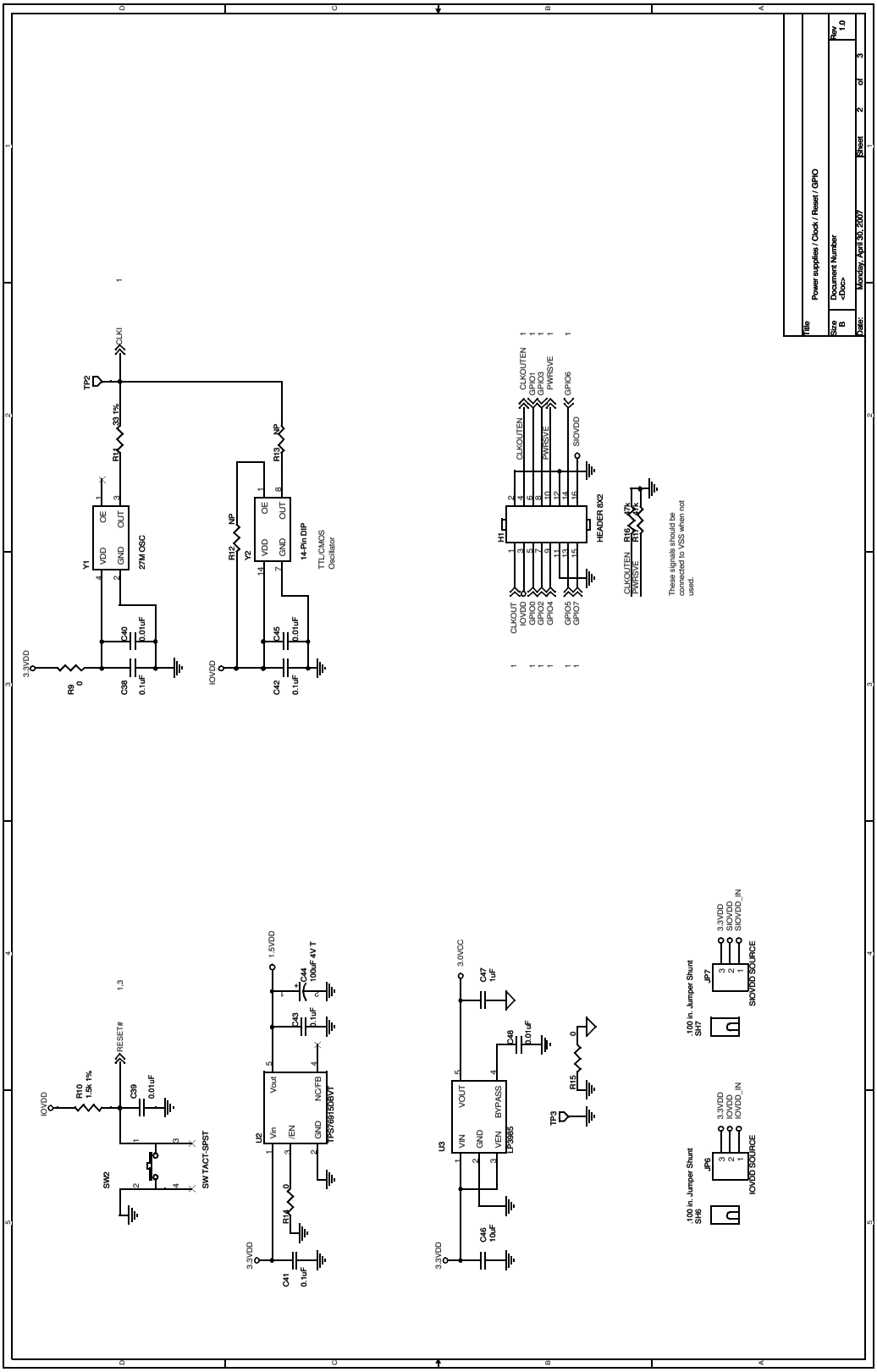

Figure 6-2: S5U13746P00C100 Schematics (2 of 3)

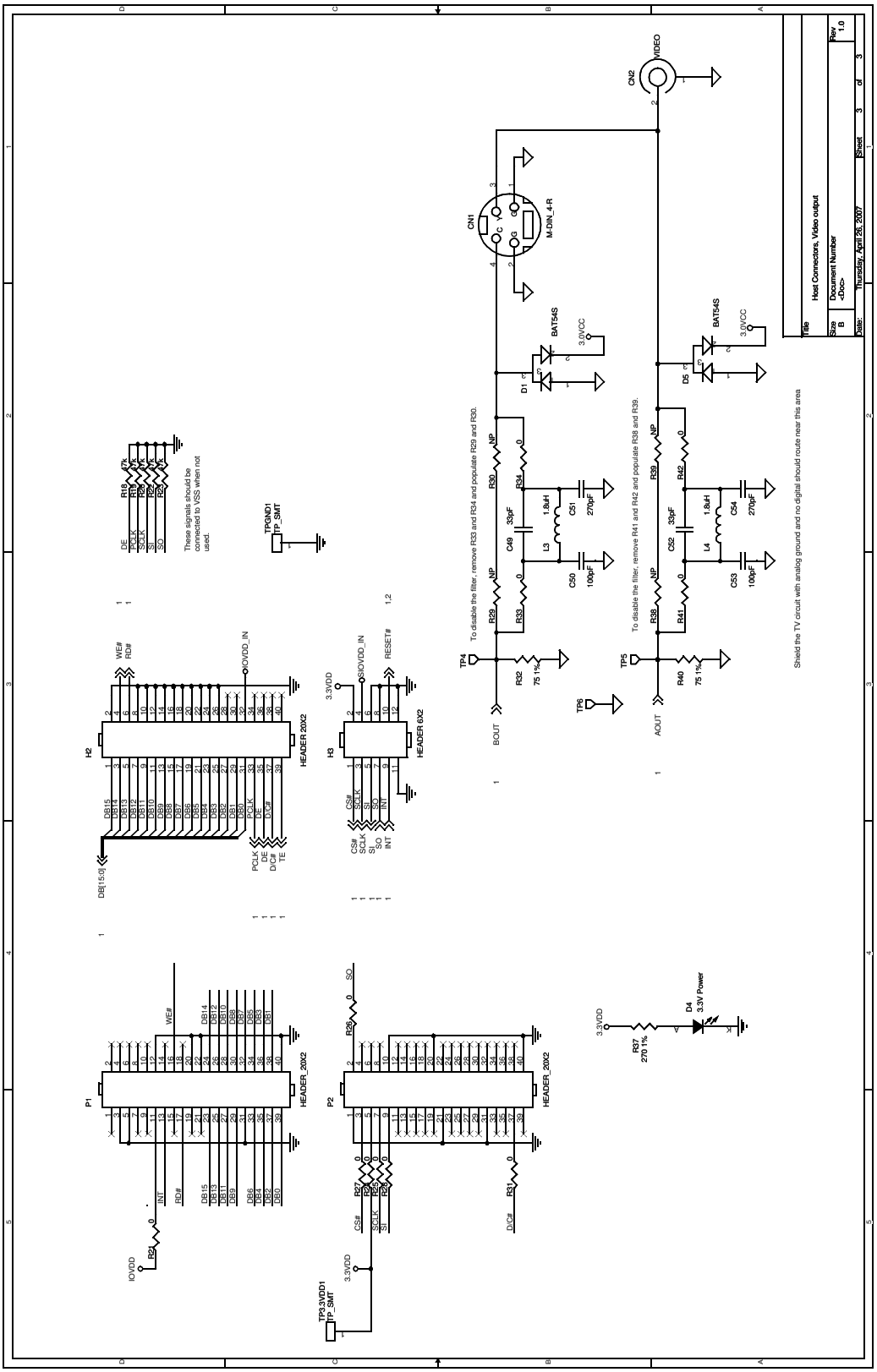

Figure 6-3: S5U13746P00C100 Schematics (3 of 3)

7 S5U13746P00C100 Board Layout

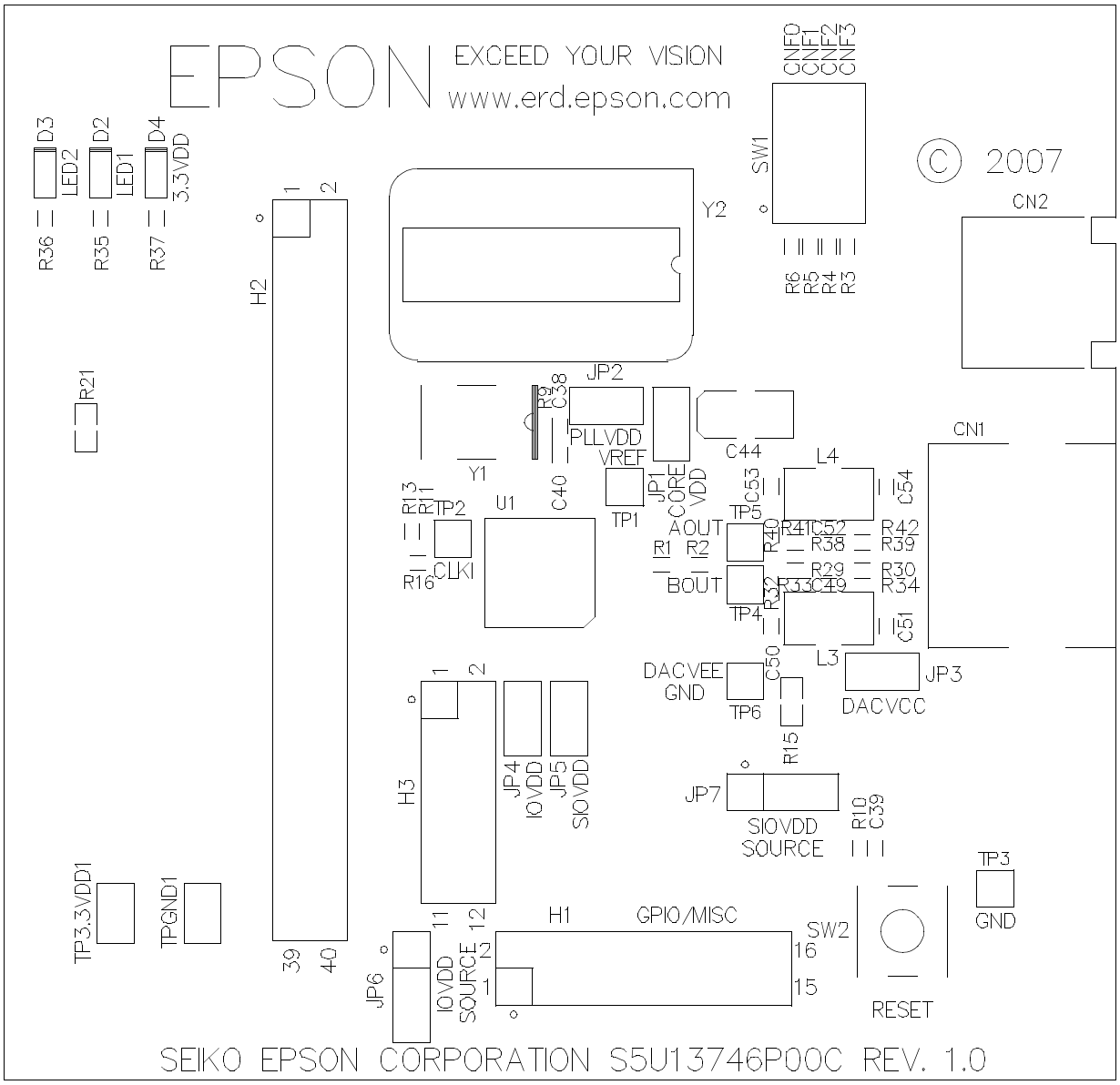

Figure 7-1: S5U13746P00C100 Board Layout - Top View

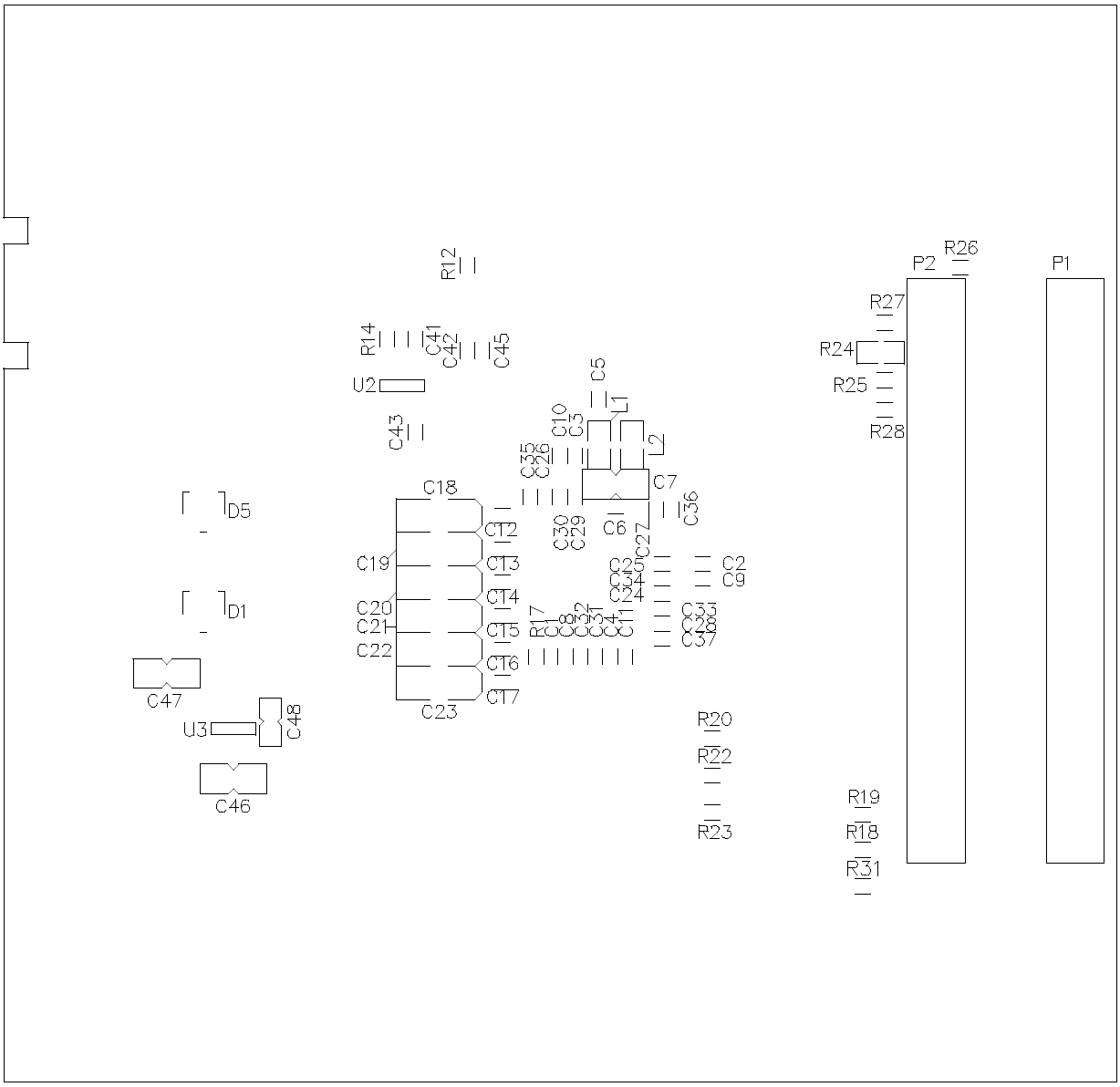

Figure 7-2: S5U13746P00C100 Board Layout - Bottom View