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S6AP111A28

2ch DC/DC Converter IC with PWM Synchronous Rectification

Description

S6AP111A28 is an Nch MOS drive-compatible 2ch DC/DC Converter IC with synchronous rectification that is equipped with a bottom detection comparator. It supports low on-duty operation to allow stable output of low voltages when there is a large difference between input and output voltages. It supports high-speed responses and achieves high efficiency. CH1 can change the internal reference voltage and is suitable for the power supply of POL.

Features

- High efficiency: 96% (maximum)
- High accuracy reference voltage: +/-0.7% (+25°C)
- Input voltage range: 6V to 28V
- Output voltage setting range: 0.75V to 5.5V
- CH1 reference voltage with built-in variable function
- Built-in boost switch
- Over voltage protection function
- Under voltage protection function
- Over current detection function
- Built-in soft start circuit: 1.4 ms (typical)
- Built-in discharge control circuit
- Built-in synchronous rectification type output steps for Nch MOS FET
- Standby current: 0 μA (typical)
- Small package: TSSOP-24

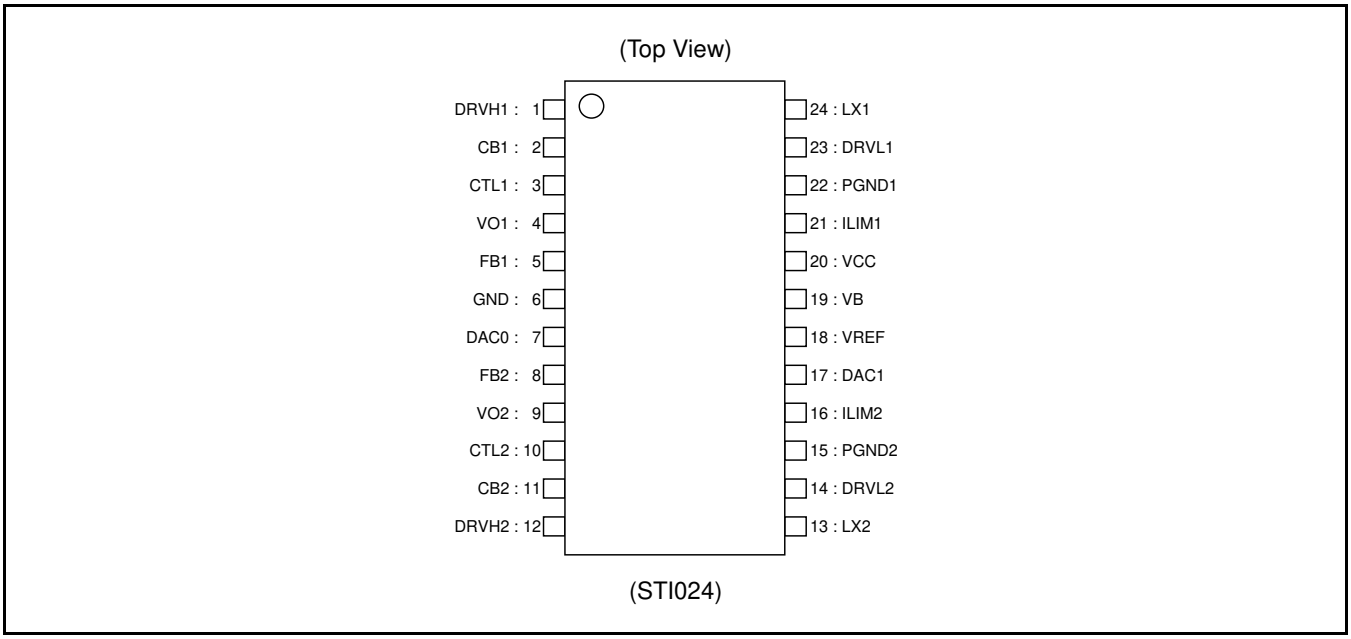
Applications

- Industrial equipment
- Multi-function printers
- Storage devices
- Servers and PCs

Contents

1. Pin Assignment

Figure 1-1. Pin Assignment



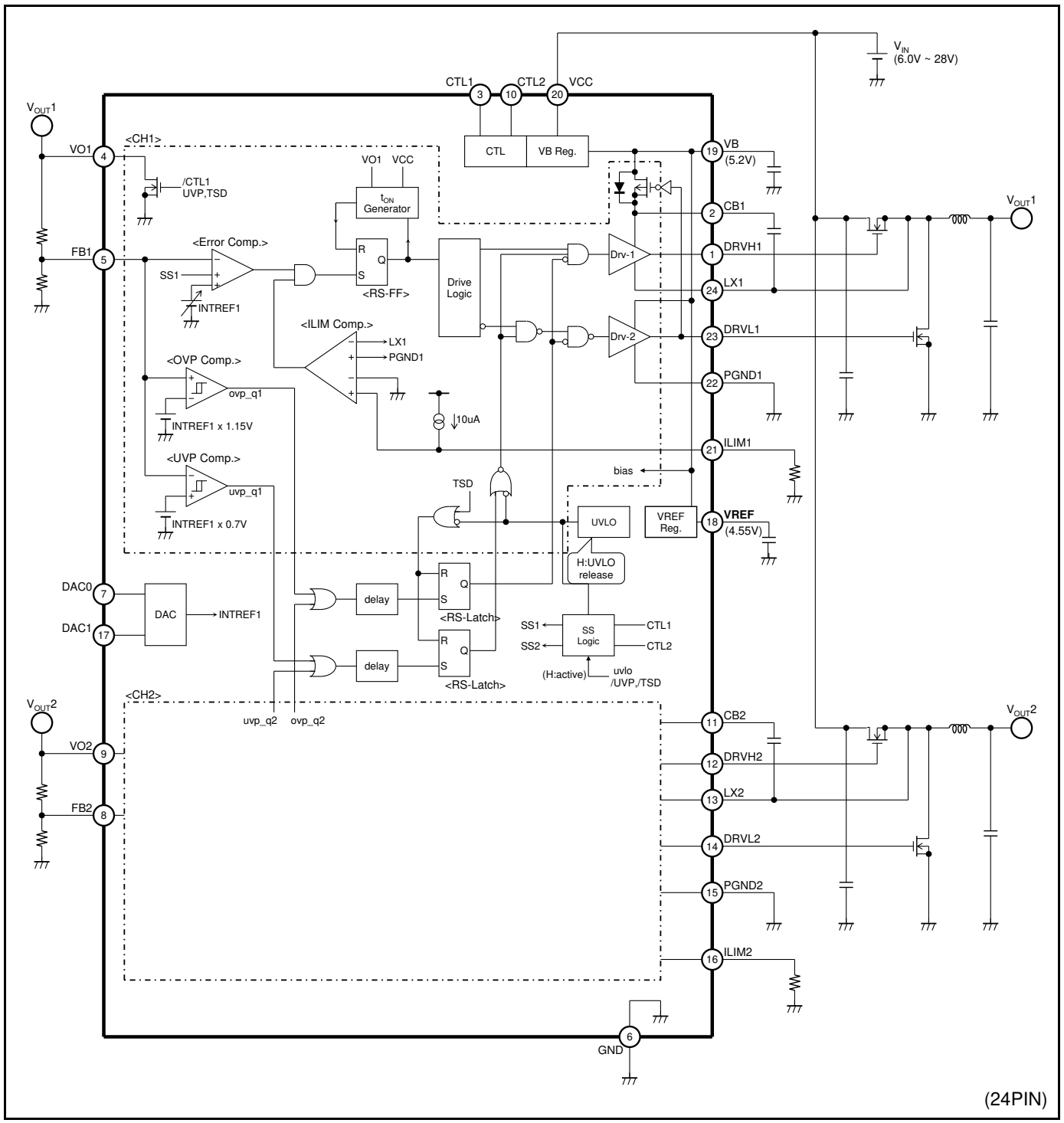
2. Pin Descriptions

Table 2-1. Pin Descriptions

Pin Number	Pin Name	I/O	Function Description
1	DRVH1	O	CH1 output pin for external high side FET gate drive.
2	CB1	-	CH1 bootstrap capacitor connection pin.
3	CTL1	I	CH1 control pin.
4	VO1	I	CH1 input pin for DC/DC output voltage.
5	FB1	I	CH1 feedback pin for DC/DC output voltage.
6	GND	-	Ground pin.
7	DAC0	I	CH1 DAC input pin for change the internal reference voltage.
8	FB2	I	CH2 feedback pin for DC/DC output voltage.
9	VO2	I	CH2 input pin for DC/DC output voltage.
10	CTL2	I	CH2 control pin.
11	CB2	-	CH2 bootstrap capacitor connection pin.
12	DRVH2	O	CH2 output pin for external high side FET drive.
13	LX2	-	CH2 inductor and external high side FET source connection pin.
14	DRVL2	O	CH2 output pin for external synchronous rectification-side FET gate drive.
15	PGND2	-	Ground pin for CH2 output circuit.
16	ILIM2	I	CH2 over current detection level setting voltage input pin.
17	DAC1	I	CH1 DAC input pin for change the internal reference voltage.
18	VREF	O	Control circuit bias output pin.
19	VB	O	Output circuit bias output pin.
20	VCC	I	Power supply pin for the reference voltage and control circuit.
21	ILIM1	I	CH1 over current detection level setting voltage input pin.
22	PGND1	O	Ground pin for CH1 output circuit.
23	DRVL1	O	CH1 output pin for external synchronous rectification-side FET gate drive.
24	LX1	-	CH1 inductor and external high side FET source connection pin.

3. Block Diagram

Figure 3-1. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		
			Min	Max	Unit
Power supply voltage	V_{VCC}	-	-0.3	+36	V
CB pin input voltage	V_{CB}	CB1 and 2 pins	-0.3	+42	V
LX pin input voltage	V_{LX}	LX1 and 2 pins	-2.0	+36	V
Voltage between CB and LX	V_{CBLX}	-	-0.3	+6.9	V
Control input voltage	V_I	CTL1 and 2 pins	-0.3	+30	V
Input voltage	V_{FB}	FB1 and 2 pins	-0.3	+6.9	V
	V_{VO}	VO1 and 2 pins	-0.3	+6.9	V
	V_{ILIM}	ILIM 1 and 2 pins	-0.3	+6.9	V
	V_{DAC}	DAC 0 and 1 pins	-0.3	+6.9	V
Power Dissipation*1	P_D	Ta ≤ +25°C	0	1333	mW
Storage temperature	T_{STG}	-	-55	+125	°C

*1: Given that the IC is mounted on four-layer FR-4 board.

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VCC}	-	6	-	28	V
CB pin input voltage	V_{CB}	-	-	-	V_{VCC} +VB	V
CTL pin input voltage	V_I	CTL1 and 2 pins	0	-	28	V
Input voltage	V_{FB}	FB1 and 2 pins	0	-	VREF	V
	V_{VO}	VO1 and 2 pins	0	-	VB	V
	V_{ILIM}	ILIM1 and 2 pins	30	-	200	mV
	V_{DAC}	DAC0 and 1 pins	0	-	VB	V
Peak output current	I_{OUT}	DRVH1 and 2 pins, DRVL1 and 2 pins Duty ≤ 5% (t = 1/f_{OSC}xDuty)	-1200	-	+1200	mA
CB pin capacity	C_{CB}	-	-	0.1	1.0	µF
Bias voltage output capacity	C_{VB}	-	-	2.2	10	µF
Reference voltage output capacity	C_{REF}	-	-	1.0	4.7	µF
Operating ambient temperature	Ta	-	-40	+25	+85	°C

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

6. Electrical Characteristics

VCC = 12V, CTL1,2 = 5V, Ta = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Bias Voltage Block [VB Reg.]						
Output voltage	V_{VB}	-	5.04	5.20	5.36	V
Input stability	LINE	VCC = 6V to 28V	-	10	100	mV
Load stability	LOAD	VB = 0A to -1 mA	-	10	100	mV
Short circuit output current	I_{OS}	VB = 0V	-220	-140	-100	mA
Bias Voltage Block [VREF Reg.]						
VREF output voltage	VVREF	VREF pin	4.45	4.55	4.65	V
Under Voltage Lock Out Protection [UVLO]						
UVLO VB Threshold voltage	V_{TLH}	VB pin	3.9	4.2	4.5	V
	V_{THL}	VB pin	3.3	3.6	3.9	V
Hysteresis width	V_H	VB pin	-	0.6(*1)	-	V
UVLO VREF Threshold voltage	V_{TLH}	VREF pin	3.5	3.8	4.1	V
	V_{THL}	VREF pin	3.3	3.6	3.9	V
Hysteresis width	V_H	VREF pin	-	0.2(*1)	-	V
Soft start/Discharge Block [Soft-Start, Discharge]						
Soft start time	t_{SS}	FB1, 2 = 0.735V	0.9	1.4	1.9	ms
Electrical discharge resistance	R_D	CTL1,2 = 0V, VO1, 2 = 0.5V	-	35	70	Ω
Discharge end voltage	V_O	CTL1,2 = 0V, VO1, 2 pins	0.1	0.2	0.3	V
ON/OFF Time Generator Block [t_{ON} Generator]						
ON time	t_{ON1}	VCC = 12V, VO1 = 1.2V	320	400	480	ns
	t_{ON2}	VCC = 12V, VO2 = 1.8V	320	400	480	ns
Minimum ON time	t_{ONMIN}	VCC = 12V, VO1, 2 = 0V	-	140	170	ns
Minimum OFF time	t_{OFFMIN}	-	-	380	560	ns
Error Comparison Block [Error Comp.]						
Threshold voltage [Ch1]	V_{TH11}	DAC1, DAC0 = 0,0 DC threshold	0.797	0.802	0.807	V
	V_{TH12}	DAC1, DAC0 = 0,1 DC threshold	0.829	0.834	0.839	V
	V_{TH13}	DAC1, DAC0 = 1,0 DC threshold	0.862	0.867	0.872	V
	V_{TH14}	DAC1, DAC0 = 1,1 DC threshold	0.765	0.770	0.775	V
Threshold voltage [Ch2]	V_{TH2}	DC threshold	0.768	0.773	0.778	V
FB pin input current	I_{FB}	FB1, 2 = 0.8V	-0.1	0	0.1	µA
VO pin input current	I_{VO}	VO1, 2 = 2V	-	20	29	µA

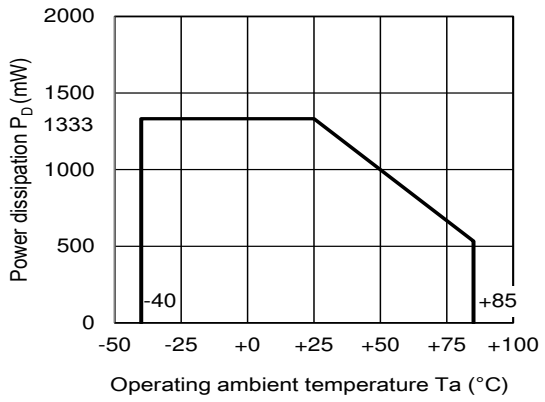
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Over voltage Protection Circuit Block [OVP Comp.]						
Over voltage detecting voltage	V_{OVP}	Error Comp. input	INTREF ×1.11	INTREF ×1.15	INTREF ×1.19	V
Over voltage detection delay time	t_{OVP}	-	-	50(*1)	-	µs
Under voltage Protection Circuit Block [UVP Comp.]						
Under voltage detecting voltage	V_{UVP}	Error Comp. input	INTREF ×0.65	INTREF ×0.70	INTREF ×0.75	V
Under voltage detection delay time	t_{UVP}	-	1.2(*1)	1.7(*1)	2.2(*1)	ms
Thermal shutdown Protection Circuit Block [TSD]						
Protection temperature	T_{TSDH}	-	-	+150(*1)	-	°C
	T_{TSDL}	-	-	+125(*1)	-	°C
DAC Block [DAC]						
DAC input "H" condition	V_{IH}	DAC1, DAC0 pins	2.64	-	VB	V
DAC input "L" condition	V_{IL}	DAC1, DAC0 pins	0	-	0.66	V
Output Block [DRV]						
High side output on resistance	R_{OH}	DRVH1, 2 = -100 mA	-	5	7	Ω
	R_{OL}	DRVH1, 2 = 100 mA	-	1.5	2.5	Ω
Low side output on resistance	R_{OH}	DRVL1, 2 = -100 mA	-	4	6	Ω
	R_{OL}	DRVL1, 2 = 100 mA	-	1	2	Ω
Output source current	I_{SOURCE}	LX1, 2 = 0V, CB1, 2 = VB DRVH1, 2 = 2.5 DUTY ≤ 5%	-	-0.4(*1)	-	A
		LX1, 2 = 0V, CB1, 2 = VB DRVL1, 2 = 2.5V DUTY ≤ 5%	-	-0.5(*1)	-	A
Output sink current	I_{SINK}	LX1, 2 = 0V, CB1, 2 = VB DRVH1, 2 = 2.5V DUTY ≤ 5%	-	0.7(*1)	-	A
		LX1, 2 = 0V, CB1, 2 = VB DRVL1, 2 = 2.5V DUTY ≤ 5%	-	0.9(*1)	-	A
Deadtime	T_D	LX1, 2 = 0V, BST1, 2 = VB	-	30(*1)	-	ns
Boost switch on resistance	R_{BST}	IVB = 30 mA	-	30	40	Ω
Leakage current	I_{LEAK}	CB1, 2 = 33.2V, LX1, 2 = 28V	-	0.1	1	µA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Over Current Detection Block [Current Sense]						
ILIM pin source current	I_{ILIM}	ILIM1, 2 = 0.1V	-12.5	-10	-8.3	µA
ILIM pin source current Temperature slope	T_{ILIM}	-	-	4200(*1)	-	ppm /°C
Overcurrent detection offset voltage	$V_{OFFILIM}$	ILIMx − (PGNDx−LXx) PGNDx − LX = 60 mV	-20	0	20	mV
Overcurrent detection Setting range	V_{ILIM}	ILIM input	30	-	200	mV
Control Block [CTL1, 2]						
On condition	V_{ON}	CTL1,2 pin	2	-	28	V
Off condition	V_{OFF}	CTL1,2 pin	0	-	0.8	V
Hysteresis width	V_H	CTL1,2 pin	-	0.4(*1)	-	V
Input current	I_{CTLH}	CTL1,2 = 5V	-	25	40	µA
	I_{CTLL}	CTL1,2 = 0V	-	0	1	µA
All Devices						
Standby current	I_{CCS}	VCC = 12V, CTL1,2 = 0V	-	0	10	µA
Power supply current	I_{CC}	VCC = 12V, LX1, 2 = 0V, FB1, 2 = 1.0V	-	1.3	1.8	mA

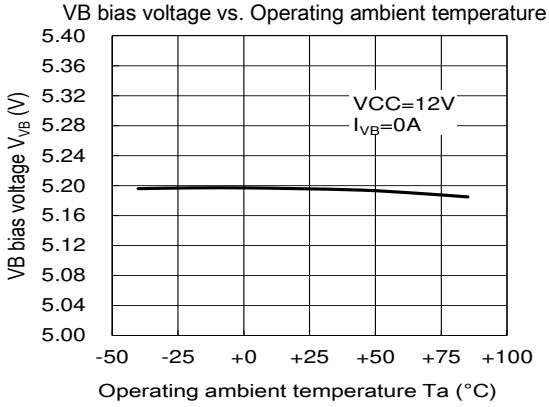
*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

7. Typical Characteristics

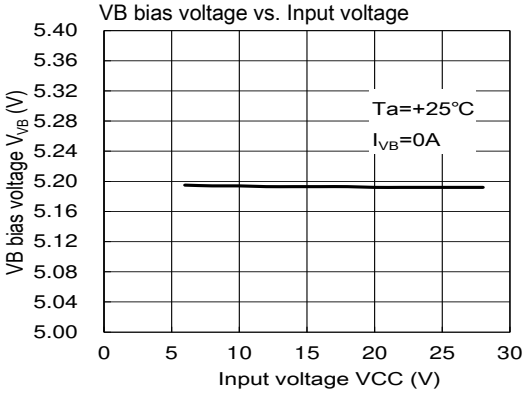
Power dissipation vs. Operating ambient temperature



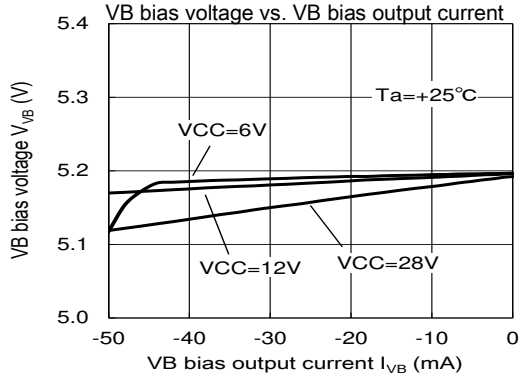
VB bias voltage vs. Operating ambient temperature



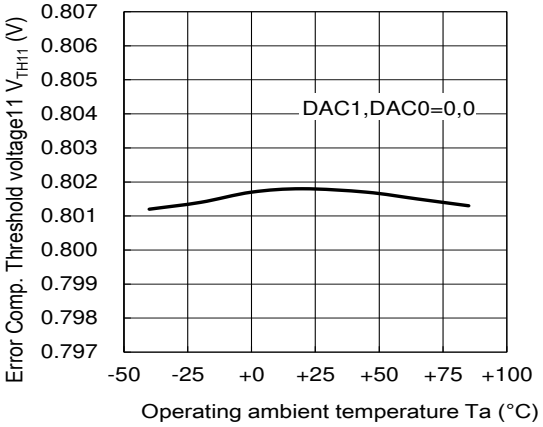
VB bias voltage vs. Input voltage



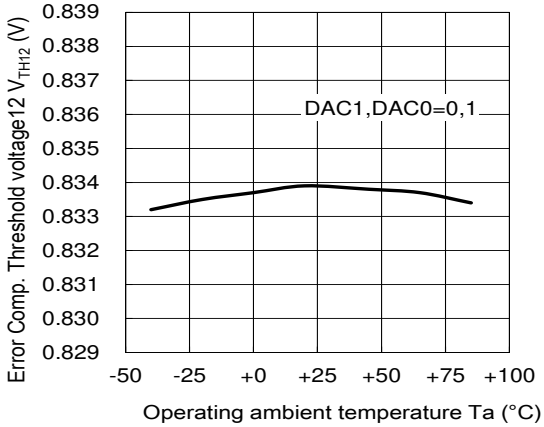
VB bias voltage vs. VB bias output current



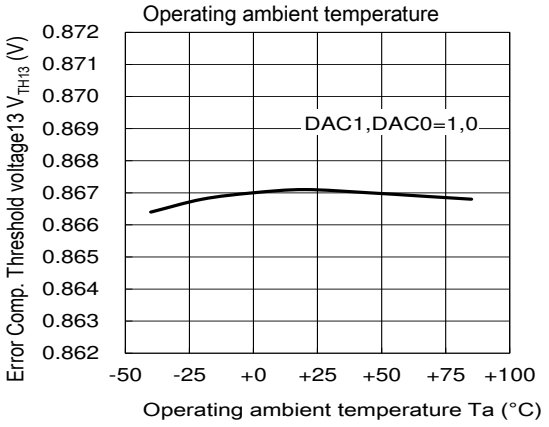
Error Comp. Threshold voltage (V_{TH11}) vs. Operating ambient temperature



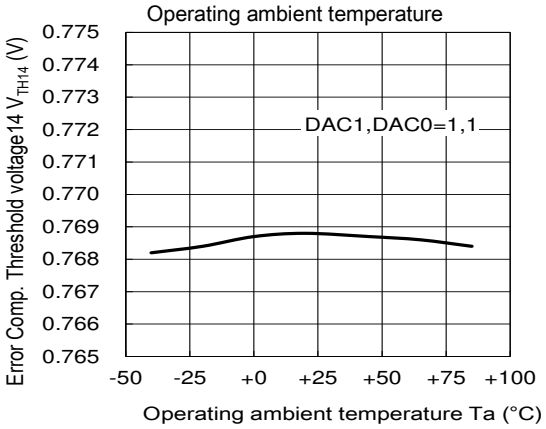
Error Comp. Threshold voltage (V_{TH12}) vs. Operating ambient temperature



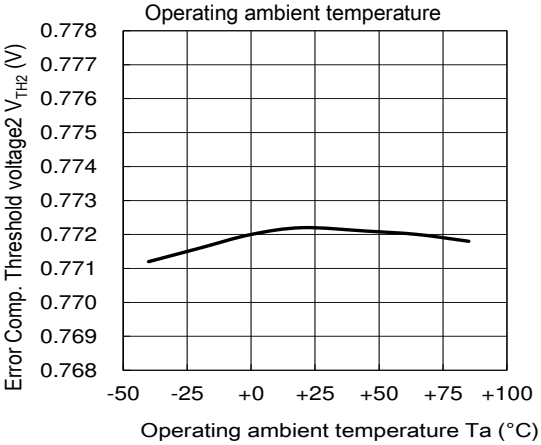
Error Comp. Threshold voltage (V_{TH13}) vs. Operating ambient temperature



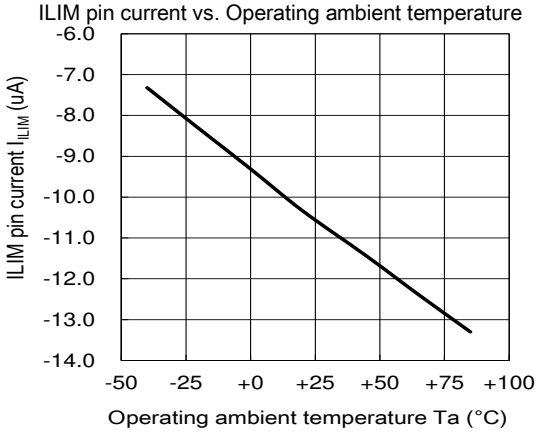
Error Comp. Threshold voltage (V_{TH14}) vs. Operating ambient temperature



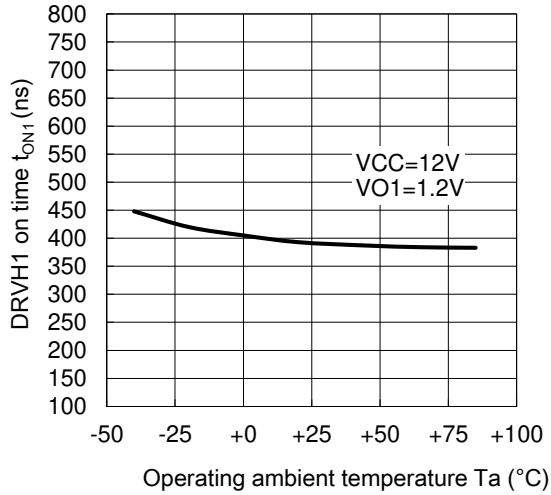
Error Comp. Threshold voltage (V_{TH2}) vs. Operating ambient temperature



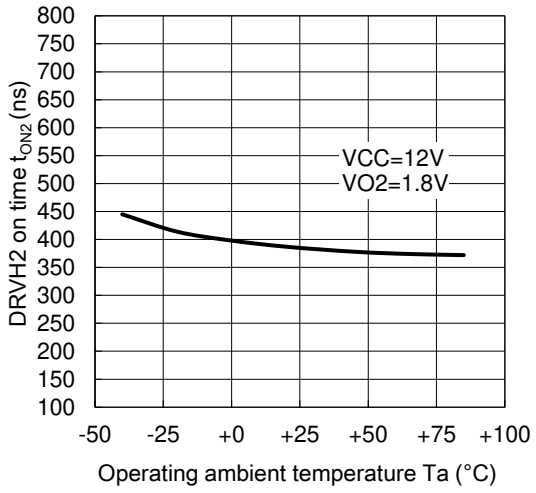
ILIM pin current vs. Operating ambient temperature



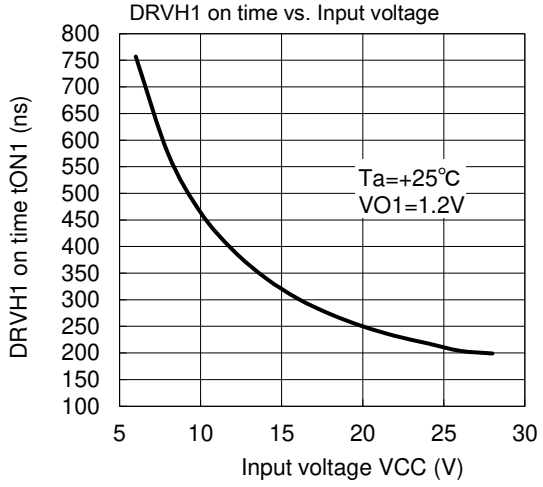
DRVH1 on time vs. Operating ambient temperature



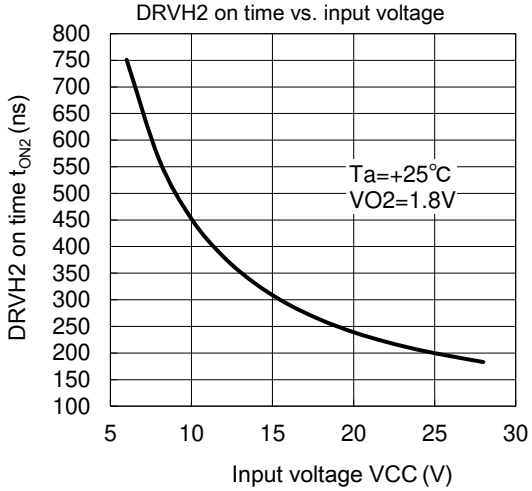
DRVH2 on time vs. Operating ambient temperature



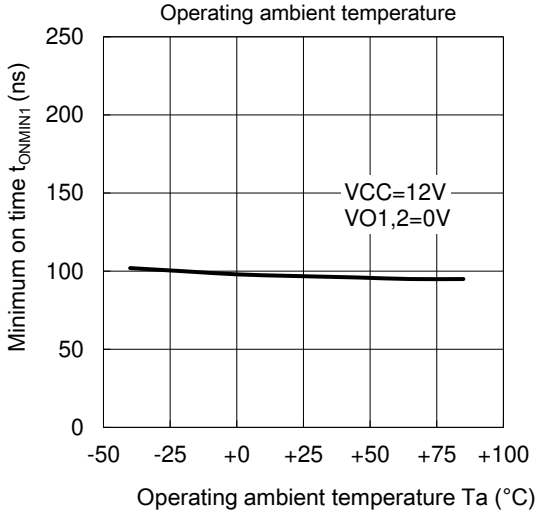
DRVH1 on time vs. Input voltage



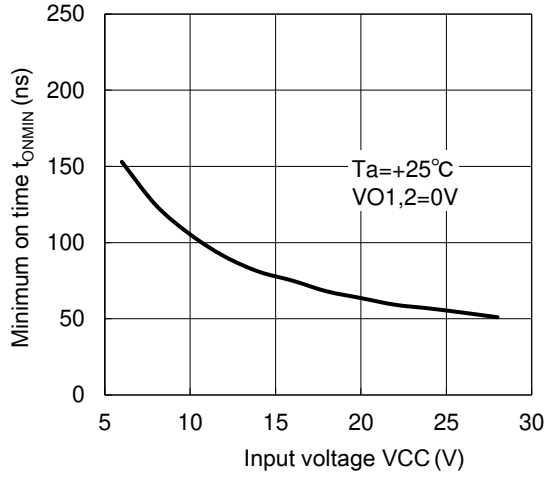
DRVH2 on time vs. input voltage



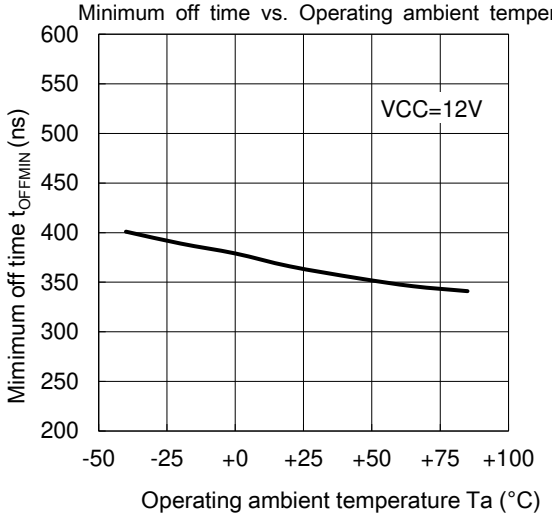
Minimum on time vs.
Operating ambient temperature



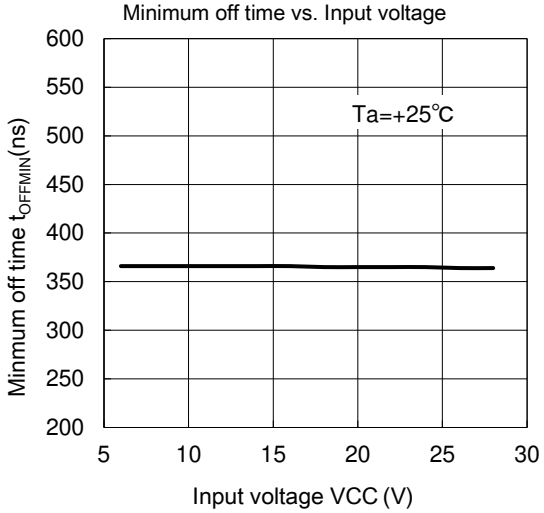
Minimum on time vs. Input voltage



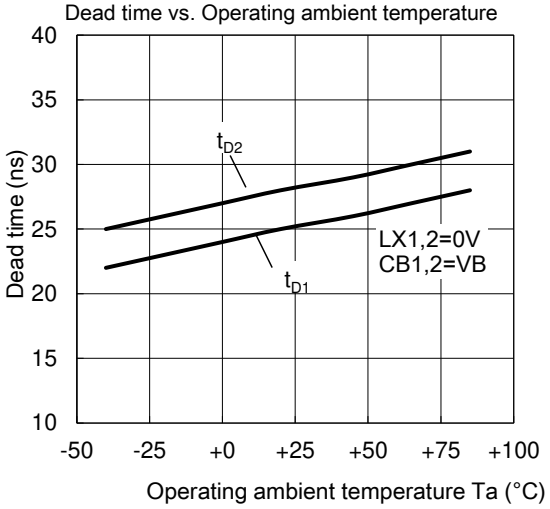
Minimum off time vs. Operating ambient temper



Minimum off time vs. Input voltage



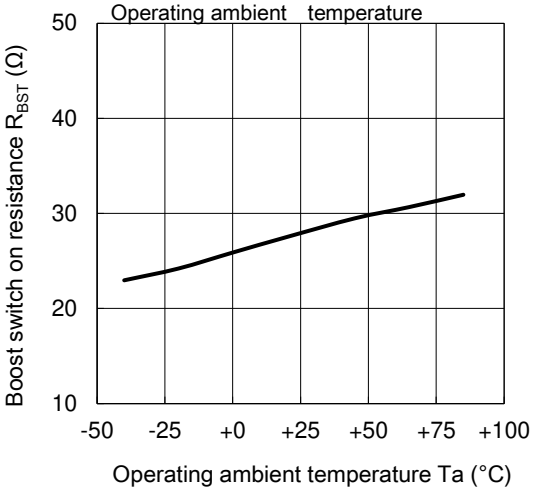
Dead time vs. Operating ambient temperature



t_{D1} : period from DRVL off to DRVH on

t_{D2} : period from DRVH off to DRVL on

Boost switch on resistance vs. Operating ambient temperature



8. Function Description

8.1 Bottom Detection Comparator System

The bottom detection comparator system for low output voltage ripple determines the ON time (t_{ON}) using the input voltage (V_{IN}) and output voltage (V_{OUT}) and holds the ON state for a specified period. During the OFF period, the reference voltage (INTREF) is compared with the feedback voltage (FB) using the error comparator (Error Comp.). When the feedback voltage (FB) is below the reference voltage (INTREF), RS-FF is set and the ON period starts again. Switching is repeated as described above. Error Comp. is used to compare the reference voltage (INTREF) with the feedback voltage (FB) to control the off time in order to stabilize the output voltage.

This system adds the inductor current slope detected during the synchronous rectification period (t_{OFF}) to the reference voltage (INTREF), and generates an output voltage slope in the IC during the OFF period, which is essential for the bottom detection comparator system. This enables the stable control operations under the low output voltage ripple conditions.

Figure 8-1. Circuit Diagram

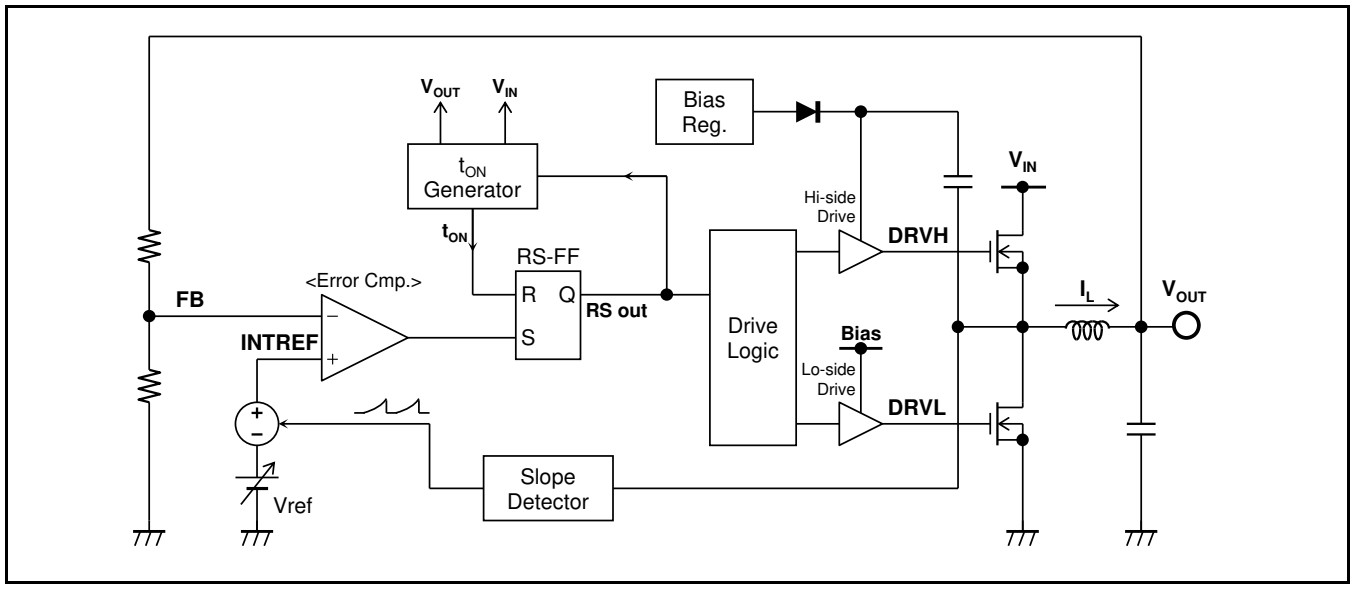
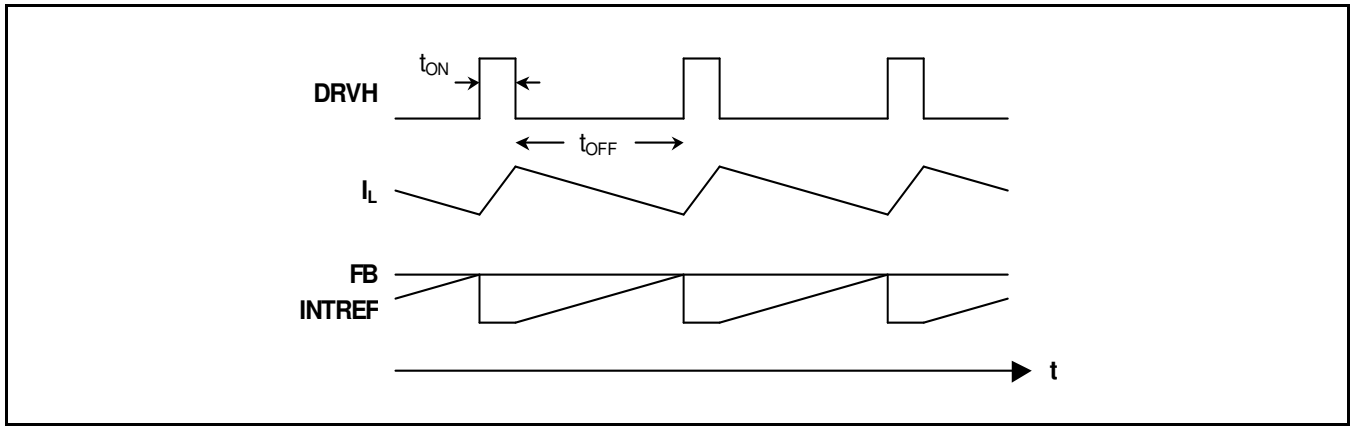


Figure 8-2. Bottom Detecting Operation



8.2 Bias Voltage Block [VB Reg., VREF Reg.]

VB Reg. generates 5.2V (typical) bias voltage from the VCC pin voltage for the control, output, and boost circuits. When either or both of the CTL1 or CTL2 pins (pins 3 and 10) are set to the “H” level, the system is restored from the standby state to supply the bias voltage from the VB pin (pin 19).

VREF Reg. generates a temperature compensating stable voltage of 4.55 V (typical) from the VREF pin (pin 18) which is used as the reference voltage in the IC and the bias power supply for the control circuit.

8.3 Under Voltage Lockout Protection Circuit Block (UVLO)

A transitional state or an instantaneous drop when the bias voltage (V_{VB}) for the control circuit starts will evoke malfunction of the IC and will cause system destruction or degradation. To avoid this sort of malfunction, the under voltage lockout protection detects a voltage drop in the VB pin (pin 19) and fixes the DRVH1 pin (pin 1), DRVH2 pin (pin 12), DRVL1 pin (pin 23), and DRVL2 pin (pin 14) to Level "L." The system recovers when the VB pin voltage exceeds the 4.2V threshold voltage (typical) of the under voltage lockout protection circuit.

8.4 Soft Start/Discharge Block (Soft Start, Discharge)

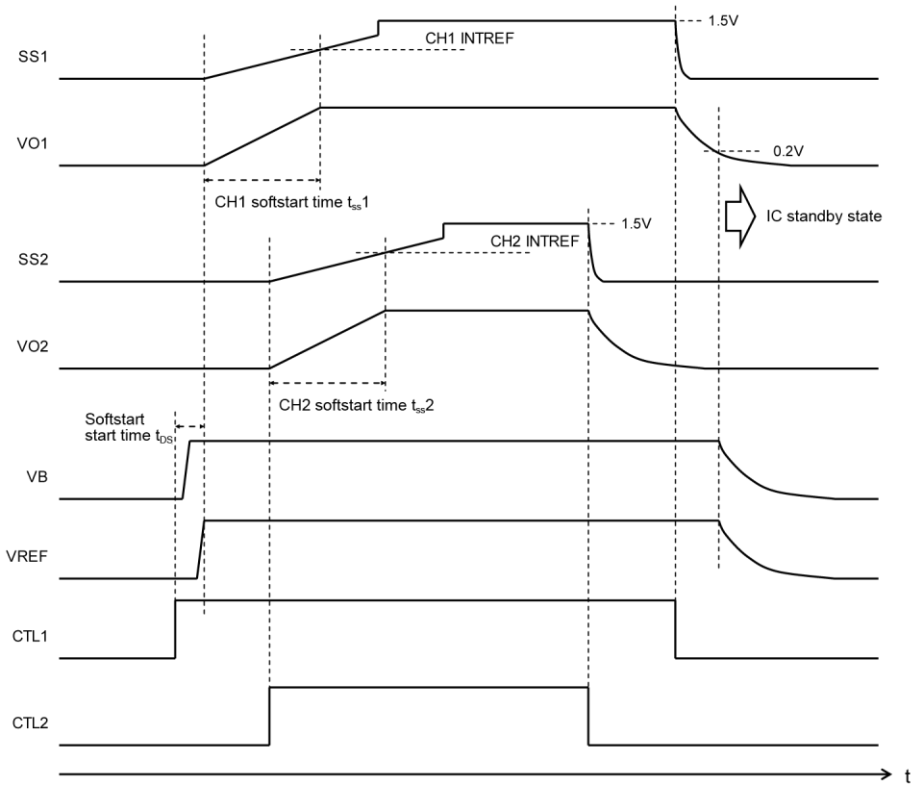
The soft start block is a circuit that prevents inrush current when powering on the IC.

When the CTL1 pin (pin 3) and CTL2 pin (pin 10) are set to Level "H," the reference voltage (SS1) for the CH1 error comparator and the reference voltage (SS2) for the CH2 error comparator start to increase in the soft start circuit built in to the IC. The reference voltages SS1 and SS2 increase linearly until the INTREF1 and INTREF2 voltages with the formula in Figure 10-3(tss1 and tss2). The system soft starts independent of the DC/DC convertor output load because the DC/DC convertor output increase with the same slope of the reference voltage.

From the time that the soft start commences until the initial switching commences, the low side FET stays OFF. The low side FET is allowed to come on after high side FET switching commences.

When the CTL1 pin (pin 3) and CTL2 pin (pin 10) are set to Level "L," the output capacitor discharges based on the FET(R_{ON}≈35Ω) for the discharge built in to the IC. When the VO1 pin (pin 4) and VO2 pin (pin 9) voltage becomes less than 0.2 V (typical) as a result of output capacitor discharge, the IC shuts down and transitions to standby. In addition, the discharge function operates both after under voltage protection circuit block (UVP Comp.) latch setting and after thermal shutdown protection circuit block (TSD) over temperature detection.

Figure 8-3. Example Timing Chart for Soft Start/Discharge



Channel	DAC0	DAC1	tss1
CH1	0V	0V	1.5 ms typ
	VB	0V	1.6 ms typ
	0V	VB	1.7 ms typ
	VB	VB	1.5 ms typ

Channel	DAC0	DAC1	tss2
CH2	-	-	1.5 ms typ

tss1,2 is calculated using the following formula.

$$tss1,2(ms) = tss(ms) \times \frac{V_{INTREF}}{0.735}$$

tss1,2: Soft start time of DC/DC converter CH1,2

tss: Soft start time (1.4 ms typical), which is specified at "6. Electrical Characteristics "

INTREF: Internal reference voltage (DC threshold) [V], which is referred at " V_{TH} in 6. Electrical Characteristics "

8.5 ON/OFF Time Generator Block (t_{ON} Generator)

The ON/OFF time generator block (t_{ON} Generator) has a built-in capacitor for timing setting and a resistor for timing setting and generates ON time which depends on input voltage and output voltage, and a minimum 380 ns (typical) OFF time.

The ON time is set from the voltage value for VCC pin (pin 20), input pin VO1 (pin 4) and the VO2 pin (pin 9) for the output voltage for each channel, using the following formula. To avoid beats from frequency discrepancies between both channels, the CH2 frequency is set to 1.5 times the CH1 frequency.

$$When\ (\frac{V_{VO1}}{V_{VCC}} \geq 0.035), t_{ON1}(ns) = \frac{V_{VO1}}{V_{VCC}} \times 4000\ , f_{OSC1} \cong 250\ kHz$$

$$When\ (\frac{V_{VO2}}{V_{VCC}} \geq 0.052), t_{ON2}(ns) = \frac{V_{VO2}}{V_{VCC}} \times 2667\ , f_{OSC2} \cong 375\ kHz$$

The ON time is set so that it does not become less than the minimum 140 ns (typical). Therefore, when a soft start commences or when the input/output voltage ratio is small, the ON time operates at a minimum of 140 ns (typical).

$$When\ (\frac{V_{VO1}}{V_{VCC}} \leq 0.035), t_{ON1}(ns) = t_{ONMIN} = 140\ (typical)$$

$$When\ (\frac{V_{VO2}}{V_{VCC}} \leq 0.052), t_{ON2}(ns) = t_{ONMIN} = 140\ (typical)$$

8.6 Error Comparison Block (Error Comp.)

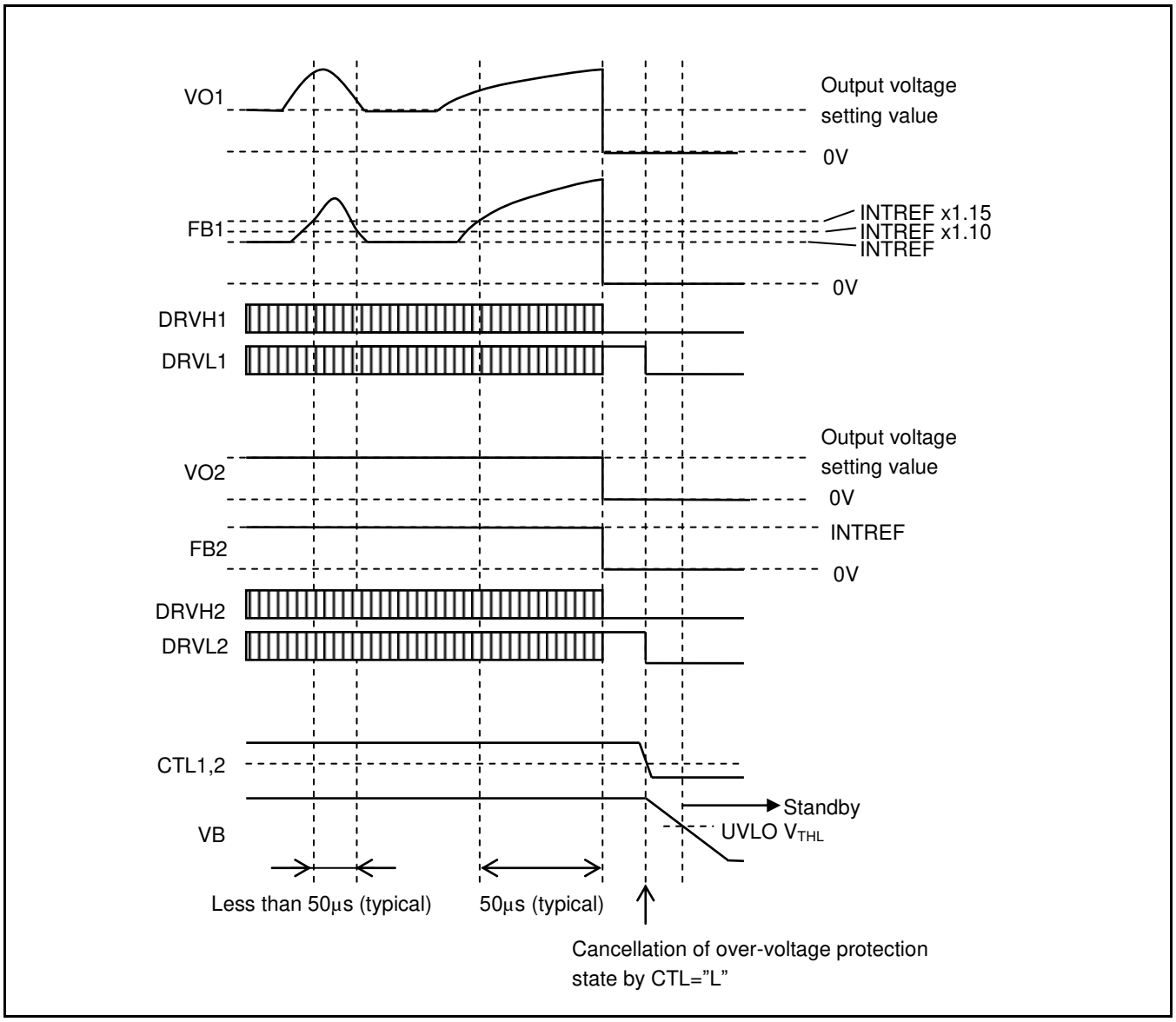
The error comparison block (Error Comp.) detects the bottom value of the output voltage ripple in the DC/DC converter.

You can set the output voltage flexibily(0.75V to 5.5V) by connecting an external output voltage setting resistor to FB1 (pin 5) and FB2 (pin 8).

8.7 Over Voltage Protection Circuit Block (OVP Comp.)

This function stops the output voltage when the DC/DC output voltage has increased, and protects devices connected to the output. This function compares the voltage that is 1.15 times (typical) the INTREF internal reference voltage with the feedback voltage that is input in the FB1 pin (pin 5) and the FB2 pin (pin 8). If the feedback voltage is found to be at least 50 μs (typical) higher, the RS latch is set, the DRVH1 pin (pin 1) and DRVH2 pin (pin 12) are set to Level "L", and the DRVL1 pin (pin 23) and DRVL2 pin (pin 14) are set to Level "H." The voltage output stops because these operations fix the high side FET to the off state and the low side FET to the on state for both channels of the DC/DC converter. Further, there is 5% (typical) hysteresis in the threshold for the over voltage protection operation to avoid malfunction of the over voltage protection function.

Figure 8-4. Example Timing Chart for the Over Voltage Protection Operation



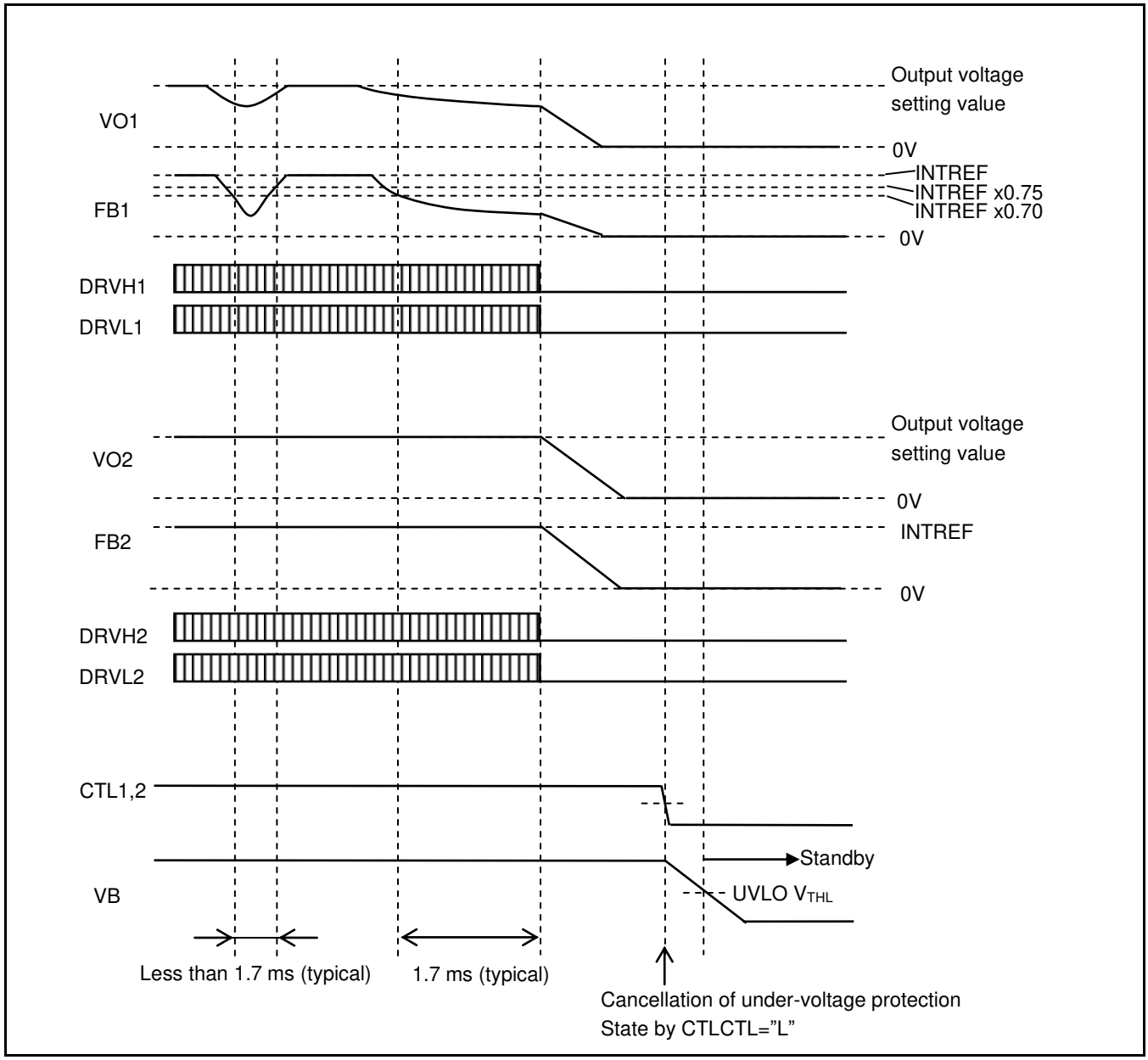
The over voltage protection state is released (the RS latch for over voltage protection is reset) under either of the following conditions.

- UVLO detection in the stop sequence after setting both the CTL1 pin (pin 3) and CTL2 pin (pin 10) to Level "L".
- UVLO detection in VCC power-off
- Thermal shutdown protection function (TSD) detection.

8.8 Under Voltage Protection Circuit Block (UVP Comp.)

This function stops the output voltage when the DC/DC output voltage has decreased, and protects devices connected to the output. This function compares the voltage that is 0.7 times (typical) the INTREF internal reference voltage with the feedback voltage that is input in the FB1 pin (pin 5) and the FB2 pin (pin 8). If the feedback voltage is found to be at least 1.7 ms (typical) lower, the RS latch is set, the DRVH1 pin (pin 1) and DRVH2 pin (pin 12) are set to Level "L", and the DRVL1 pin (pin 23) and DRVL2 pin (pin 14) are set to Level "L." In addition, when the latch is set for under voltage protection, the discharge function built in to the IC starts at the same time and voltage output stops for both channels. Further, there is 5% (typical) hysteresis in the threshold for the under voltage protection operation to avoid malfunction of the under voltage protection function.

Figure 8-5. Example Timing Chart for the Under Voltage Protection Operation



The under voltage protection state is released (the RS latch for under voltage protection is reset) under either of the following conditions.

- UVLO detection in the stop sequence after setting both the CTL1 pin (pin 3) and CTL2 pin (pin 10) to Level "L".
- UVLO detection in VCC power-off
- Thermal shutdown protection function (TSD) detection.

8.9 Thermal Shutdown Protection Block (TSD)

The thermal shutdown protection block (TSD) provides a function that prevents the IC from thermal damage. If the junction temperature of the thermal shutdown protection circuit reaches +150°C, the DRVH1 pin (pin 1) and DRVH2 pin (pin 12) are set to the “L” level, and the DRVL1 pin (pin 23) and DRVL2 pin (pin 14) are set to the “L” level, and switching stops. In addition, the discharge function that is built in to the IC runs, and voltage output for both channels stops. If the junction temperature drops to +125°C, the soft start is reactivated (restored automatically).

TSD detection is +150°C, but operations above the absolute maximum rating for the storage temperature (+125°C) are not guaranteed.

8.10 DAC Block (DAC)

You can change the reference voltage (INTREF1) for the CH1 error comparison block and the output voltage for the DC/DC converter by inputting an external 0V or VB pin voltage in the DAC0 pin (pin 7) and DAC1 pin (pin 17).

Table 8-1. Reference Voltage Settings

DAC0	DAC1	CH1 Reference Voltage (INTREF1)
0V	0V	0.802V typ
VB	0V	0.834V typ
0V	VB	0.867V typ
VB	VB	0.770V typ

8.11 Output Block (DRV1 and 2)

The output circuit is configured in CMOS format for both of the high side and the low side, and can drive an external Nch MOS FET.

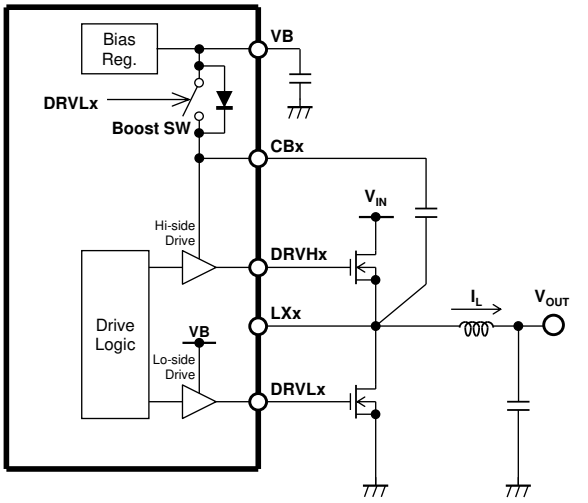
The output block for the high side FET supplies power from the built-in boost circuit, and the output block for the low side FET supplies power from the VB. This circuit prevents through-current by monitoring the gate voltages of the high side and low side FETs and controlling the timing of turning on one FET until the other FET is off. The sink ON resistance of the output circuit is a low 1Ω (typical), and the self turn on margin for the low side FET is improved.

8.12 Boost Circuit Block (CB1 and 2)

The boost circuit is needed high side FET in a case using Nch MOS FET.Efficiency improvement and/or reduction in parts cost can be expected of High side FET by using Nch MOSFET.

The boost circuit is formed a boost charge pump block which consists of the built-in switch for bootstraps and the condenser connected between CB pin and the LX pin. Then the condenser is charged through built-in switch from VB. The boosted power supply for gate drives of high side FET. The boost circuit has a built-in boost switch that eliminates the boost voltage (voltage between the CB pin and LX pin) loss of the forward voltage (Vf) that existed in older boost diodes. Therefore further efficiency improvement and reduction in parts cost can be expected more than a diode system.

Figure 8-6. Output Block and Boost Circuit Block



x: Each channel number

8.13 Over Current Detection Block (ILIM Comp.)

This function limits the output current when it has increased, and protects devices connected to the output. It compares the difference in voltage between the PGND1 pin (pin 22) and the LX1 pin (pin 24) and the ILIM1 pin (pin 21) voltage, and the difference in voltage between the PGND2 pin (pin 15) and LX2 pin (pin 13) and the ILIM2 pin (pin 16) voltage during the synchronous rectification period, and performs over current detection in every cycle.

The high side FET stays off until the difference in voltage between PGNDx and LXx is lower than the ILIMx pin voltage, and turns on after it becomes lower. This is how over current protection is performed. This protection operation drops the output voltage.

For the difference in voltage between PGNDx and LXx during the synchronous rectification period, the low side FET on resistance is sense resistance, and the inductor current is the sensed voltage waveform.

A 10 μA (typical) I_{ILIM} current is supplied from the ILIMx pin, so you can set any over current limit value by connecting resistance to the ILIMx pin. For the I_{ILIM} current, a temperature slope of 4200ppm/°C is set to compensate for the temperature dependence characteristics of the low side FET on resistance.

8.14 Control Block (CTL)

Turn CH1 on or off using the CTL1 pin (pin 3) and turn the CH2 on or off using the CTL2 pin (pin 10). Setting both CTL1 and 2 to Level "L" at the same time puts it in standby (the power supply current during standby is a maximum of 10 μA).

Table 8-2. Control Functions

CTL1	CTL2	DC/DC Converter (CH1)	DC/DC Converter (CH2)
L	L	OFF	OFF
H	L	ON	OFF
L	H	OFF	ON
H	H	ON	ON

8.15 Table of Protection Functions

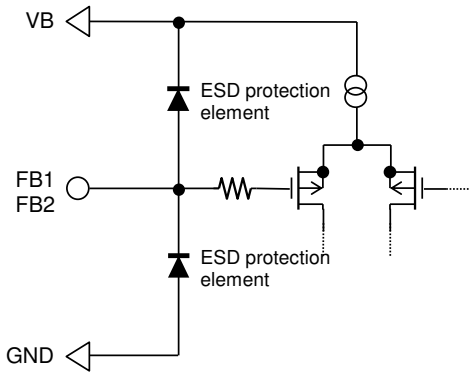
The following table shows the state of the DRVH1 and 2 pins (pins 1 and 12) and the DRVL1 and 2 pins (pins 23 and 14) when each protection function is in operation.

Table 8-3. Protection Functions

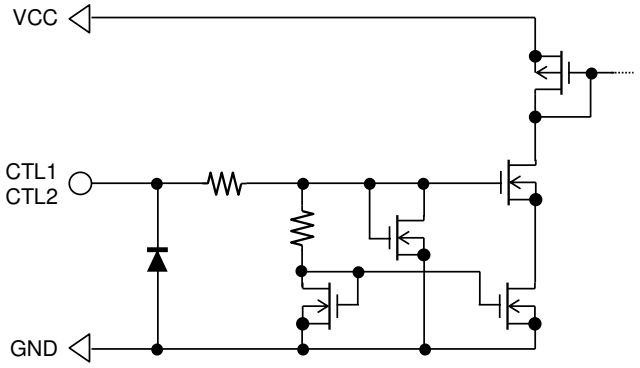
Protection function	Detection condition	Output of each pin during detection			DC/DC output drop state
		VB	DRVHx	DRVLx	
Under voltage lockout protection (UVLO)	V_{VB} < 3.6V	-	L	L	Natural electric discharge
Under voltage protection (UVP)	V_{FBx} < INTREFx × 0.7 V	5.2V	L	L	Electrical discharge by discharge function
Over voltage protection (OVP)	V_{FBx} > INTREFx × 1.15 V	5.2V	L	H	0V clamping
Over current protection (ILIM)	$V_{PGNDx} - V_{LXx} > V_{ILIMx}$	5.2V	switching	switching	Dropped by the set current value
Thermal shutdown protection (TSD)	Tj > +150°C	5.2V	L	L	Electrical discharge by discharge function
Control (CTL)	CTLx : H → L (VOx > 0.2V)	5.2V	L	L	Electrical discharge by discharge function

9. I/O Pin Equivalent Circuit Diagram

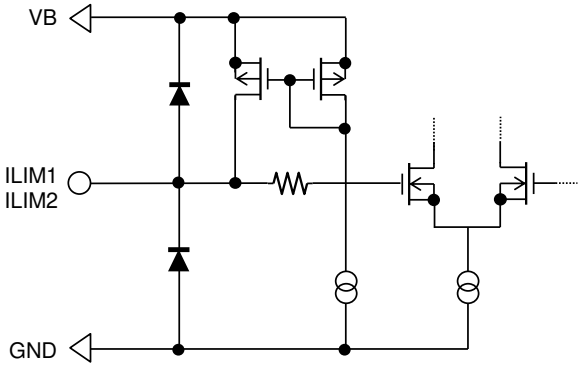
FB1, FB2 pins



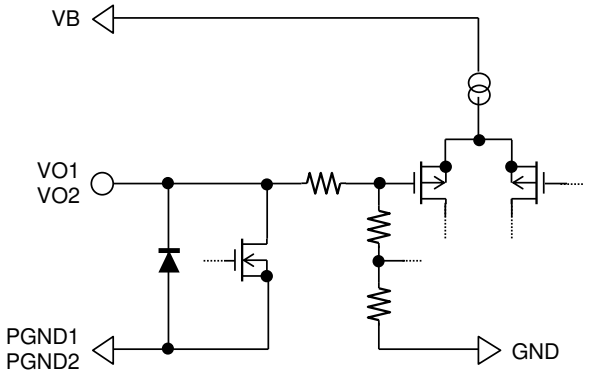
CTL1, CTL2 pins



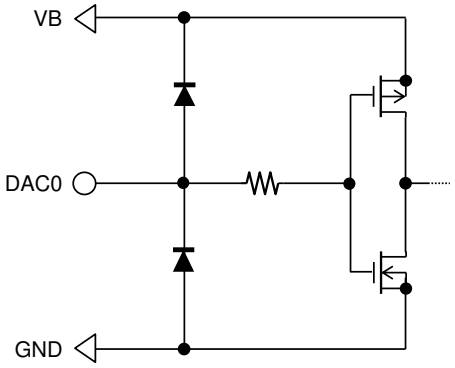
ILIM1, ILIM2 pins



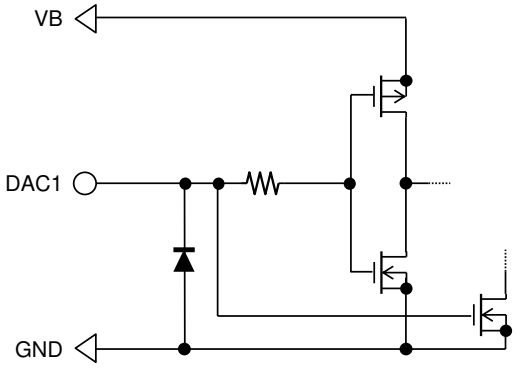
VO1, VO2 pins



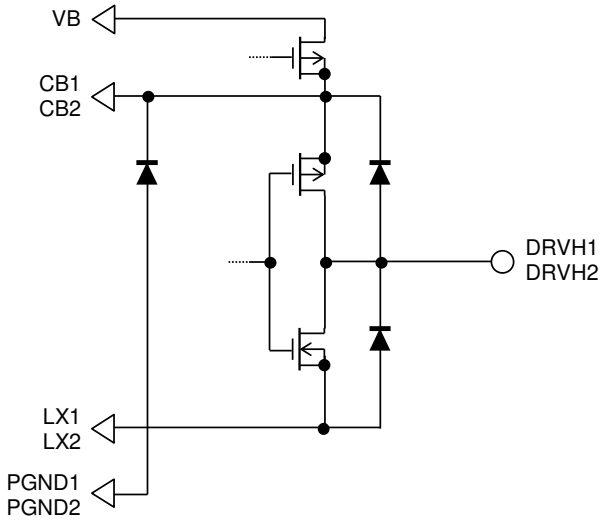
DAC0 pin



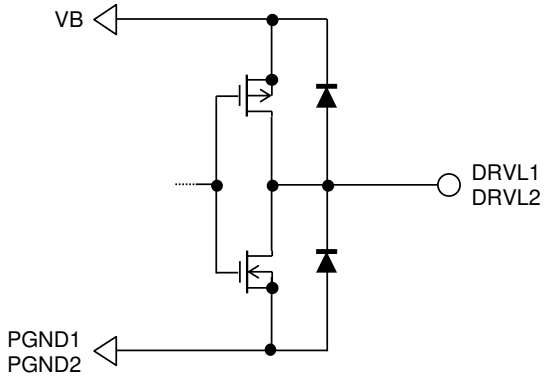
DAC1 pin



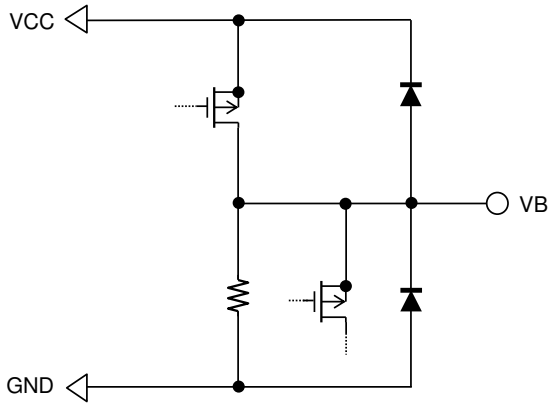
DRVH1, DRVH2, CB1, CB2, LX1, LX2 pins



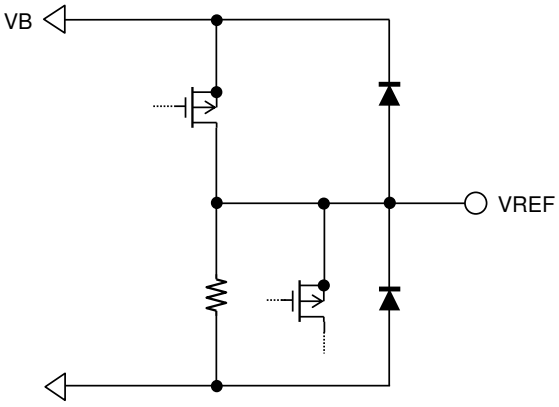
DRVL1, DRVL2 pins



VB pin



VREF pin



VCC, GND, PGND1, PGND2 pins