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S6AP413A

4ch DC/DC Converter with I²C Interface and Internal SW FETs

S6AP413A contains 3ch buck DC/DC converter and 1ch buck-boost DC/DC converter. S6AP413A can supply the main power line in several systems by using only its chip. The current mode control is adopted for the DC/DC converter, and it is possible to use the small chip inductor with the high switching frequency operation which contains internal switching FETs. S6AP413A contains the output setting resistor and the phase compensation circuit, and contributes to reduce the number of external components and its mount area. Also it contains the CTL input pin which can control the ON/OFF for each DC/DC converter, the Power Good signal output pin and I²C communication interface, therefore it is easy to design the power supply sequence. It is possible to tune in the output voltage exactly using the I²C communication.

Features

- Operating input voltage range: 2.5V to 5.5V (Maximum rating: 6.5V)
 - Output voltage setting range: DD1*:0.7V to 1.32V (20mV/step)
DD2*:1.2V to 1.95V (50mV/step)
DD3*:2.8V to 3.5V (100mV/step)
DD4*:0.7V to 1.32V (20mV/step)
 - Maximum output current: DD1:2A, DD2:1.2A, DD3:0.6A, DD4:2A
 - Internal switching FETs, output voltage setting resistor, phase compensation circuit and output discharge resistor (all DC/DC converters)
 - Buck-boost DC/DC converter is seamless to change operation mode
 - Soft start time setting range: 1 ms to 16 ms (approximately 1ms/step)
 - Switching frequency for the DC/DC converter: 3 MHz
 - Communication interface: I²C (ON/OFF, Output voltage, Soft start time)
 - Internal PFM/PWM auto switching mode
 - Each DC/DC converter Power Good function (open drain)
 - Several protection functions: Under voltage lockout (UVLO), Over current protection (OCP), Thermal shut down (TSD)
 - Small package: QFN32 (5mm × 5mm × 0.71mm, 0.5mm pitch)
- *: DD1, DD2, DD3, and DD4: DC/DC converter blocks 1,2,3,4

Applications

Network equipment, Factory automation, Security system, Surveillance camera, Electrical music instrument, Multi-function printer, Scanner, Printer, Copy machine, Home appliances, Data storage (HDD, SSD), Mobile equipment for Li+ battery (1 cell)

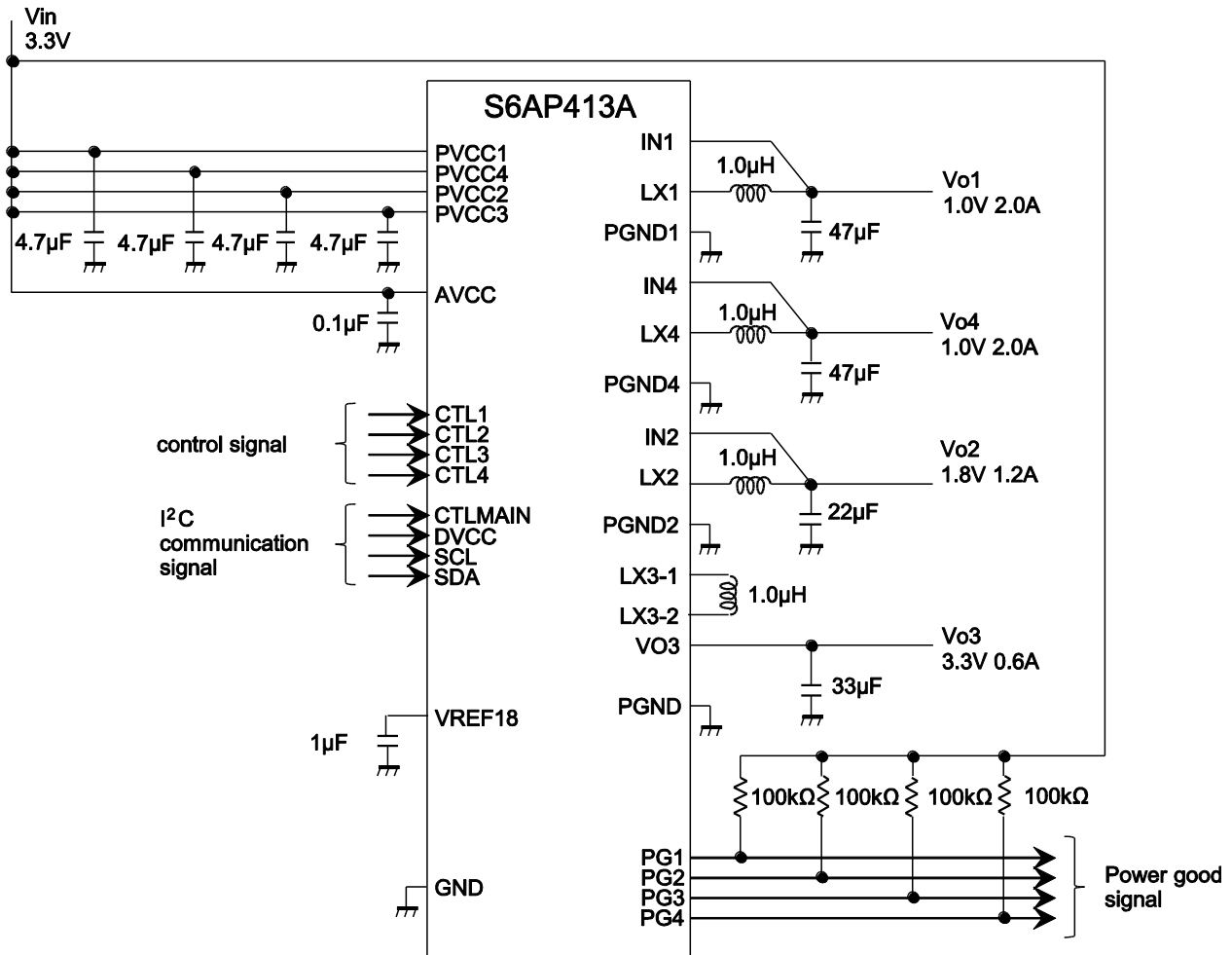
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1. Application Circuit Example

Figure 1. Application Circuit



2. Recommended Application Specification

[Input Voltage Range]

Input Voltage Vin(V)		
Min	Typ	Max
2.5	3.3	5.5

[Output specification]

(Ta=+25°C)

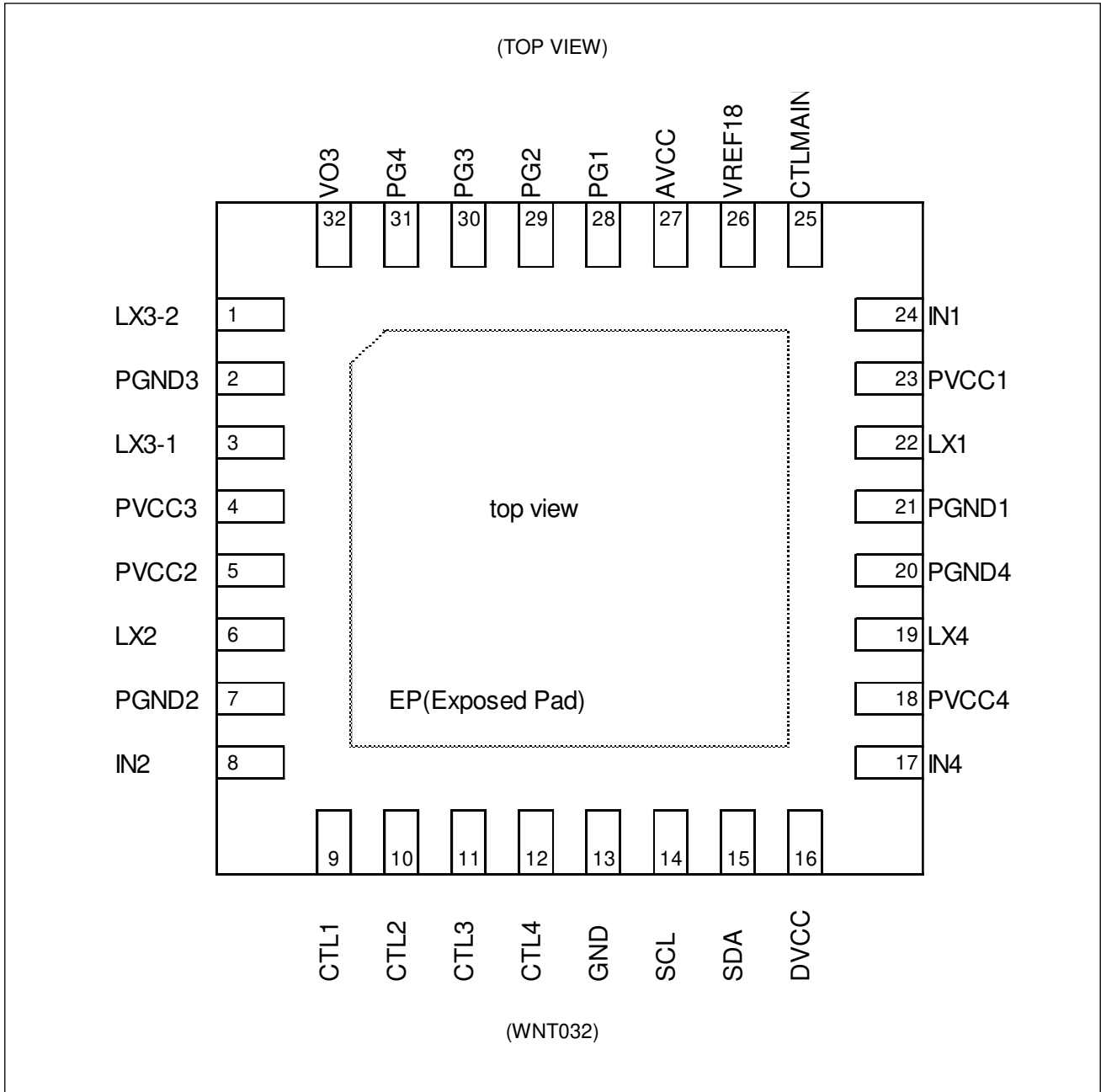
Channel	Symbol	Accuracy	Output Voltage (V)			Output Current(mA)	Limit Current(mA)	Mode	Switching Frequency(MHz)	Inductor(μH)	Output Capacitance	Soft-start Time (ms)	Discharge Resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD1	VO1	±1.2 %	0.692	0.700	0.708	2000	(2400)	Buck (synchronous rectification) C-mode	3.0	1.0	22	1 to 16ms At the time of 1.0V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			0.711	0.720	0.729									
			0.731	0.740	0.749									
			0.751	0.760	0.769									
			0.771	0.780	0.789									
			0.790	0.800	0.810									
			0.810	0.820	0.830									
			0.830	0.840	0.850									
			0.850	0.860	0.870									
			0.869	0.880	0.891									
			0.889 (*1)	0.900 (*1)	0.911 (*1)									
			0.909	0.920	0.931									
			0.929	0.940	0.951									
			0.948	0.960	0.972									
			0.968	0.980	0.992									
			0.988 (*1)	1.000 (*1)	1.012 (*1)									
			1.008	1.020	1.032									
			1.028	1.040	1.052									
			1.047	1.060	1.073									
			1.067	1.080	1.093									
			1.087 (*1)	1.100 (*1)	1.113 (*1)									
			1.107	1.120	1.133									
			1.126	1.140	1.154									
1.146	1.160	1.174												
1.166	1.180	1.194												
1.186 (*1)	1.200 (*1)	1.214 (*1)												
1.205	1.220	1.235												
1.225	1.240	1.255												
1.245	1.260	1.275												
1.265	1.280	1.295												
1.284	1.300	1.316												
1.304	1.320	1.336												

Channel	Symbol	Accuracy	Output Voltage (V)			Output Current(mA)	Limit Current(mA)	Mode	Switching Frequency(MHz)	Inductor(μH)	Output Capacitance	Soft-start Time (ms)	Discharge Resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD2	VO2	±1.2 %	1.186 (*1)	1.200 (*1)	1.214 (*1)	1200	(1500)	Buck (synchronous rectification) C-mode	3.0	1.0	10	1 to 16ms At the time of 1.8V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			1.235	1.250	1.265									
			1.284	1.300	1.316									
			1.334 (*1)	1.350 (*1)	1.366 (*1)									
			1.383	1.400	1.417									
			1.433	1.450	1.467									
			1.482 (*1)	1.500 (*1)	1.518 (*1)									
			1.531	1.550	1.569									
			1.581	1.600	1.619									
			1.630	1.650	1.670									
			1.680	1.700	1.720									
			1.729	1.750	1.771									
			1.778 (*1)	1.800 (*1)	1.822 (*1)									
			1.828	1.850	1.872									
1.877	1.900	1.923												
1.927	1.950	1.973												
DD3	VO3	±1.8 %	2.74 (*1)	2.80 (*1)	2.86 (*1)	600	(750)	Buck-boost (synchronous rectification) C-mode	3.0	1.0	22	1 to 16ms At the time of 3.3V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			2.84	2.90	2.96									
			2.94 (*1)	3.00 (*1)	3.06 (*1)									
			3.04	3.10	3.16									
			3.14	3.20	3.26									
			3.23 (*1)	3.30 (*1)	3.37 (*1)									
			3.33	3.40	3.47									
			3.43 (*1)	3.50 (*1)	3.57 (*1)									

Channel	Symbol	Accuracy	Output Voltage (V)			Output Current(mA)	Limit Current(mA)	Mode	Switching Frequency(MHz)	Inductor(μH)	Output Capacitance	Soft-start Time (ms)	Discharge Resistance (kΩ)	Remarks
			Min	Typ	Max	Max	Min							
DD4	VO4	±1.2 %	0.692	0.700	0.708	2000	(2400)	Buck (synchronous rectification) C-mode	3.0	1.0	22	1 to 16ms At the time of 1.8V setting, the details are cf. Contents 17	5.0	Built-in SWFET Built-in output setting resistors Built-in phase compensation circuit
			0.711	0.720	0.729									
			0.731	0.740	0.749									
			0.751	0.760	0.769									
			0.771	0.780	0.789									
			0.790	0.800	0.810									
			0.810	0.820	0.830									
			0.830	0.840	0.850									
			0.850	0.860	0.870									
			0.869	0.880	0.891									
			0.889 (*1)	0.900 (*1)	0.911(*1)									
			0.909	0.920	0.931									
			0.929	0.940	0.951									
			0.948	0.960	0.972									
			0.968	0.980	0.992									
			0.988 (*1)	1.000 (*1)	1.012 (*1)									
			1.008	1.020	1.032									
			1.028	1.040	1.052									
			1.047	1.060	1.073									
			1.067	1.080	1.093									
			1.087 (*1)	1.100 (*1)	1.113 (*1)									
			1.107	1.120	1.133									
			1.126	1.140	1.154									
1.146	1.160	1.174												
1.166	1.180	1.194												
1.186 (*1)	1.200 (*1)	1.214 (*1)												
1.205	1.220	1.235												
1.225	1.240	1.255												
1.245	1.260	1.275												
1.265	1.280	1.295												
1.284	1.300	1.316												
1.304	1.320	1.336												

*1:default(It is selectable with the default output voltage)

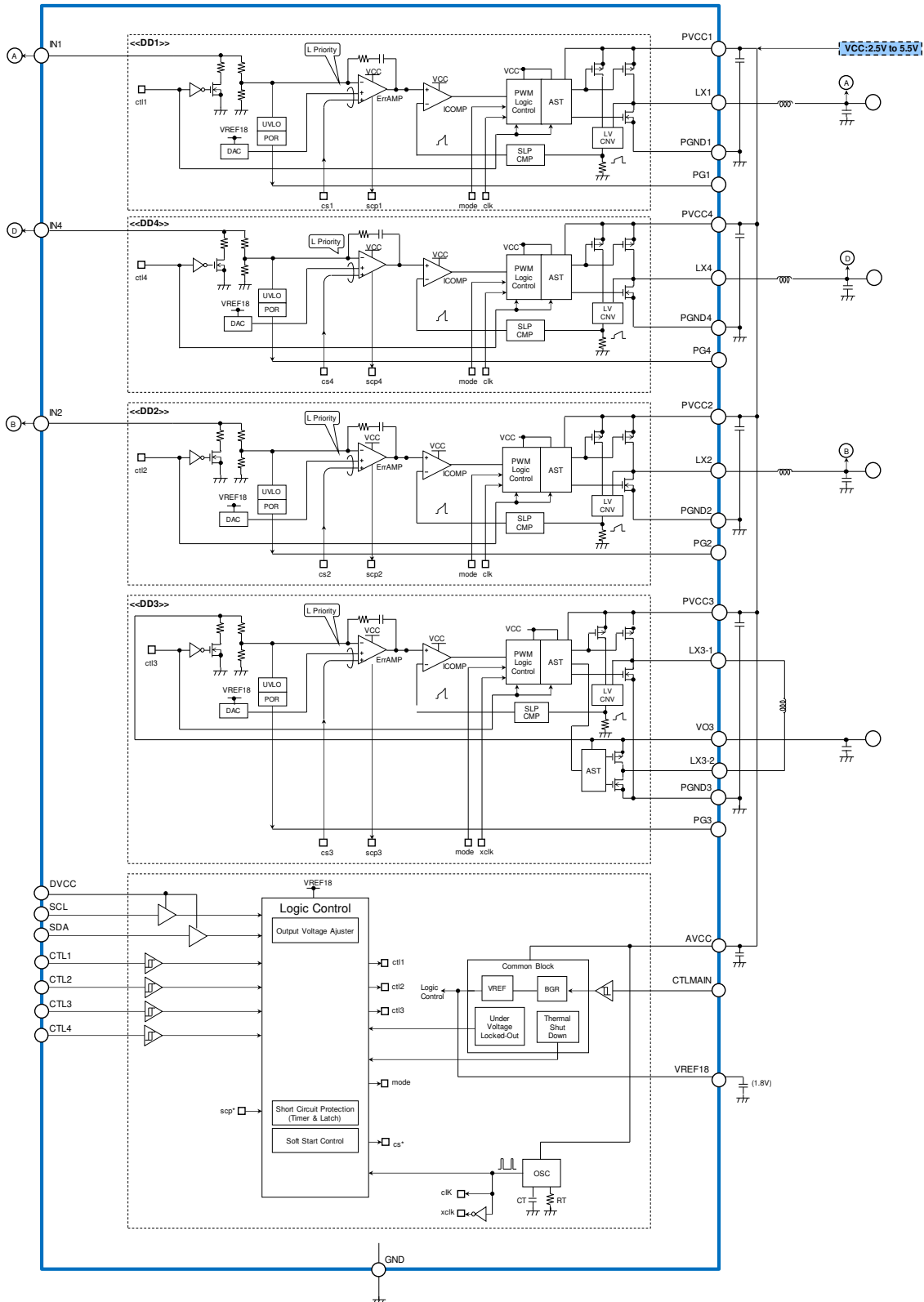
3. Pin Configuration



4. Pin Descriptions

Block	Pin Name	Pin Number	I/O	Description	Pull-down Resistor	Unused DD1	Unused DD2	Unused DD3	Unused DD4	Unused I ² C
DD1 Buck	IN1	24	I	DD1 output voltage feedback	-	GND	-	-	-	-
	PVCC1	23	-	DD1 output block power supply	-	AVCC	-	-	-	-
	LX1	22	O	DD1 inductor connection	-	Open	-	-	-	-
	PG1	28	O	DD1 Power Good output	-	GND	-	-	-	-
	PGND1	21	O	DD1 output block ground	-	GND	-	-	-	-
DD2 Buck	IN2	8	I	DD2 output voltage feedback	-	-	GND	-	-	-
	PVCC2	5	-	DD2 output block power supply	-	-	AVCC	-	-	-
	LX2	6	O	DD2 inductor connection	-	-	Open	-	-	-
	PG2	29	O	DD2 Power Good output	-	-	GND	-	-	-
	PGND2	7	-	DD2 output block ground	-	-	GND	-	-	-
DD3 Buck-boost	PVCC3	4	-	Power supply for DD3 output block	-	-	-	AVCC	-	-
	VO3	32	O	Output voltage for DD3	-	-	-	GND	-	-
	LX3-1	3	O	DD3 inductor connection1	-	-	-	Open	-	-
	LX3-2	1	O	DD3 inductor connection2	-	-	-	Open	-	-
	PG3	30	O	Output for DD3 Power Good	-	-	-	GND	-	-
	PGND3	2	-	Ground for DD3 output block	-	-	-	GND	-	-
DD4 Buck	IN4	17	-	DD4 output voltage feedback	-	-	-	-	GND	-
	PVCC4	18	-	DD4 output block power supply	-	-	-	-	AVCC	-
	LX4	19	O	DD4 inductor connection	-	-	-	-	Open	-
	PG4	31	O	DD4 Power Good output	-	-	-	-	GND	-
	PGND4	20	-	DD4 output block ground	-	-	-	-	GND	-
CTL	CTLM AIN	25	I	Control for reference voltage output	Exist	-	-	-	-	-
	CTL1	9	I	DD1 control	Exist	Open	-	-	-	-
	CTL2	10	I	DD2 control	Exist	-	Open	-	-	-
	CTL3	11	I	DD3 control	Exist	-	-	Open	-	-
	CTL4	12	I	DD4 control	Exist	-	-	-	Open	-
I ² C	DVCC	16	I	Power supply for I ² C communication	-	-	-	-	-	GND
	SCL	14	I	Clock for I ² C communication	-	-	-	-	-	Open
	SDA	15	I/O	Data for I ² C communication	Exist	-	-	-	-	Open
Reference control	AVCC	27	-	Power supply for reference voltage	-	-	-	-	-	-
	VREF18	26	O	Output reference voltage	-	-	-	-	-	-
	GND	13	-	Ground for reference voltage	-	-	-	-	-	-
	GND	EP	-	Ground for reference voltage	-	-	-	-	-	-

5. Block Diagram



6. Absolute Maximum Ratings

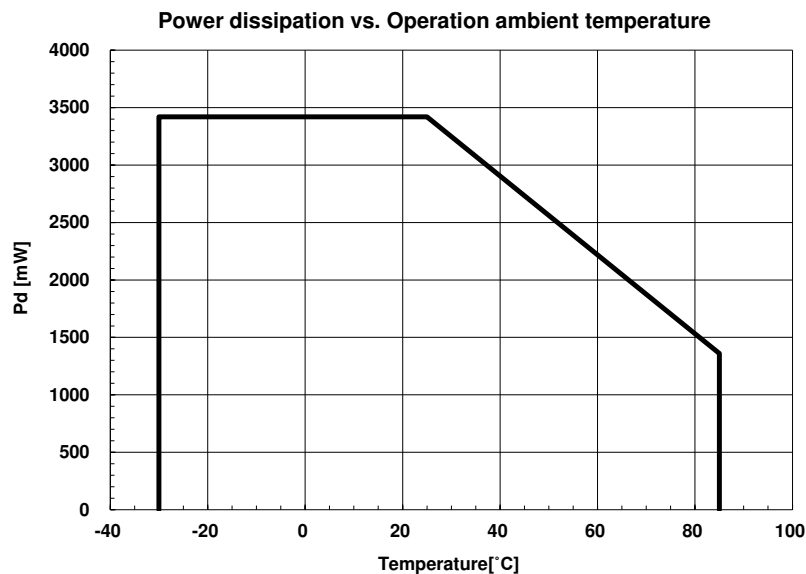
Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V _{VCC1}	AVCC, PVCC input voltage	-0.3	6.5	V
	V _{VCC2}	DVCC input voltage	-0.3	6.5	V
Terminal voltage	V _{CTL1}	CTL1, CTL2, CTL3 input voltage	-0.3	6.5	V
	V _{CTL2}	CTLMAIN input voltage	-0.3	6.5	V
	V _{LOGIC}	SDA, SCL input voltage	-0.3	6.5	V
	V _{PG}	PG1, PG2, PG3, PG4 drain voltage	-0.3	6.5	V
	V _{OUT}	IN1, IN2, IN3, IN4 input voltage	-0.3	6.5	V
LX voltage	V _{LX}	LX1, LX2, LX3, LX4 voltage	-1.0	6.5	V
Permission loss	P _D	T _a ≤ +25°C Thermal resistance(θ _{ja}):(29.2°C /W(*1))	0	3420	mW
Maximum junction temperature	T _{jmax}	-	-	+125	°C
Storage temperature	T _{STG}	-	-55	+125	°C

*1: When the IC is mounted on 74mm × 74mm four-layer square epoxy board. IC is mounted on a four-layer epoxy board, which terminal bias, and the IC's thermal pad is connected to the epoxy board.

WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Figure 2. Power Dissipation vs. Operation Ambient Temperature



7. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. Reference control block						
Power supply voltage	V _{VCC}	AVCC	2.5	3.3	5.5	V
Output current for reference voltage	I _{REF}	VREF18	-1	-	0	mA
Operating temperature	T _a	-	-30	+25	+85	°C
2. DC/DC channel						
Power supply voltage	V _{VCC}	PVCC1, PVCC2, PVCC3, PVCC4	2.5	3.3	5.5	V
Input voltage	V _{OUT}	IN1, IN2	0	-	AVCC	V
PG input voltage	V _{PG}	PG1, PG2, PG3, PG4	0	-	5.5	V
3. Input block						
Input voltage	V _{CTL} V _{MODE}	CTL1, CTL 2, CTL3, mode CTLMAN	0	-	AVCC	V
4. I ² C communication block						
Power supply voltage	V _{VCC}	DVCC	1.70	-	3.50	V
Input voltage	V _{LOGIC}	SDA, SCL	0	-	DVCC	V

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

8. Electrical Characteristics

8.1 Reference Control Block

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V, Ta = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. Reference voltage [VREF18]						
Output voltage	V _{VREF1}	VREF18 pin = 0mA	1.773	1.800	1.827	V
	V _{VREF2}	AVCC pin = 2.5V to 5.5V VREF18 pin = 0mA	1.768	1.800	1.832	V
	V _{VREF3}	VREF18 pin = 0mA to -1mA	1.768	1.800	1.832	V
2. Under voltage lockout [VCC UVLO]						
Threshold voltage	V _{TH}	AVCC rising	2.156	2.20	2.244	V
Hysteresis width	V _H	-	-	0.20(*1)	-	V
3. Over current protection [OCP]						
Timer	t _{OCP1}	DD1, DD2, DD3, DD4	0.9	1	1.1	ms
4. Thermal shut down [TSD]						
Stop temperature	T _{TSDH}	-	125(*2)	150	-	°C
5. Input block (CTL,mode,CTLMMAIN) [CTL,CTLMMAIN]						
Input voltage	V _{IH}	CTL1, CTL2, CTL3, CTL4 pin CTLMMAIN pin	AVCC ×0.7	-	AVCC	V
Input voltage	V _{IL}	CTL1, CTL2, CTL3, CTL4 pin CTLMMAIN pin	0	-	0.4	V
Input current	I _{CTLH} I _{MODEH}	CTL1, CTL2, CTL3, CTL4 pin = 3.3V CTLMMAIN pin = 3.3V	2.5	3.3	4.7	μA
	I _{CTL} I _{MODEL}	CTL1, CTL2, CTL3, CTL4 pin = 0V CTLMMAIN pin = 0V	-	-	1	μA
Input pull-down resistor	R _P	CTL1, CTL2, CTL3, CTL4 pin CTLMMAIN pin	-	1(*1)	-	MΩ
6. Consumption current (DC/DC converter block)						
Power supply current	I _{VCCS1}	CTL1, CTL2, CTL3, CTL4 pin = 0V CTLMMAIN pin = 0V	-	0	1.0	μA
	I _{VCCS2}	CTL1, CTL2, CTL3, CTL4 pin = 0V CTLMMAIN pin = 3.3V	-	30	45	μA
	I _{VCC}	DD1,DD2,DD3,DD4=ON, All DD are 0mA (operation mode: PFM/PWM mode)	-	450	670	μA
	I _{VCC}	DD1,DD2,DD3,DD4=ON, All DD are 0mA (operation mode: Fixed PWM mode)	-	18	27	mA

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

8.2 DD1

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply, PGND1=PGND2=PGND3=PGND4=GND = 0V. Ta = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. DC/DC converter block [DD1]						
Output voltage	V _{OUT}	I _{OUT} = -10mA, Output voltage setting: 1.0V	0.988	1.000	1.012	V
Input stability	V _{LINE}	I _{OUT} = -10mA, PVCC1= 2.5V to 5.5V	-5	-	+5	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -400mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -400mA (PFM/PWM mode)	-10	-	+15	mV
IN1 input impedance	R _{IN}	IN1 = 2.0V	-	190(*1)	-	kΩ
SW PMOS-Tr on resistance	R _{PMOS}	LX1 = -30mA	-	120(*1)	-	mΩ
SW NMOS-Tr on resistance	R _{NMOS}	LX1 = 30mA	-	80(*1)	-	mΩ
SW PMOS-Tr leakage current	I _{LEAK}	LX1 = 0V	-3	-	-	μA
SW NMOS-Tr Leakage current	I _{LEAK}	LX1 = 3.3V	-	-	3	μA
Over current protection value	I _{LIMIT}	L=1.0μH	2400(*2)	-	-	mA
PFM/PWM mode changeover current	I _{PFM}	L=1.0μH	-	100(*1)	-	mA
Discharge resistor	R _{DIS}	-	-	5(*1)	-	kΩ
Soft start time	T _{SS}	Soft start time setting: 1ms	0.9	1	1.1	ms
Switching frequency	f _{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

8.3 DD2

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. Ta = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
2. DC/DC converter block [DD2]						
Output voltage	V _{OUT}	I _{OUT} = -10mA, Output voltage setting:1.8V	1.778	1.800	1.822	V
Input stability	V _{LINE}	I _{OUT} = -10mA PVCC2= 2.5V to 5.5V	-5	-	+5	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -1200mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -1200mA (PFM/PWM mode)	-10	-	+20	mV
IN2 input impedance	R _{IN}	IN2 = 2.0V	-	150(*1)	-	kΩ
SW PMOS-Tr on resistance	R _{PMOS}	LX2 = -30mA	-	190(*1)	-	mΩ
SW NMOS-Tr on resistance	R _{NMOS}	LX2 = 30mA	-	135(*1)	-	mΩ
SW PMOS-Tr leakage current	I _{LEAK}	LX2 = 0V	-3	-	-	μA
SW NMOS-Tr leakage current	I _{LEAK}	LX2 = 3.3V	-	-	3	μA
Over current protection value	I _{LIMIT}	L=1.0μH	1500(*2)	-	-	mA
PFM/PWM mode changeover current	I _{PFM}	L=1.0μH	-	65(*1)	-	mA
Discharge resistor	R _{DIS}	-	-	5(*1)	-	kΩ
Soft start time	T _{SS}	Soft start time setting:1ms	0.9	1	1.1	ms
Switching frequency	f _{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

8.4 DD3

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. Ta = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
3. DC/DC converter block [DD3]						
Output voltage	V _{OUT}	I _{OUT} = -10mA, Output voltage setting:3.3V	3.241	3.300	3.359	V
Input stability	V _{LINE}	I _{OUT} = -10mA, PVCC3= 2.5V to 5.5V	-5	-	+5	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -600mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -600mA (PFM/PWM mode)	-10	-	+15	mV
VO3 impedance	R _{VO3}	VO3= 2.0V	-	550(*1)	-	kΩ
SW PMOS-Tr on resistance	R _{PMOS}	LX3-1 = -30mA	-	115(*1)	-	mΩ
SW NMOS-Tr on resistance	R _{NMOS}	LX3-1 = 30mA	-	140(*1)	-	mΩ
SW PMOS-Tr on resistance	R _{PMOS}	LX3-2 = -30mA	-	155(*1)	-	mΩ
SW NMOS-Tr on resistance	R _{NMOS}	LX3-2 = 30mA	-	220(*1)	-	mΩ
SW PMOS-Tr leakage current	I _{LEAK}	LX3-1 = 0V	-3	-	-	μA
SW NMOS-Tr leakage current	I _{LEAK}	LX3-1 = 3.3V	-	-	1	μA
SW PMOS-Tr leakage current	I _{LEAK}	LX3-2 = 0V	-3	-	-	μA
SW NMOS-Tr leakage current	I _{LEAK}	LX3-2 = 3.3V	-	-	1	μA
Over current protection value	I _{LIMIT}	L=1.0μH	1000(*2)	-	-	mA
PFM/PWM mode changeover current	I _{PFM}	L=1.0μH	-	200(*1)	-	mA
Discharge resistor	R _{DIS}	-	-	5(*1)	-	kΩ
Soft start time	T _{SS}	Soft start time setting:1ms	0.9	1	1.1	ms
Switching frequency	f _{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

8.5 DD4

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. Ta = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
4. DC/DC converter block [DD4]						
Output voltage	V _{OUT}	I _{OUT} = -10mA, Output voltage setting: 1.0V	0.988	1.000	1.012	V
Input stability	V _{LINE}	I _{OUT} = -10mA, PVCC4 = 2.5V to 5.5V	-5	-	+5	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -4000mA (Fixed PWM mode)	-10	-	+10	mV
Load stability	V _{LOAD}	I _{OUT} = -1mA to -4000mA (PFM/PWM mode)	-10	-	+15	mV
IN4 input impedance	R _{IN}	IN4 = 2.0V	-	190(*1)	-	kΩ
SW PMOS-Tr on resistance	R _{PMOS}	LX4 = -30mA	-	120(*1)	-	mΩ
SW NMOS-Tr on resistance	R _{NMOS}	LX4 = 30mA	-	80(*1)	-	mΩ
SW PMOS-Tr leakage current	I _{LEAK}	LX4 = 0V	-3	-	-	μA
SW NMOS-Tr Leakage current	I _{LEAK}	LX4 = 3.3V	-	-	3	μA
Over current protection value	I _{LIMIT}	L=1.0μH	2300(*2)	-	-	mA
PFM/PWM mode changeover current	I _{PFM}	L=1.0μH	-	75(*1)	-	mA
Discharge resistor	R _{DIS}	-	-	5(*1)	-	kΩ
Soft start time	T _{SS}	Soft start time setting: 1ms	0.9	1	1.1	ms
Switching frequency	f _{OSC}	-	2.7	3.0	3.3	MHz

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

*2: No production tested, ensure by design.

8.6 Digital Block

(AVCC = PVCC1=PVCC2=PVCC3=PVCC4= 3.3V supply,
PGND1=PGND2=PGND3=PGND4=GND = 0V. Ta = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
1. Power Good block [Power Good]						
Output voltage	V _{OL}	PG1, PG2, PG3, PG4 I _{OL} = 1mA	-	-	0.4	V
Output current	I _{OL}	PG1, PG2, PG3, PG4	1	-	-	mA
Low voltage detection	V _{TH}	IN1, IN2, IN4 = falling VO3 = falling	-	V _o × 0.90 (*1)	-	V
Power on detection	V _{TH}	IN1, IN2, IN4 = rising VO3 = rising	-	V _o × 0.93 (*1)	-	V
2. I ² C block [I ² C]						
Input voltage	V _{IH}	SCL,SDA	DVCC ×0.7	-	DVCC	V
	V _{IL}	SCL,SDA	0	-	DVCC ×0.3	V
Input current	I _{IH}	SCL,SDA DVCC = 3.3V	-	-	10	μA
	I _{IL}	SCL,SDA DVCC = 3.3V	-10	-	-	μA
Output voltage	V _{OL}	SDA I _{OL} = 3mA	-	-	0.4	V
Output current	I _{OL}	SDA	3	-	-	mA

*1: This parameter is not be specified. This should be used as a reference to support designing the circuits.

9. Operation Mode List

Table 1. Operation Mode List

	Mode	Stand-by	Stand-by2	Normal	Error Detection
CTL signal	CTLMAIN (external)	L	H	H	H
	CTL1 (external/I ² C)	L	L	H/L(*1)	X
	CTL2 (external/I ² C)	L	L	H/L(*1)	X
	CTL3 (external/I ² C)	L	L	H/L(*1)	X
	CTL4 (external/I ² C)	L	L	H/L(*1)	X
Operation Block	Reference	OFF	ON	ON	ON
	Digital	OFF	ON	ON	ON
	DD1	OFF	OFF	ON/OFF	OFF
	DD2	OFF	OFF	ON/OFF	OFF
	DD3	OFF	OFF	ON/OFF	OFF
I ² C communication	I ² C communication	disable	enable	enable	enable
Protection operating	Thermal shut down (TSD)	Not available	Not available	available	(*2)
	Over current protection(OCP)	Not available	Not available	available	(*2)

*1: normal mode means that CTLMAIN pin is "H" level and each DD CTL pin is "H" level

*2: This state is after each err detection. Error state will release, when the power supply voltage or CTLMAIN pin will turn off and on.

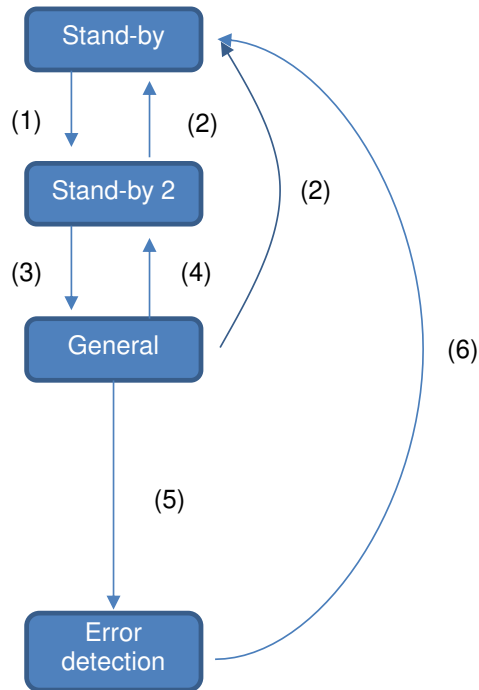
Priority of the External CTL Pin and I²C Communication

CTLMAIN (External)	CTL1, CTL2, CTL3, CTL4 (External)	30h Resistor (I ² C)	Relevant Channel
H	H	1	ON
H	H	0	ON
H	L	1	ON
H	L	0	OFF
L	X	disable	OFF

Notes:

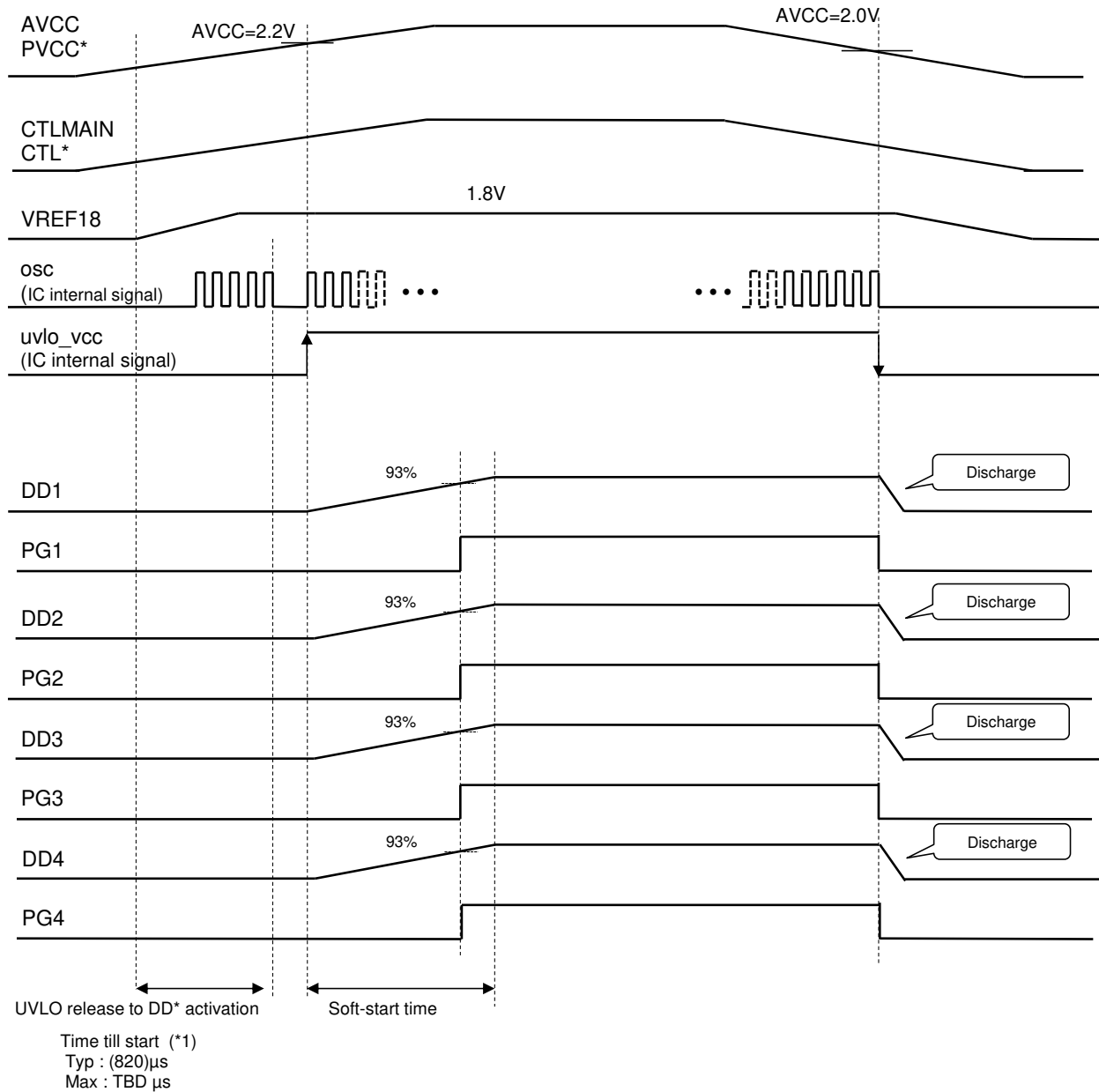
- The I²C communication is valid after the reference control block and digital block activation setting the external CTLMAIN pin to "H" level.
- Please attention below note about ON/OFF control of DD1, DD2, DD3, DD4 by I²C communication. When each DD control is turned off by I²C communication and external CTL pin remains "H" level, DCDC converter keep operating.

10. State Transition Diagram



- (1) External CTLMAIN pin is "H" level.
- (2) External CTLMAIN pin is "L" level.
- (3) External CTL pin or I²C communication "relevant CH_ON"
- (4) External CTL pin or I²C communication "relevant CH_OFF"
- (5) Error detection (TSD, OCP 1ms continuation)
- (6) Turning on the power supply again (equal to or less than uvlo_vcc rest voltage) or setting CTLMAIN to "L" level

11. Turning ON and OFF Sequence (AVCC=CTLMAIN, CTL1, CTL2, CTL3, CTL4)



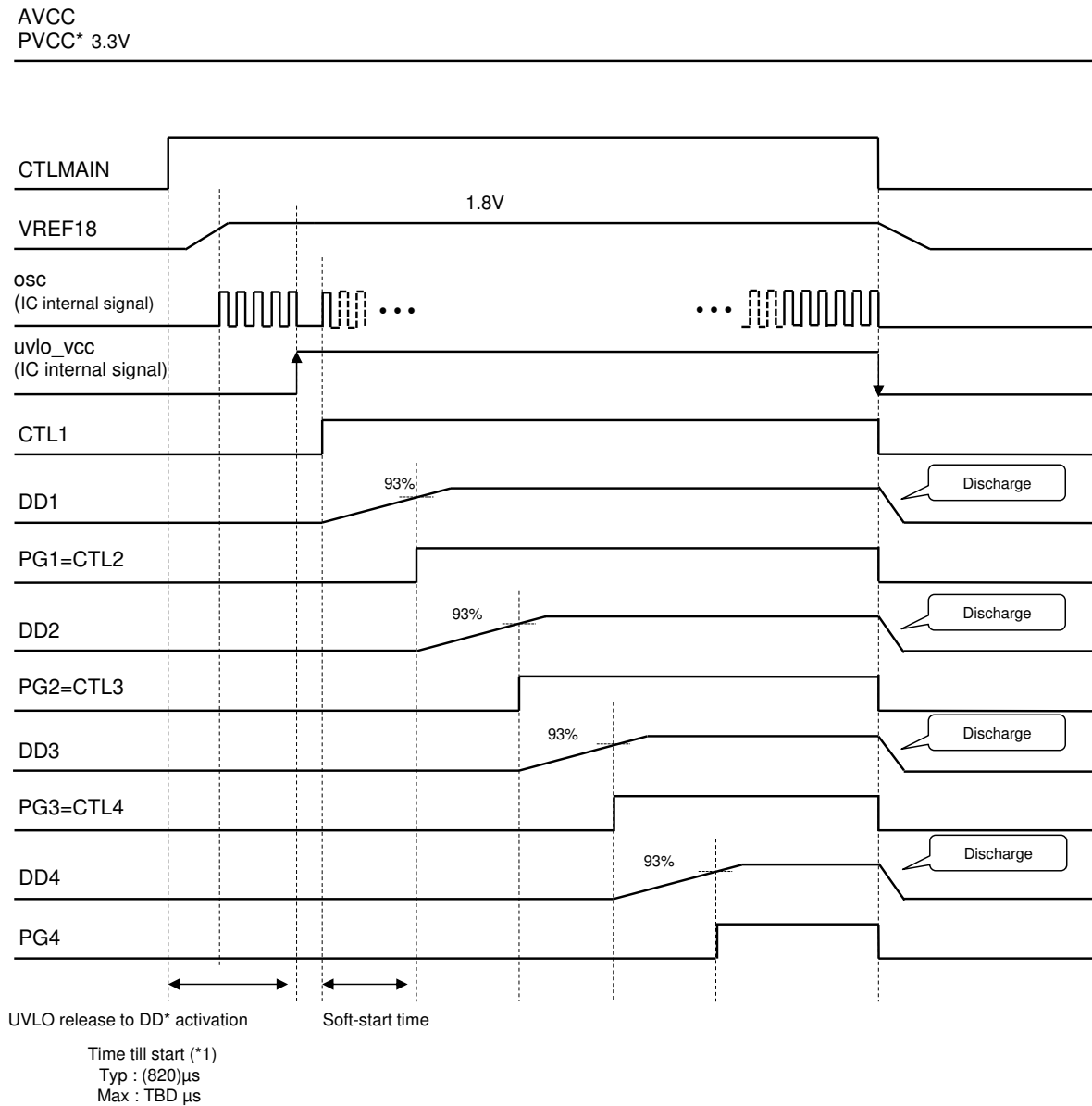
*1: PVCC1, PVCC2, PVCC3, PVCC4

*2: CTL1, CTL2, CTL3, CTL4

*3: DD1, DD2, DD3, DD4

*4: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0 μ F

12. Turning ON and OFF Sequence (AVCC → CTLMAIN → CTL1 → CTL2 → CTL3 → CTL4)

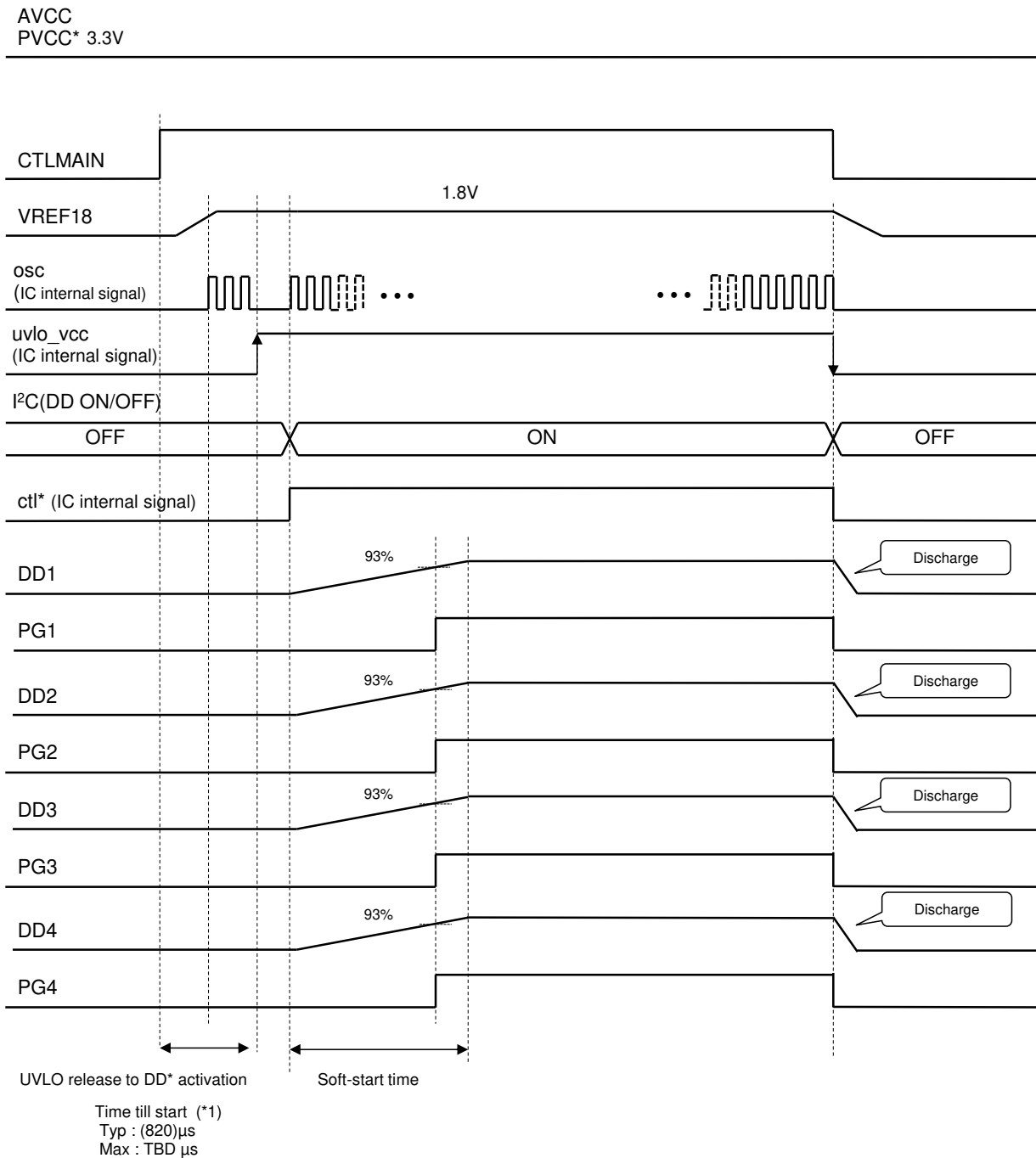


*1: PVCC1, PVCC2, PVCC3, PVCC4

*2: DD1, DD2, DD3, DD4

*3: VREF18 activations depend on the VREF18 pin capacitance.
Time in the sequence figure above is applied for the following condition.
VREF18 pin capacitance: 1.0μF

13. Turning ON and OFF Sequence (AVCC→CTLMAIN→I²C)



*1: PVCC1, PVCC2, PVCC3, PVCC4

*2: CTL1, CTL2, CTL3

*3: DD1, DD2, DD3

*4: VREF18 activations depend on the VREF18 pin capacitance.

Time in the sequence figure above is applied for the following condition.

VREF18 pin capacitance: 1.0μF

14. CTL Pin Threshold Voltage

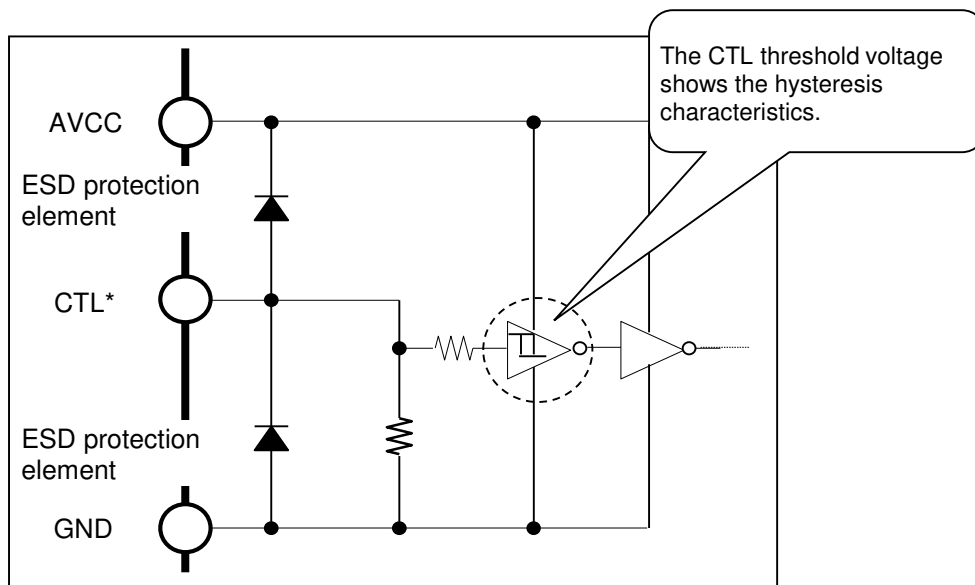
The input circuit structure for the CTL(*1) pin is the Schmitt trigger style, and the threshold voltage shows the hysteresis characteristics when CTL(*1) OFF to ON and ON to OFF.

(See "CTL (*1) Pin Equivalent Circuit Diagram" below.)

Also, the threshold voltage level depends on the VCC pin voltage.

Moreover, make sure to input either the "H" level ($>VCC \times 0.7V$) or "L" level ($<0.4V$) to the CTL(*1)pin when in use.

Figure 3. CTL (*1) Pin Equivalent Circuit Diagram



*1: CTLMAN, CTL1, CTL2, CTL3, CTL4

15. Protection Operation Sequence

Over Current Protection (DD channel)

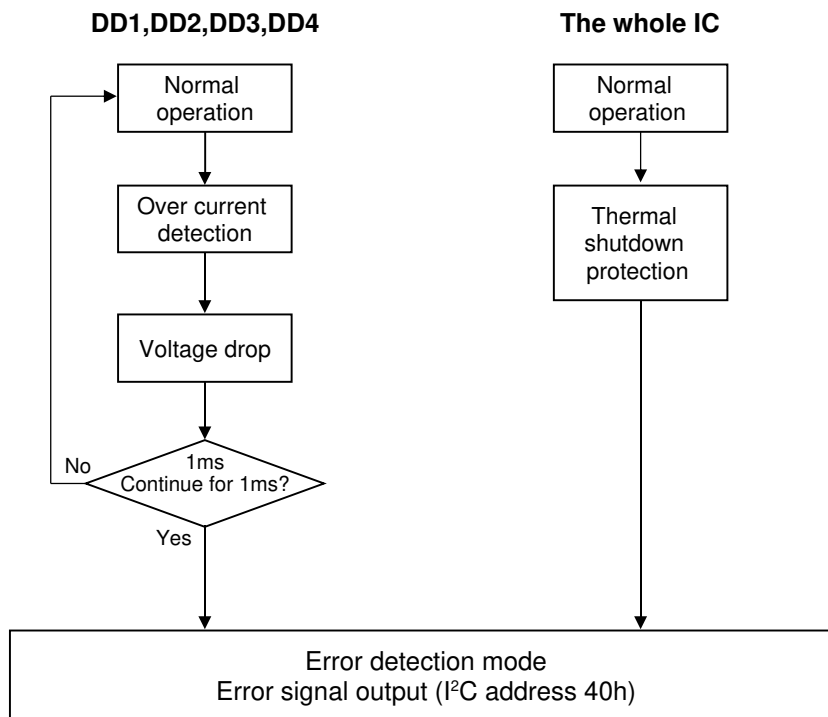
The DD channel monitors the peak current of FET at any time during the operation. When the DD output becomes the over current state, the output voltage is decreased. Afterward, the timer operation is performed and the output stops after about 1ms progress. When one of each DD channel stops operation by over current protection, all DD channels stop operation.

Thermal Shut Down

If the temperature at the junction part reaches +150°C, the thermal shutdown protection circuit turns all channels off.

Error Detection Sequence

Figure 4. Error Detection Sequence



Error Detection Mode Release

It is necessary to turn the power supply turning on again, or to turn CTLMAIN turning on again to release the error detection mode.