# Chipsmall

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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



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The S6E1C3 Series is a series of highly integrated 32-bit microcontrollers designed for embedded controllers aiming at low power consumption and low cost. This series has the ARM Cortex-M0+ Processor with on-chip Flash memory and SRAM, and consists of peripheral functions such as various timers, ADC and communication interfaces (UART, CSIO (SPI), I²C, I²S, Smart Card, and USB). The products which are described in this data sheet are placed into TYPE3-M0+ product categories in "FM0+ Family Peripheral Manual".

## Features

### 32-bit ARM Cortex-M0+ Core

■ Processor version: r0p1

■ Maximum operating frequency: 40.8 MHz

■ Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 24 peripheral interrupt with 4 selectable interrupt priority levels

■ 24-bit System timer (Sys Tick): System timer for OS task management

### Bit Band Operation
Compatible with Cortex-M3 bit band operation.

### On-Chip Memory

■ Flash memory
□ Up to 128 Kbytes
□ Read cycle: 0 wait-cycle
□ Security function for code protection

■ SRAM
The on-chip SRAM of this series has one independent SRAM .
□ Up to 16 Kbytes
□ 4Kbytes: can retain value in Deep standby Mode

### USB Interface
USB interface is composed of Device and Host
With Main PLL, USB clock can be generated by multiplication of Main clock.

■ USB Device
□ USB 2.0 Full-Speed supported
□ Max 6 EndPoint supported
  • EndPoint 0 is control transfer
  • EndPoint 1, 2 can be selected Bulk-transfer, Interrupt-transfer or Isochronous-transfer
  • EndPoint 3 to 5 can select Bulk-transfer or Interrupt-transfer
  • EndPoint 1 to 5 comprise Double Buffer
  • The size of each EndPoint is according to the follows
  • EndPoint 0, 2 to 5 : 64 bytes
  • EndPoint 1 : 256 bytes

■ USB host
□ USB 2.0 Full/Low-Speed supported

□ Bulk-transfer, Interrupt-transfer and Isochronous-transfer support
□ USB Device connected/disconnected automatically detect
□ IN/OUT token handshake packet automatically
□ Max 256-byte packet-length supported
□ Wake-up function supported

### Multi-Function Serial Interface (Max 6channels)

■ 3 channels with 64Byte FIFO (Ch.4, 6 and 7), 3 channels without FIFO (Ch.0, 1 and 3)

■ The operation mode of each channel can be selected from one of the following.
□ UART
□ CSIO (CSIO is known to many customers as SPI)
□ I²C

■ UART
□ Full duplex double buffer
□ Parity can be enabled or disabled.
□ Built-in dedicated baud rate generator
□ External clock available as a serial clock
□ Hardware Flow control* : Automatically control the transmission by CTS/RTS (only ch.4)
  * : S6E1C32B0A/S6E1C31B0A and S6E1C32C0A/S6E1C31C0A do not support Hardware Flow control.
□ Various error detection functions (parity errors, framing errors, and overrun errors)

■ CSIO (also known as SPI)
□ Full duplex double buffer
□ Built-in dedicated baud rate generator
□ Overrun error detection function
□ Serial chip select function (ch1 and ch6 only)
□ Data length: 5 to 16 bits

■ I²C
□ Standard-mode (Max: 100 kbps) supported / Fast-mode (Max 400 kbps) supported.

■ I²S (MFS-I2S)
□ Using CSIO (Max 2 ch: ch.4, ch.6) and I²S clock generator
□ Supports two transfer protocol
  • I²S
  • MSB-justified
□ Master mode only

## I2C Slave

■ I2C Slave supports the slave function of I2C and wake-up function from Standby mode.

## Descriptor System Data Transfer Controller (DSTC) (64 Channels)

■ The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor that has already been constructed on the memory, can access directly the memory / peripheral device and performs the data transfer operation.

■ It supports the software activation, the hardware activation, and the chain activation functions

## A/D Converter (Max: 8 Channels)

■ 12-bit A/D Converter
  □ Successive approximation type
  □ Conversion time: 2.0 µs @ 2.7 V to 3.6 V
  □ Priority conversion available (2 levels of priority)
  □ Scan conversion mode
  □ Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

## Base Timer (Max: 8 Channels)

The operation mode of each channel can be selected from one of the following.

■ 16-bit PWM timer

■ 16-bit PPG timer

■ 16/32-bit reload timer

■ 16/32-bit PWC timer

## General-Purpose I/O Port

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

■ All ports are Fast GPIO which can be accessed by 1cycle

■ Capable of controlling the pull-up of each pin

■ Capable of reading pin level directly

■ Port relocate function

■ Up to 54 fast general-purpose I/O ports @64-pin package

■ Certain ports are 5 V tolerant.
  See 4.List of Pin Functions and 5.I/O Circuit Typefor the corresponding pins.

## Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

■ Free-running mode

■ Periodic mode (= Reload mode)

■ One-shot mode

## Real-Time Clock

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 00 to year 99.

■ The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.

■ It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.

■ It can keep counting while rewriting the time.

■ It can count leap years automatically.

## Watch Counter

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

## External Interrupt Controller Unit

■ Up to 12 external interrupt input pins

■ Non-maskable interrupt (NMI) input pin: 1

## Watchdog Timer (2 Channels)

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

## CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

■ CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  □ CCITT CRC16 Generator Polynomial: 0x1021
  □ IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

## HDMI-CEC/Remote Control Receiver (Up to 2 Channels)

■ HDMI-CEC transmitter
  □ Header block automatic transmission by judging Signal free
  □ Generating status interrupt by detecting Arbitration lost

□ Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
□ Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)

■ HDMI-CEC receiver
□ Automatic ACK reply function available
□ Line error detection function available

■ Remote control receiver
□ 4 bytes reception buffer
□ Repeat code detection function available

## Smart Card Interface (Max 1 Channel)

■ Compliant with ISO7816-3 specification

■ Card Reader only/B class card only

■ Available protocols
□ Transmitter: 8E2, 8O2, 8N2
□ Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
□ Inverse mode

■ TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

## Clock and Reset

■ Clocks
A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

| | |
|---|---|
| □ Main clock: | 8 MHz to 48 MHz |
| □ Sub clock: | 32.768 kHz |
| □ Built-in high-speed CR clock: | 8 MHz |
| □ Built-in low-speed CR clock: | 100 kHz |
| □ Main PLL clock | 8MHz to 16MHz (Input), 75MHz to 150MHz (Output) |

■ Resets
□ Reset request from the INITX pin
□ Power on reset
□ Software reset
□ Watchdog timer reset
□ Low-voltage detection reset
□ Clock supervisor reset

## Clock Supervisor (CSV)
The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

■ If an external clock failure (clock stop) is detected, a reset is asserted.

■ If an external frequency anomaly is detected, an interrupt or a reset is asserted.

## Low-Voltage Detector (LVD)
This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

■ LVD1: monitor $V_{CC}$ and error reporting via an interrupt

■ LVD2: auto-reset operation

## Low Power Consumption Mode
This series has six low power consumption modes.

■ Sleep

■ Timer

■ RTC

■ Stop

■ Deep standby RTC (selectable between keeping the value of RAM and not)

■ Deep standby Stop (selectable between keeping the value of RAM and not)

## Peripheral Clock Gating
The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

## Debug

■ Serial Wire Debug Port (SW-DP)

■ Micro Trace Buffer (MTB)

## Unique ID
A 41-bit unique value of the device has been set.

## Power Supply

■ Wide voltage range:
VCC = 1.65V to 3.6 V
VCC = 3.0V to 3.6V (when USB is used)

# Table of Contents

# 1. Product Lineup

**Memory Size**

| Product name | S6E1C31B0A/<br>S6E1C31C0A/<br>S6E1C31D0A | S6E1C32B0A/<br>S6E1C32C0A/<br>S6E1C32D0A |
|---|---|---|
| On-chip Flash memory | 64 Kbytes | 128 Kbytes |
| On-chip SRAM | 12 Kbytes | 16 Kbytes |

**Function**

| Product name | S6E1C32B0A<br>(WLCSP) | S6E1C32B0A/<br>S6E1C31B0A | S6E1C32C0A/<br>S6E1C32C0A | S6E1C31D0A/<br>S6E1C32D0A |
|---|---|---|---|---|
| Pin count | TBD | 32 | 48 | 64 |
| CPU | Cortex-M0+ | | | |
|    Frequency | 40.8 MHz | | | |
| Power supply voltage range | 1.65 V to 3.6 V | | | |
| USB2.0 (Device/Host) | 1 unit | | | |
| DSTC | 64 ch. | | | |
| Multi-function Serial Interface (UART/CSIO/I²C/I2S) | 2 ch. (Max)<br>Ch.0/3 without FIFO | 4 ch. (Max)<br>Ch.0/1/3 without FIFO<br>Ch. 6 with FIFO | 6 ch. (Max)<br>Ch.0/1/3 without FIFO<br>Ch.4/6/7 with FIFO | 6 ch. (Max)<br>Ch.0/1/3 without FIFO<br>Ch.4/6/7 with FIFO |
| | I2S : No | | I2S : 1 ch (Max)<br>Ch. 6 with FIFO | I2S : 2 ch (Max)<br>Ch. 4/6 with FIFO |
| Base Timer (PWC/Reload timer/PWM/PPG) | 8 ch. (Max) | | | |
| Dual Timer | 1 unit | | | |
| HDMI-CEC/ Remote Control Receiver | 1 ch.(Max)<br>Ch.1 | | 2 ch (Max)<br>Ch.0/1 | |
| I2C Slave | No | 1 ch (Max) | | |
| Smart Card Interface | No | | | 1 ch (Max) |
| Real-time Clock | 1 unit | | | |
| Watch Counter | 1 unit | | | |
| CRC Accelerator | Yes | | | |
| Watchdog timer | 1 ch. (SW) + 1 ch. (HW) | | | |
| External Interrupt | 5 pins (Max),<br>NMI × 1 | 7 pins (Max),<br>NMI x 1 | 9 pins (Max),<br>NMI x 1 | 12 pins (Max),<br>NMI x 1 |
| I/O port | 20 pins (Max) | 24 pins (Max) | 38 pins (Max) | 54 pins (Max) |
| 12-bit A/D converter | 4 ch (1 unit) | 6 ch. (1 unit) | 8 ch. (1 unit) | 8 ch. (1 unit) |
| CSV (Clock Supervisor) | Yes | | | |
| LVD (Low-voltage Detection) | 2 ch. | | | |
| Built-in CR  High-speed | 8 MHz (Typ) | | | |
|     Low-speed | 100 kHz (Typ) | | | |
| Debug Function | SW-DP | | | |
| Unique ID | Yes | | | |

**Note:**

− All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
See "11. Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

## 2. Packages

| Product name / Package | S6E1C32B0A (WLCSP) | S6E1C32B0A/ S6E1C31B0A | S6E1C32C0A/ S6E1C31C0A | S6E1C32D0A/ S6E1C31D0A |
|---|---|---|---|---|
| WLCSP (TBD) | ○ | | - | - |
| LQFP: FPT-32P-M30 (0.80 mm pitch) | - | ○ | - | - |
| QFN: LCC-32P-M73 (0.50 mm pitch) | | ○ | | |
| LQFP: FPT-48P-M49 (0.50 mm pitch) | - | - | ○ | - |
| QFN: LCC-48P-M74 (0.50 mm pitch) | - | - | ○ | - |
| LQFP: FPT-64P-M38 (0.50 mm pitch) | - | - | - | ○ |
| QFN: LCC-64P-M25 (0.50 mm pitch) | - | - | - | ○ |

○: Available

*Note:*

− *See "13. Package Dimensions" for detailed information on each package.*

## 3. Pin Assignment

FPT-64P-M38



(TOP VIEW)

LQFP - 64

**Left side (pins 1–16):**

| Pin | Name |
|---|---|
| 1 | P50/SIN3_1/INT00_0 |
| 2 | P51/SOT3_1/INT01_0 |
| 3 | P52/SCK3_1/INT02_0 |
| 4 | P53/TIOA1_2/INT07_2 |
| 5 | P30/SCS60_1/TIOB0_1/INT03_2/MI2SWS6_1 |
| 6 | P31/SCK6_1/SI2CSCL6_1/INT04_2/MI2SCK6_1 |
| 7 | P32/SOT6_1/SI2CSDA6_1/TIOB2_1/INT05_2/MI2SDO6_1 |
| 8 | P33/ADTG_6/SIN6_1/INT04_0/MI2SDI6_1 |
| 9 | P34/SCS61_1/TIOB4_1/MI2SMCK6_1 |
| 10 | P35/SCS62_1/TIOB5_1/INT08_1 |
| 11 | P3A/TIOA0_1/INT03_0/RTCCO_2/SUBOUT_2/IC1_CIN_0 |
| 12 | P3B/TIOA1_1/IC1_DATA_0 |
| 13 | P3C/TIOA2_1/IC1_RST_0 |
| 14 | P3D/TIOA3_1/IC1_VPEN_0 |
| 15 | P3E/TIOA4_1/IC1_VCC_0 |
| 16 | P3F/TIOA5_1/IC1_CLK_0 |

**Top side (pins 64–49):**

| Pin | Name |
|---|---|
| 64 | P0F/NMIX/WKUP0/RTCCO_0/SUBOUT_0/CROUT_1 |
| 63 | P0C/TIOA6_1/WKUP7 |
| 62 | P0B/TIOB6_1/WKUP6 |
| 61 | P61/UHCONX0/TIOB2_2 |
| 60 | VSS |
| 59 | P81/UDP0 |
| 58 | P80/UDM0 |
| 57 | VCC |
| 56 | P05/MD1/TIOA5_2/INT00_1/WKUP3 |
| 55 | P03/SWDIO/SIN0_0/TIOB7_0 |
| 54 | P02/WKUP5 |
| 53 | P01/SWCLK/SOT0_0 |
| 52 | P00/WKUP4 |
| 51 | P21/INT06_1/WKUP2 |
| 50 | AVRL |
| 49 | AVRH |

**Right side (pins 48–33):**

| Pin | Name |
|---|---|
| 48 | VCC |
| 47 | P22/AN07/TIOB7_1 |
| 46 | P23/AN06/SCK0_0/TIOA7_1 |
| 45 | P15/AN05/SOT0_1/SCS11_1 |
| 44 | P14/AN04/SIN0_1/SCS10_1/INT03_1 |
| 43 | P13/AN03/SCK1_1/RTCCO_1/SUBOUT_1 |
| 42 | P12/AN02/SOT1_1 |
| 41 | P11/AN01/SIN1_1/INT02_1/WKUP1 |
| 40 | P10/AN00 |
| 39 | P1F/ADTG_5 |
| 38 | P1A/SIN4_1/INT05_1/CEC0_0/MI2SDI4_1 |
| 37 | P1B/SOT4_1/MI2SDO4_1 |
| 36 | P1C/SCK4_1/MI2SCK4_1 |
| 35 | P1D/CTS4_1/MI2SWS4_1 |
| 34 | P1E/RTS4_1/MI2SMCK4_1 |
| 33 | P60/TIOA2_2/INT15_1/CEC1_0 |

**Bottom side (pins 17–32):**

| Pin | Name |
|---|---|
| 17 | MD0 |
| 18 | PE2/X0 |
| 19 | PE3/X1 |
| 20 | P40/TIOA0_0/INT12_1 |
| 21 | P41/TIOA1_0/INT13_1 |
| 22 | P42/TIOA2_0 |
| 23 | P43/ADTG_7/TIOA3_0 |
| 24 | P4C/SCK7_1/TIOB3_0 |
| 25 | P4D/SOT7_1 |
| 26 | P4E/SIN7_1/INT06_2 |
| 27 | VCC |
| 28 | C |
| 29 | VSS |
| 30 | P46/X0A |
| 31 | P47/X1A |
| 32 | INITX |

Note:

− The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

**LCC-64P-M25**

(TOP VIEW)

Top pins (64–49):

- 64 P0F/NMIX/WKUP0/RTCCO_0/SUBOUT_0/CROUT_1
- 63 P0C/TIOA6_1/WKUP7
- 62 P0B/TIOB6_1/WKUP6
- 61 P61/UHCONX0/TIOB2_2
- 60 VSS
- 59 P81/UDP0
- 58 P80/UDM0
- 57 VCC
- 56 P05/MD1/TIOA5_2/INT00_1/WKUP3
- 55 P03/SWDIO/SIN0_0/TIOB7_0
- 54 P02/WKUP5
- 53 P01/SWCLK/SOT0_0
- 52 P00/WKUP4
- 51 P21/INT06_1/WKUP2
- 50 AVRL
- 49 AVRH

Left pins (1–16):

- P50/SIN3_1/INT00_0 — 1
- P51/SOT3_1/INT01_0 — 2
- P52/SCK3_1/INT02_0 — 3
- P53/TIOA1_2/INT07_2 — 4
- P30/SCS60_1/TIOB0_1/INT03_2/MI2SWS6_1 — 5
- P31/SCK6_1/SI2CSCL6_1/INT04_2/MI2SCK6_1 — 6
- P32/SOT6_1/SI2CSDA6_1/TIOB2_1/INT05_2/MI2SDO6_1 — 7
- P33/ADTG_6/SIN6_1/INT04_0/MI2SDI6_1 — 8
- P34/SCS61_1/TIOB4_1/MI2SMCK6_1 — 9
- P35/SCS62_1/TIOB5_1/INT08_1 — 10
- P3A/TIOA0_1/INT03_0/RTCCO_2/SUBOUT_2/IC1_CIN_0 — 11
- P3B/TIOA1_1/IC1_DATA_0 — 12
- P3C/TIOA2_1/IC1_RST_0 — 13
- P3D/TIOA3_1/IC1_VPEN_0 — 14
- P3E/TIOA4_1/IC1_VCC_0 — 15
- P3F/TIOA5_1/IC1_CLK_0 — 16

**QFN – 64**

Right pins (48–33):

- 48 VCC
- 47 P22/AN07/TIOB7_1
- 46 P23/AN06/SCK0_0/TIOA7_1
- 45 P15/AN05/SOT0_1/SCS11_1
- 44 P14/AN04/SIN0_1/SCS10_1/INT03_1
- 43 P13/AN03/SCK1_1/RTCCO_1/SUBOUT_1
- 42 P12/AN02/SOT1_1
- 41 P11/AN01/SIN1_1/INT02_1/WKUP1
- 40 P10/AN00
- 39 P1F/ADTG_5
- 38 P1A/SIN4_1/INT05_1/CEC0_0/MI2SDI4_1
- 37 P1B/SOT4_1/MI2SDO4_1
- 36 P1C/SCK4_1/MI2SCK4_1
- 35 P1D/CTS4_1/MI2SWS4_1
- 34 P1E/RTS4_1/MI2SMCK4_1
- 33 P60/TIOA2_2/INT15_1/CEC1_0

Bottom pins (17–32):

- 17 MD0
- 18 PE2/X0
- 19 PE3/X1
- 20 P40/TIOA0_0/INT12_1
- 21 P41/TIOA1_0/INT13_1
- 22 P42/TIOA2_0
- 23 P43/ADTG_7/TIOA3_0
- 24 P4C/SCK7_1/TIOB3_0
- 25 P4D/SOT7_1
- 26 P4E/SIN7_1/INT06_2
- 27 VCC
- 28 C
- 29 VSS
- 30 P46/X0A
- 31 P47/X1A
- 32 INITX

**Note:**

− The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

**FPT-48P-M49**

(TOP VIEW)



LQFP – 48

Top pins (48–37):
- 48: P0F/NMIX/WKUP0/RTCCO_0/SUBOUT_0/CROUT_1
- 47: P61/UHCONX0/TIOB2_2
- 46: VSS
- 45: P81/UDP0
- 44: P80/UDM0
- 43: VCC
- 42: P05/MD1/TIOA5_2/INT00_1/WKUP3
- 41: P03/SWDIO/SIN0_0/TIOB7_0
- 40: P01/SWCLK/SOT0_0
- 39: P21/INT06_1/WKUP2
- 38: AVRL
- 37: AVRH

Left pins (1–12):
- 1: P50/SIN3_1/INT00_0
- 2: P51/SOT3_1/INT01_0
- 3: P52/SCK3_1/INT02_0
- 4: P53/TIOA1_2/INT07_2
- 5: P30/SCS60_1/TIOB0_1/INT03_2/MI2SWS6_1
- 6: P31/SCK6_1/SI2CSCL6_1/INT04_2/MI2SCK6_1
- 7: P32/SOT6_1/SI2CSDA6_1/TIOB2_1/INT05_2/MI2SDO6_1
- 8: P33/ADTG_6/SIN6_1/INT04_0/MI2SDI6_1
- 9: P34/SCS61_1/MI2SMCK6_1
- 10: P3A/TIOA0_1/INT03_0/RTCCO_2/SUBOUT_2
- 11: P3B/TIOA1_1
- 12: P3C/TIOA2_1

Right pins (36–25):
- 36: VCC
- 35: P22/AN07/TIOB7_1
- 34: P23/AN06/SCK0_0/TIOA7_1
- 33: P15/AN05/SOT0_1/SCS11_1
- 32: P14/AN04/SIN0_1/SCS10_1/INT03_1
- 31: P13/AN03/SCK1_1/RTCCO_1/SUBOUT_1
- 30: P12/AN02/SOT1_1
- 29: P11/AN01/SIN1_1/INT02_1/WKUP1
- 28: P10/AN00
- 27: P1A/SIN4_1/INT05_1/CEC0_0
- 26: P1B/SOT4_1
- 25: P60/TIOA2_2/INT15_1/CEC1_0

Bottom pins (13–24):
- 13: MD0
- 14: PE2/X0
- 15: PE3/X1
- 16: P4C/SCK7_1
- 17: P4D/SOT7_1
- 18: P4E/SIN7_1/INT06_2
- 19: VCC
- 20: C
- 21: VSS
- 22: P46/X0A
- 23: P47/X1A
- 24: INITX

**Note:**

− The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

**LCC-48P-M74**

(TOP VIEW)

QFN – 48

Top pins (48–37):
- 48: P0F/NMIX/WKUP0/RTCCO_0/SUBOUT_0/CROUT_1
- 47: P61/UHCONX0/TIOB2_2
- 46: VSS
- 45: P81/UDP0
- 44: P80/UDM0
- 43: VCC
- 42: P05/MD1/TIOA5_2/INT00_1/WKUP3
- 41: P03/SWDIO/SIN0_0/TIOB7_0
- 40: P01/SWCLK/SOT0_0
- 39: P21/INT06_1/WKUP2
- 38: AVRL
- 37: AVRH

Left pins (1–12):
- 1: P50/SIN3_1/INT00_0
- 2: P51/SOT3_1/INT01_0
- 3: P52/SCK3_1/INT02_0
- 4: P53/TIOA1_2/INT07_2
- 5: P30/SCS60_1/TIOB0_1/INT03_2/MI2SWS6_1
- 6: P31/SCK6_1/SI2CSCL6_1/INT04_2/MI2SCK6_1
- 7: P32/SOT6_1/SI2CSDA6_1/TIOB2_1/INT05_2/MI2SDO6_1
- 8: P33/ADTG_6/SIN6_1/INT04_0/MI2SDI6_1
- 9: P34/SCS61_1/MI2SMCK6_1
- 10: P3A/TIOA0_1/INT03_0/RTCCO_2/SUBOUT_2
- 11: P3B/TIOA1_1
- 12: P3C/TIOA2_1

Right pins (36–25):
- 36: VCC
- 35: P22/AN07/TIOB7_1
- 34: P23/AN06/SCK0_0/TIOA7_1
- 33: P15/AN05/SOT0_1/SCS11_1
- 32: P14/AN04/SIN0_1/SCS10_1/INT03_1
- 31: P13/AN03/SCK1_1/RTCCO_1/SUBOUT_1
- 30: P12/AN02/SOT1_1
- 29: P11/AN01/SIN1_1/INT02_1/WKUP1
- 28: P10/AN00
- 27: P1A/SIN4_1/INT05_1/CEC0_0
- 26: P1B/SOT4_1
- 25: P60/TIOA2_2/INT15_1/CEC1_0

Bottom pins (13–24):
- 13: MD0
- 14: PE2/X0
- 15: PE3/X1
- 16: P4C/SCK7_1
- 17: P4D/SOT7_1
- 18: P4E/SIN7_1/INT06_2
- 19: VCC
- 20: C
- 21: VSS
- 22: P46/X0A
- 23: P47/X1A
- 24: INITX

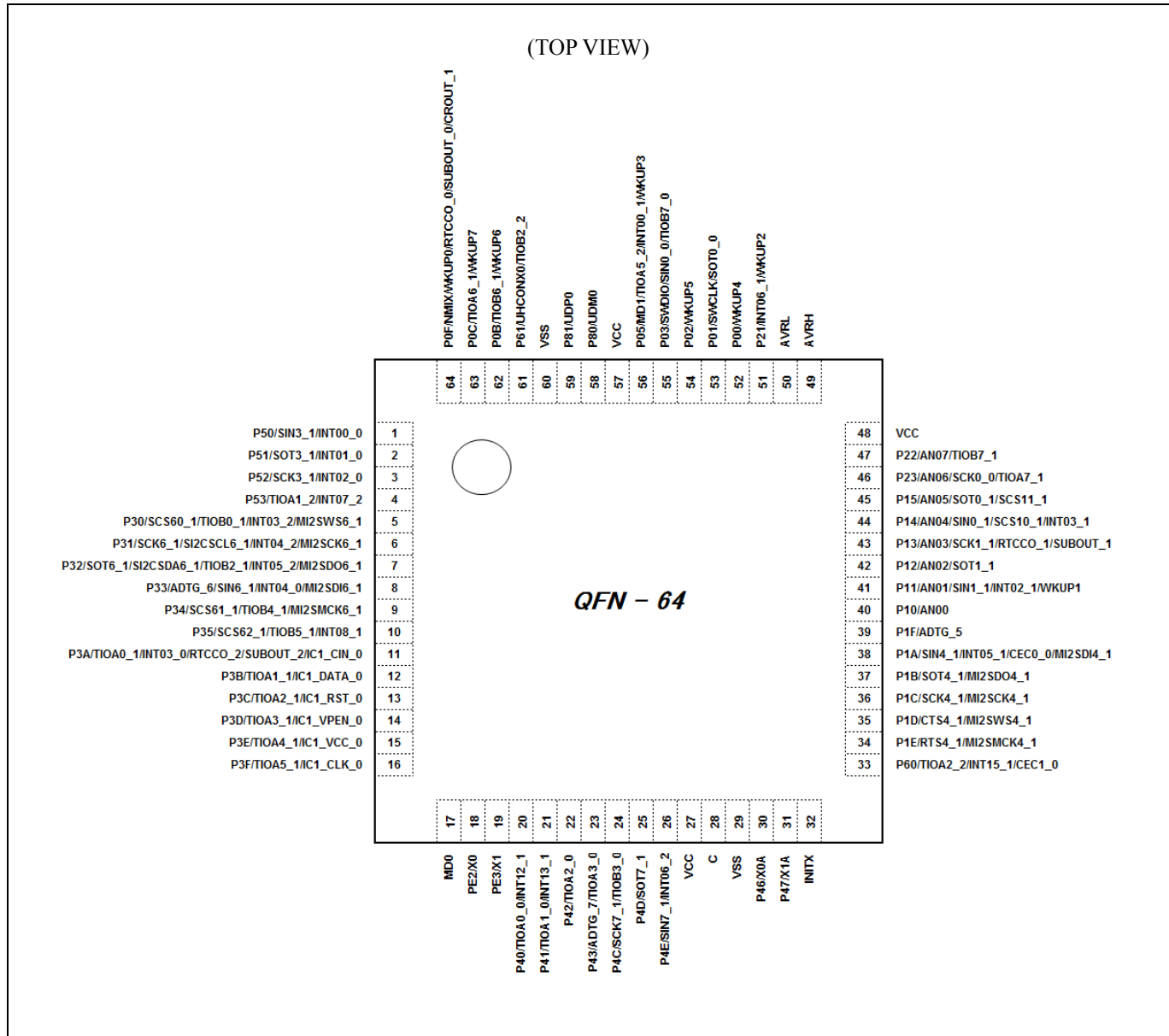**Note:**

- The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.
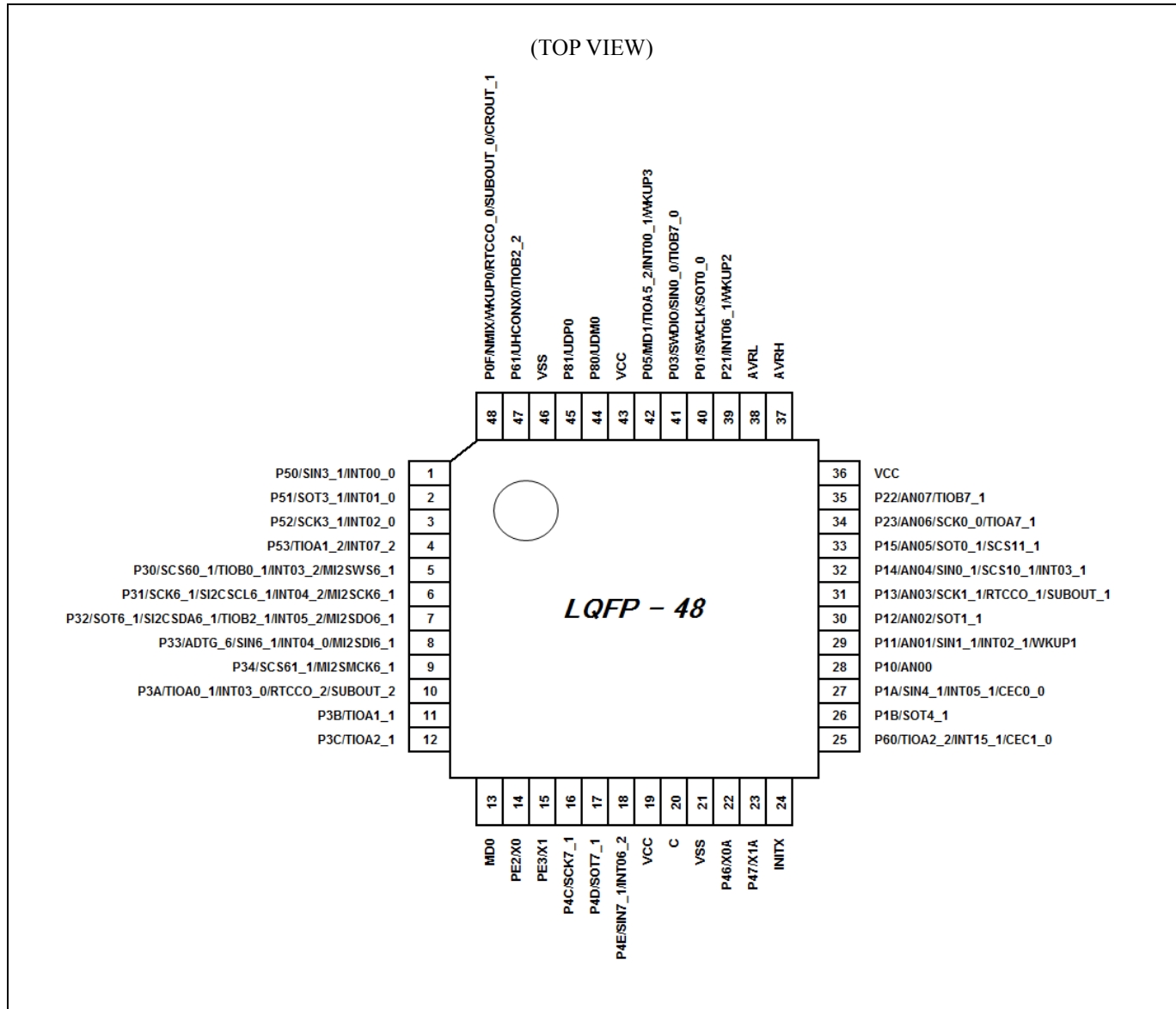
**FPT-32P-M30**

(TOP VIEW)



P0F/NMIX/WKUP0/RTCCO_0/SUBOUT_0/CROUT_1 — 1    24 — VCC

P50/SIN3_1/INT00_0 — 2    23 — P22/AN07/TIOB7_1

P51/SOT3_1/INT01_0 — 3    22 — P23/AN06/SCK0_0/TIOA7_1

P52/SCK3_1/INT02_0 — 4    21 — P13/AN03/SCK1_1/RTCCO_1/SUBOUT_1

P31/SCK6_1/SI2CSCL6_1/INT04_2 — 5    20 — P12/AN02/SOT1_1

P32/SOT6_1/SI2CSDA6_1/TIOB2_1/INT05_2 — 6    19 — P11/AN01/SIN1_1/INT02_1/WKUP1

P33/ADTG_6/SIN6_1/INT04_0 — 7    18 — P10/AN00

MD0 — 8    17 — P60/TIOA2_2/INT15_1/CEC1_0

LQFP – 32

Top pins (32–25): VSS, P81/UDP0, P80/UDM0, P05/MD1/TIOA5_2/INT00_1/WKUP3, P03/SWDIO/SIN0_0/TIOB7_0, P01/SWCLK/SOT0_0, P21/INT06_1/WKUP2, AVRL

Bottom pins (9–16): PE2/X0, PE3/X1, VCC, C, VSS, P46/X0A, P47/X1A, INITX

*Note:*

− *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*
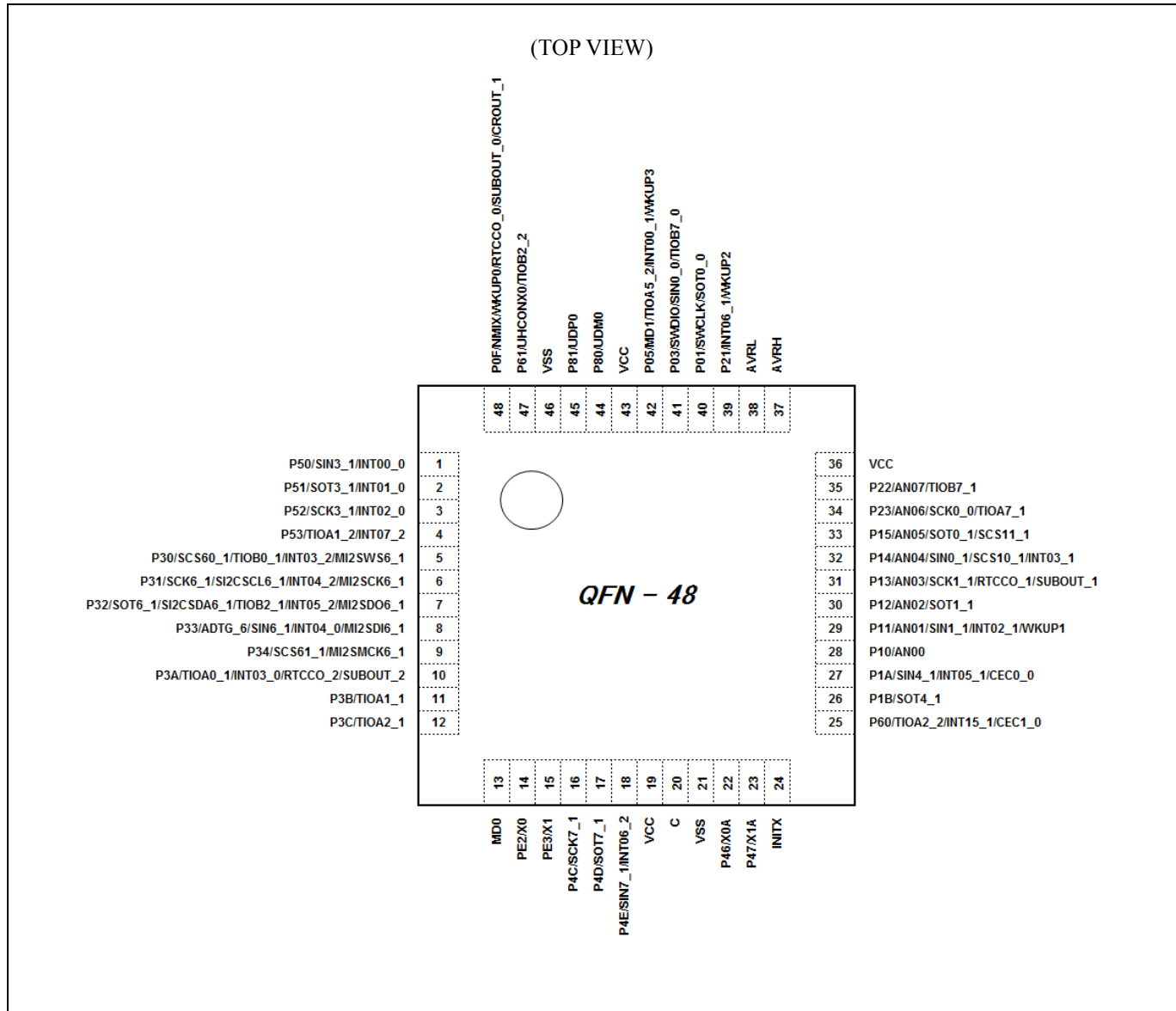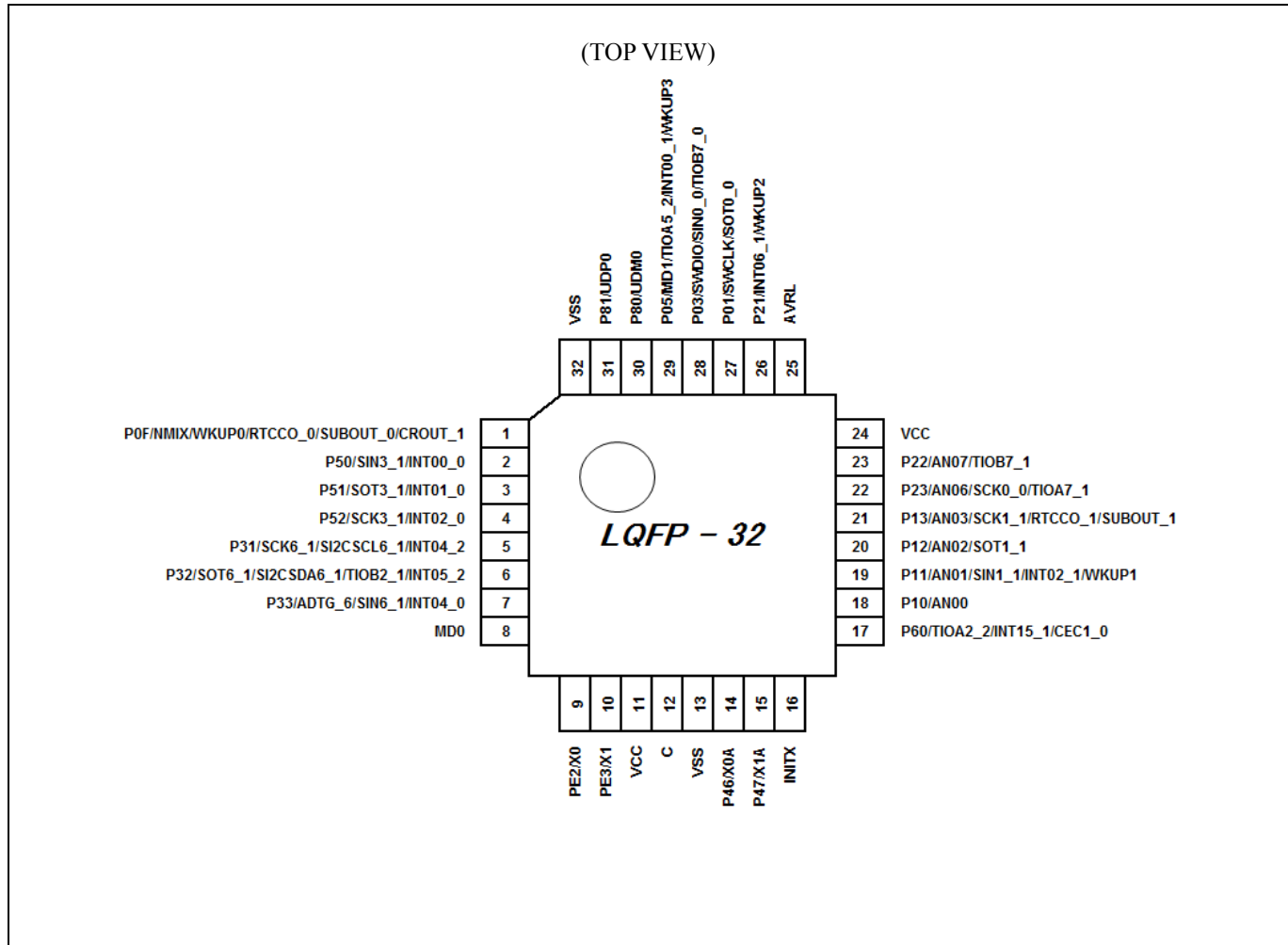
**LCC-32P-M73**

(TOP VIEW)

QFN – 32

Pin assignments (pins along the top, numbered 32 to 25):

| Pin | Name |
|-----|------|
| 32 | VSS |
| 31 | P81/UDP0 |
| 30 | P80/UDM0 |
| 29 | P05/MD1/TIOA5_2/INT00_1/WKUP3 |
| 28 | P03/SWDIO/SIN0_0/TIOB7_0 |
| 27 | P01/SWCLK/SOT0_0 |
| 26 | P21/INT06_1/WKUP2 |
| 25 | AVRL |

Left side pins (numbered 1 to 8):

| Pin | Name |
|-----|------|
| 1 | P0F/NMIX/WKUP0/RTCCO_0/SUBOUT_0/CROUT_1 |
| 2 | P50/SIN3_1/INT00_0 |
| 3 | P51/SOT3_1/INT01_0 |
| 4 | P52/SCK3_1/INT02_0 |
| 5 | P31/SCK6_1/SI2CSCL6_1/INT04_2 |
| 6 | P32/SOT6_1/SI2CSDA6_1/TIOB2_1/INT05_2 |
| 7 | P33/ADTG_6/SIN6_1/INT04_0 |
| 8 | MD0 |

Right side pins (numbered 24 to 17):

| Pin | Name |
|-----|------|
| 24 | VCC |
| 23 | P22/AN07/TIOB7_1 |
| 22 | P23/AN06/SCK0_0/TIOA7_1 |
| 21 | P13/AN03/SCK1_1/RTCCO_1/SUBOUT_1 |
| 20 | P12/AN02/SOT1_1 |
| 19 | P11/AN01/SIN1_1/INT02_1/WKUP1 |
| 18 | P10/AN00 |
| 17 | P60/TIOA2_2/INT15_1/CEC1_0 |

Bottom pins (numbered 9 to 16):

| Pin | Name |
|-----|------|
| 9 | PE2/X0 |
| 10 | PE3/X1 |
| 11 | VCC |
| 12 | C |
| 13 | VSS |
| 14 | P46/X0A |
| 15 | P47/X1A |
| 16 | INITX |

*Note:*

− *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*
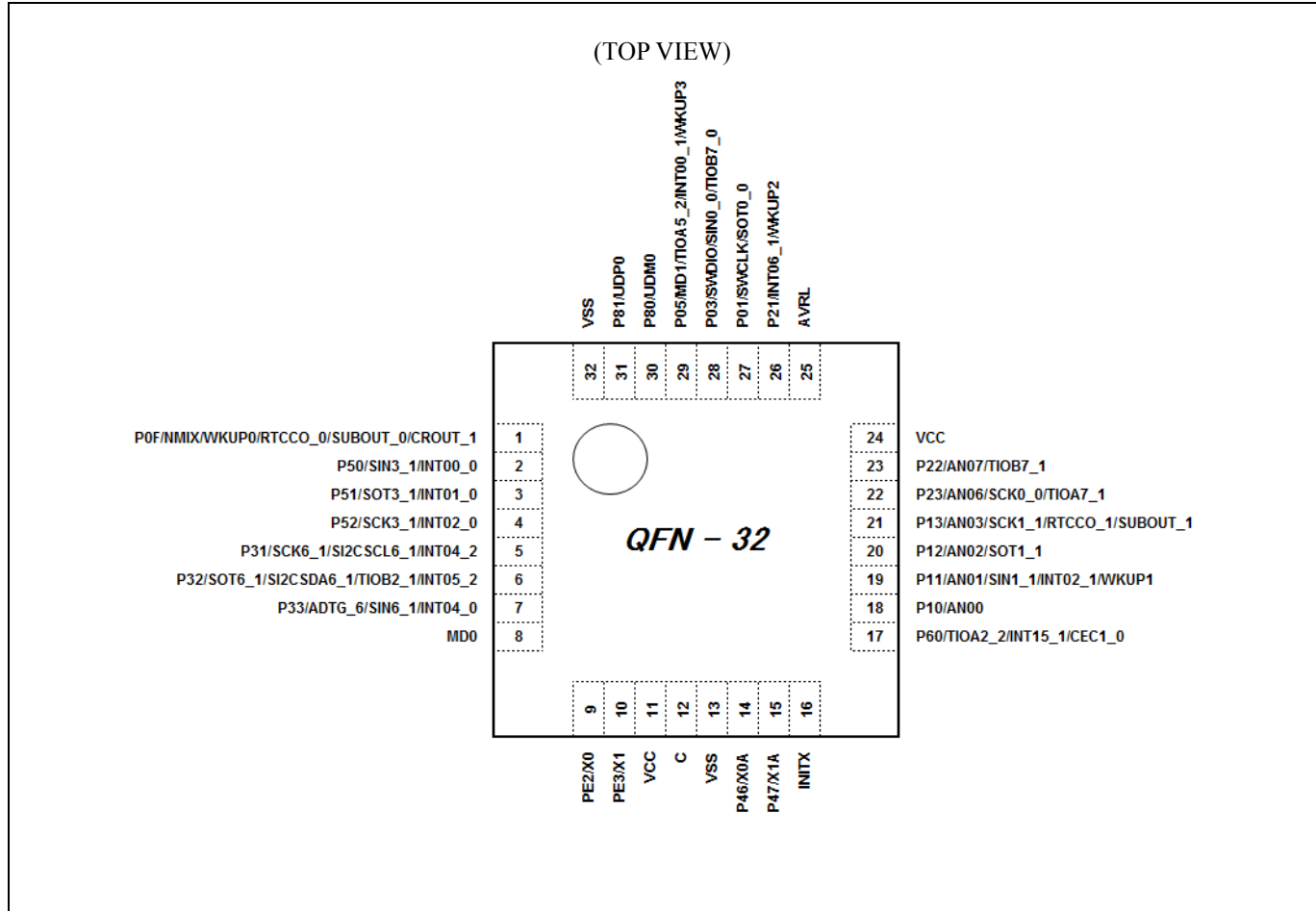
**WLCSP**

TBD

*Note:*

− *The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.*

# 4. List of Pin Functions

**List of Pin Numbers**

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

| Pin no. | | | | Pin Function | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|
| LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) | | | |
| 1 | 1 | 2 | - | P50 | D | K |
| | | | | SIN3_1 | | |
| | | | | INT00_0 | | |
| 2 | 2 | 3 | - | P51 | D | K |
| | | | | SOT3_1 | | |
| | | | | INT01_0 | | |
| 3 | 3 | 4 | - | P52 | D | K |
| | | | | SCK3_1 | | |
| | | | | INT02_0 | | |
| 4 | 4 | - | - | P53 | D | K |
| | | | | TIOA1_2 | | |
| | | | | INT07_2 | | |
| 5 | 5 | - | - | P30 | D | K |
| | | | | SCS60_1 | | |
| | | | | TIOB0_1 | | |
| | | | | INT03_2 | | |
| | | | | MI2SWS6_1 | | |
| 6 | 6 | - | - | P31 | H | K |
| | | | | SCK6_1 | | |
| | | | | SI2CSCL6_1 | | |
| | | | | INT04_2 | | |
| | | | | MI2SCK6_1 | | |
| - | - | 5 | - | P31 | H | K |
| | | | | SCK6_1 | | |
| | | | | SI2CSCL6_1 | | |
| | | | | INT04_2 | | |
| 7 | 7 | - | - | P32 | H | K |
| | | | | SOT6_1 | | |
| | | | | SI2CSDA6_1 | | |
| | | | | TIOB2_1 | | |
| | | | | INT05_2 | | |
| | | | | MI2SDO6_1 | | |
| - | - | 6 | - | P32 | H | K |
| | | | | SOT6_1 | | |
| | | | | SI2CSDA6_1 | | |
| | | | | TIOB2_1 | | |
| | | | | INT05_2 | | |

| Pin no. | | | | Pin Function | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|
| **LQFP-64 QFN-64** | **LQFP-48 QFN-48** | **LQFP-32 QFN-32** | **WLCSP (TBD)** | | | |
| 8 | 8 | - | - | P33 | H | K |
| | | | | ADTG_6 | | |
| | | | | SIN6_1 | | |
| | | | | INT04_0 | | |
| | | | | MI2SDI6_1 | | |
| - | - | 7 | - | P33 | H | K |
| | | | | ADTG_6 | | |
| | | | | SIN6_1 | | |
| | | | | INT04_0 | | |
| 9 | - | - | - | P34 | D | K |
| | | | | SCS61_1 | | |
| | | | | TIOB4_1 | | |
| | | | | MI2SMCK6_1 | | |
| - | 9 | - | - | P34 | D | K |
| | | | | SCS61_1 | | |
| | | | | MI2SMCK6_1 | | |
| 10 | - | - | - | P35 | D | K |
| | | | | SCS62_1 | | |
| | | | | TIOB5_1 | | |
| | | | | INT08_1 | | |
| 11 | - | - | - | P3A | D | K |
| | | | | TIOA0_1 | | |
| | | | | INT03_0 | | |
| | | | | RTCCO_2 | | |
| | | | | SUBOUT_2 | | |
| | | | | IC1_CIN_0 | | |
| - | 10 | - | - | P3A | D | K |
| | | | | TIOA0_1 | | |
| | | | | INT03_0 | | |
| | | | | RTCCO_2 | | |
| | | | | SUBOUT_2 | | |
| 12 | - | - | - | P3B | D | K |
| | | | | TIOA1_1 | | |
| | | | | IC1_DATA_0 | | |
| - | 11 | - | - | P3B | D | K |
| | | | | TIOA1_1 | | |
| 13 | - | - | - | P3C | D | K |
| | | | | TIOA2_1 | | |
| | | | | IC1_RST_0 | | |
| - | 12 | - | - | P3C | D | K |
| | | | | TIOA2_1 | | |
| 14 | - | - | - | P3D | D | K |
| | | | | TIOA3_1 | | |
| | | | | IC1_VPEN_0 | | |

| Pin no. | | | | Pin Function | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|
| **LQFP-64 QFN-64** | **LQFP-48 QFN-48** | **LQFP-32 QFN-32** | **WLCSP (TBD)** | | | |
| 15 | - | - | - | P3E | D | K |
| | | | | TIOA4_1 | | |
| | | | | IC1_VCC_0 | | |
| 16 | - | - | - | P3F | D | K |
| | | | | TIOA5_1 | | |
| | | | | IC1_CLK_0 | | |
| 17 | 13 | 8 | - | MD0 | I | F |
| 18 | 14 | 9 | - | PE2 | A | A |
| | | | | X0 | | |
| 19 | 15 | 10 | - | PE3 | A | B |
| | | | | X1 | | |
| 20 | - | - | - | P40 | D | K |
| | | | | TIOA0_0 | | |
| | | | | INT12_1 | | |
| 21 | - | - | - | P41 | D | K |
| | | | | TIOA1_0 | | |
| | | | | INT13_1 | | |
| 22 | - | - | - | P42 | D | K |
| | | | | TIOA2_0 | | |
| 23 | - | - | - | P43 | D | K |
| | | | | ADTG_7 | | |
| | | | | TIOA3_0 | | |
| 24 | - | - | - | P4C | D | K |
| | | | | SCK7_1 | | |
| | | | | TIOB3_0 | | |
| - | 16 | - | - | P4C | D | K |
| | | | | SCK7_1 | | |
| 25 | 17 | - | - | P4D | D | K |
| | | | | SOT7_1 | | |
| 26 | 18 | - | - | P4E | D | K |
| | | | | SIN7_1 | | |
| | | | | INT06_2 | | |
| 27 | 19 | 11 | - | VCC | - | - |
| 28 | 20 | 12 | - | C | - | - |
| 29 | 21 | 13 | - | VSS | - | - |
| 30 | 22 | 14 | - | P46 | C | C |
| | | | | X0A | | |
| 31 | 23 | 15 | - | P47 | C | D |
| | | | | X1A | | |
| 32 | 24 | 16 | - | INITX | B | E |
| 33 | 25 | 17 | - | P60 | H | K |
| | | | | TIOA2_2 | | |
| | | | | INT15_1 | | |
| | | | | CEC1_0 | | |

| Pin no. | | | | Pin Function | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|
| LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) | | | |
| 34 | - | - | - | P1E<br>RTS4_1<br>MI2SMCK4_1 | D | K |
| 35 | - | - | - | P1D<br>CTS4_1<br>MI2SWS4_1 | D | K |
| 36 | - | - | - | P1C<br>SCK4_1<br>MI2SCK4_1 | D | K |
| 37 | - | - | - | P1B<br>SOT4_1<br>MI2SDO4_1 | D | K |
| - | 26 | - | - | P1B<br>SOT4_1 | D | K |
| 38 | - | - | - | P1A<br>SIN4_1<br>INT05_1<br>CEC0_0<br>MI2SDI4_1 | H | K |
| - | 27 | - | - | P1A<br>SIN4_1<br>INT05_1<br>CEC0_0 | H | K |
| 39 | - | - | - | P1F<br>ADTG_5 | D | K |
| 40 | 28 | 18 | - | P10<br>AN00 | F | J |
| 41 | 29 | 19 | - | P11<br>AN01<br>SIN1_1<br>INT02_1<br>WKUP1 | G | J |
| 42 | 30 | 20 | - | P12<br>AN02<br>SOT1_1 | F | J |
| 43 | 31 | 21 | - | P13<br>AN03<br>SCK1_1<br>RTCCO_1<br>SUBOUT_1 | F | J |
| 44 | 32 | - | - | P14<br>AN04<br>SIN0_1<br>SCS10_1<br>INT03_1 | F | J |

| Pin no. | | | | Pin Function | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|
| LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) | | | |
| 45 | 33 | - | - | P15 | F | J |
| | | | | AN05 | | |
| | | | | SOT0_1 | | |
| | | | | SCS11_1 | | |
| 46 | 34 | 22 | - | P23 | F | J |
| | | | | AN06 | | |
| | | | | SCK0_0 | | |
| | | | | TIOA7_1 | | |
| 47 | 35 | 23 | - | P22 | F | J |
| | | | | AN07 | | |
| | | | | TIOB7_1 | | |
| 48 | 36 | 24 | - | VCC | - | - |
| 49 | 37 | - | - | AVRH * | - | - |
| 50 | 38 | 25 | - | AVRL | - | - |
| 51 | 39 | 26 | - | P21 | E | K |
| | | | | INT06_1 | | |
| | | | | WKUP2 | | |
| 52 | - | - | - | P00 | E | K |
| | | | | WKUP4 | | |
| 53 | 40 | 27 | - | P01 | D | K |
| | | | | SWCLK | | |
| | | | | SOT0_0 | | |
| 54 | - | - | - | P02 | E | K |
| | | | | WKUP5 | | |
| 55 | 41 | 28 | - | P03 | D | K |
| | | | | SWDIO | | |
| | | | | SIN0_0 | | |
| | | | | TIOB7_0 | | |
| 56 | 42 | 29 | - | P05 | E | K |
| | | | | MD1 | | |
| | | | | TIOA5_2 | | |
| | | | | INT00_1 | | |
| | | | | WKUP3 | | |
| 57 | 43 | - | - | VCC | - | - |
| 58 | 44 | 30 | - | P80 | J | G |
| | | | | UDM0 | | |
| 59 | 45 | 31 | - | P81 | J | G |
| | | | | UDP0 | | |
| 60 | 46 | 32 | - | VSS | - | - |
| 61 | 47 | - | - | P61 | H | K |
| | | | | UHCONX0 | | |
| | | | | TIOB2_2 | | |
| 62 | - | - | - | P0B | E | K |
| | | | | TIOB6_1 | | |
| | | | | WKUP6 | | |

| Pin no. | | | | Pin Function | I/O circuit type | Pin state type |
|---|---|---|---|---|---|---|
| **LQFP-64**<br>**QFN-64** | **LQFP-48**<br>**QFN-48** | **LQFP-32**<br>**QFN-32** | **WLCSP**<br>**(TBD)** | | | |
| 63 | - | - | - | P0C<br>TIOA6_1<br>WKUP7 | E | K |
| 64 | 48 | 1 | - | P0F<br>NMIX<br>WKUP0<br>RTCCO_0<br>SUBOUT_0<br>CROUT_1 | E | I |

*: In case of 32-pin package, AVRH pin is internally connected to VCC pin.

## List of Pin Functions

The number after the underscore ("_") in a pin name such as XXX_1 and XXX_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) |
| ADC | ADTG_5 | A/D converter external trigger input pin | 39 | - | - | - |
| | ADTG_6 | | 8 | 8 | 7 | - |
| | ADTG_7 | | 23 | - | - | - |
| ADC | AN00 | A/D converter analog input pin. ANxx describes ADC ch.xx. | 40 | 28 | 18 | - |
| | AN01 | | 41 | 29 | 19 | - |
| | AN02 | | 42 | 30 | 20 | - |
| | AN03 | | 43 | 31 | 21 | - |
| | AN04 | | 44 | 32 | - | - |
| | AN05 | | 45 | 33 | - | - |
| | AN06 | | 46 | 34 | 22 | - |
| | AN07 | | 47 | 35 | 23 | - |
| Base Timer 0 | TIOA0_0 | Base timer ch.0 TIOA pin | 20 | - | - | - |
| | TIOA0_1 | | 11 | 10 | - | - |
| | TIOB0_1 | Base timer ch.0 TIOB pin | 5 | 5 | - | - |
| Base Timer 1 | TIOA1_0 | Base timer ch.1 TIOA pin | 21 | - | - | - |
| | TIOA1_1 | | 12 | 11 | - | - |
| | TIOA1_2 | | 4 | 4 | - | - |
| Base Timer 2 | TIOA2_0 | Base timer ch.2 TIOA pin | 22 | - | - | - |
| | TIOA2_1 | | 13 | 12 | - | - |
| | TIOA2_2 | | 33 | 25 | 17 | - |
| | TIOB2_1 | Base timer ch.2 TIOB pin | 7 | 7 | 6 | - |
| | TIOB2_2 | | 61 | 47 | - | - |
| Base Timer 3 | TIOA3_0 | Base timer ch.3 TIOA pin | 23 | - | - | - |
| | TIOA3_1 | | 14 | - | - | - |
| | TIOB3_0 | Base timer ch.3 TIOB pin | 24 | - | - | - |
| Base Timer 4 | TIOA4_1 | Base timer ch.4 TIOA pin | 15 | - | - | - |
| | TIOB4_1 | Base timer ch.4 TIOB pin | 9 | - | - | - |
| Base Timer 5 | TIOA5_1 | Base timer ch.5 TIOA pin | 16 | - | - | - |
| | TIOA5_2 | | 56 | 42 | 29 | - |
| | TIOB5_1 | Base timer ch.5 TIOB pin | 10 | - | - | - |
| Base Timer 6 | TIOA6_1 | Base timer ch.6 TIOA pin | 63 | - | - | - |
| | TIOB6_1 | Base timer ch.6 TIOB pin | 62 | - | - | - |
| Base Timer 7 | TIOA7_1 | Base timer ch.7 TIOA pin | 46 | 34 | 22 | - |
| | TIOB7_0 | Base timer ch.7 TIOB pin | 55 | 41 | 28 | - |
| | TIOB7_1 | | 47 | 35 | 23 | - |
| Debugger | SWCLK | Serial wire debug interface clock input pin | 53 | 40 | 27 | - |
| | SWDIO | Serial wire debug interface data input / output pin | 55 | 41 | 28 | - |

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | LQFP-64 QFN-64 | LQFP-48 QFN-48 | LQFP-32 QFN-32 | WLCSP (TBD) |
| External Interrupt | INT00_0 | External interrupt request 00 input pin | 1 | 1 | 2 | - |
| | INT00_1 | | 56 | 42 | 29 | - |
| | INT01_0 | External interrupt request 01 input pin | 2 | 2 | 3 | - |
| | INT02_0 | External interrupt request 02 input pin | 3 | 3 | 4 | - |
| | INT02_1 | | 41 | 29 | 19 | - |
| | INT03_0 | External interrupt request 03 input pin | 11 | 10 | - | - |
| | INT03_1 | | 44 | 32 | - | - |
| | INT03_2 | | 5 | 5 | - | - |
| | INT04_0 | External interrupt request 04 input pin | 8 | 8 | 7 | - |
| | INT04_2 | | 6 | 6 | 5 | - |
| | INT05_1 | External interrupt request 05 input pin | 38 | 27 | - | - |
| | INT05_2 | | 7 | 7 | 6 | - |
| | INT06_1 | External interrupt request 06 input pin | 51 | 39 | 26 | - |
| | INT06_2 | | 26 | 18 | - | - |
| | INT07_2 | External interrupt request 07 input pin | 4 | 4 | - | - |
| | INT08_1 | External interrupt request 08 input pin | 10 | - | - | - |
| | INT12_1 | External interrupt request 12 input pin | 20 | - | - | - |
| | INT13_1 | External interrupt request 13 input pin | 21 | - | - | - |
| | INT15_1 | External interrupt request 15 input pin | 33 | 25 | 17 | - |
| | NMIX | Non-Maskable Interrupt input pin | 64 | 48 | 1 | - |
| GPIO | P00 | General-purpose I/O port 0 | 52 | - | - | - |
| | P01 | | 53 | 40 | 27 | - |
| | P02 | | 54 | - | - | - |
| | P03 | | 55 | 41 | 28 | - |
| | P05 | | 56 | 42 | 29 | - |
| | P0B | | 62 | - | - | - |
| | P0C | | 63 | - | - | - |
| | P0F | | 64 | 48 | 1 | - |
| GPIO | P10 | General-purpose I/O port 1 | 40 | 28 | 18 | - |
| | P11 | | 41 | 29 | 19 | - |
| | P12 | | 42 | 30 | 20 | - |
| | P13 | | 43 | 31 | 21 | - |
| | P14 | | 44 | 32 | - | - |
| | P15 | | 45 | 33 | - | - |
| | P1A | | 38 | 27 | - | - |
| | P1B | | 37 | 26 | - | - |
| | P1C | | 36 | - | - | - |
| | P1D | | 35 | - | - | - |
| | P1E | | 34 | - | - | - |
| | P1F | | 39 | - | - | - |
| GPIO | P21 | General-purpose I/O port 2 | 51 | 39 | 26 | - |
| | P22 | | 47 | 35 | 23 | - |
| | P23 | | 46 | 34 | 22 | - |

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | **LQFP-64 QFN-64** | **LQFP-48 QFN-48** | **LQFP-32 QFN-32** | **WLCSP (TBD)** |
| GPIO | P30 | General-purpose I/O port 3 | 5 | 5 | - | - |
| | P31 | | 6 | 6 | 5 | - |
| | P32 | | 7 | 7 | 6 | - |
| | P33 | | 8 | 8 | 7 | - |
| | P34 | | 9 | 9 | - | - |
| | P35 | | 10 | - | - | - |
| | P3A | | 11 | 10 | - | - |
| | P3B | | 12 | 11 | - | - |
| | P3C | | 13 | 12 | - | - |
| | P3D | | 14 | - | - | - |
| | P3E | | 15 | - | - | - |
| | P3F | | 16 | - | - | - |
| GPIO | P40 | General-purpose I/O port 4 | 20 | - | - | - |
| | P41 | | 21 | - | - | - |
| | P42 | | 22 | - | - | - |
| | P43 | | 23 | - | - | - |
| | P46 | | 30 | 22 | 14 | - |
| | P47 | | 31 | 23 | 15 | - |
| | P4C | | 24 | 16 | - | - |
| | P4D | | 25 | 17 | - | - |
| | P4E | | 26 | 18 | - | - |
| GPIO | P50 | General-purpose I/O port 5 | 1 | 1 | 2 | - |
| | P51 | | 2 | 2 | 3 | - |
| | P52 | | 3 | 3 | 4 | - |
| | P53 | | 4 | 4 | - | - |
| GPIO | P60 | General-purpose I/O port 6 | 33 | 25 | 17 | - |
| | P61 | | 61 | 47 | - | - |
| GPIO | P80 | General-purpose I/O port 8 | 58 | 44 | 30 | - |
| | P81 | | 59 | 45 | 31 | - |
| GPIO | PE2 | General-purpose I/O port E | 18 | 14 | 9 | - |
| | PE3 | | 19 | 15 | 10 | - |
| Multi-function Serial 0 | SIN0_0 | Multi-function serial interface ch.0 input pin | 55 | 41 | 28 | - |
| | SIN0_1 | | 44 | 32 | - | - |
| | SOT0_0 (SDA0_0) | Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I2C pin (operation mode 4). | 53 | 40 | 27 | - |
| | SOT0_1 (SDA0_1) | | 45 | 33 | - | - |
| | SCK0_0 (SCL0_0) | Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I2C pin (operation mode 4). | 46 | 34 | 22 | - |

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | **LQFP-64 QFN-64** | **LQFP-48 QFN-48** | **LQFP-32 QFN-32** | **WLCSP (TBD)** |
| Multi-function Serial 1 | SIN1_1 | Multi-function serial interface ch.1 input pin | 41 | 29 | 19 | - |
| | SOT1_1 (SDA1_1) | Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I2C pin (operation mode 4). | 42 | 30 | 20 | - |
| | SCK1_1 (SCL1_1) | Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I2C pin (operation mode 4). | 43 | 31 | 21 | - |
| | SCS10_1 | Multi-function serial interface ch.1 serial chip select 0 input/output pin. | 44 | 32 | - | - |
| | SCS11_1 | Multi-function serial interface ch.1 serial chip select 1 output pin. | 45 | 33 | - | - |
| Multi-function Serial 3 | SIN3_1 | Multi-function serial interface ch.3 input pin | 1 | 1 | 2 | - |
| | SOT3_1 (SDA3_1) | Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I2C pin (operation mode 4). | 2 | 2 | 3 | - |
| | SCK3_1 (SCL3_1) | Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I2C pin (operation mode 4). | 3 | 3 | 4 | - |
| Multi-function Serial 4 | SIN4_1 | Multi-function serial interface ch.4 input pin | 38 | 27 | - | - |
| | SOT4_1 (SDA4_1) | Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I2C pin (operation mode 4). | 37 | 26 | - | - |
| | SCK4_1 (SCL4_1) | Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I2C pin (operation mode 4). | 36 | - | - | - |
| | CTS4_1 | Multi-function serial interface ch4 CTS input pin | 35 | - | - | - |
| | RTS4_1 | Multi-function serial interface ch4 RTS output pin | 34 | - | - | - |

| Pin function | Pin name | Function description | Pin no. | | | |
|---|---|---|---|---|---|---|
| | | | **LQFP-64**<br>**QFN-64** | **LQFP-48**<br>**QFN-48** | **LQFP-32**<br>**QFN-32** | **WLCSP**<br>**(TBD)** |
| Multi-function<br>Serial 6 | SIN6_1 | Multi-function serial interface ch.6 input pin | 8 | 8 | 7 | - |
| | SOT6_1<br>(SDA6_1) | Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I2C pin (operation mode 4). | 7 | 7 | 6 | - |
| | SCK6_1<br>(SCL6_1) | Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I2C pin (operation mode 4). | 6 | 6 | 5 | - |
| | SCS60_1 | Multi-function serial interface ch.6 serial chip select 0 input/output pin. | 5 | 5 | - | - |
| | SCS61_1 | Multi-function serial interface ch.6 serial chip select 1 output pin. | 9 | 9 | - | - |
| | SCS62_1 | Multi-function serial interface ch.6 serial chip select 2 output pin. | 10 | - | - | - |
| Multi-function<br>Serial 7 | SIN7_1 | Multi-function serial interface ch.7 input pin | 26 | 18 | - | - |
| | SOT7_1<br>(SDA7_1) | Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I2C pin (operation mode 4). | 25 | 17 | - | - |
| | SCK7_1<br>(SCL7_1) | Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I2C pin (operation mode 4). | 24 | 16 | - | - |