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S6E2C4 Series

32-bit ARM® Cortex®-M4F FM4 Microcontroller

Devices in the S6E2C4 Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F processor with on-chip flash memory and SRAM. The series has peripherals such as motor control timers, A/D converters, and communications interfaces (CAN, UART, CSIO (SPI), I²C, LIN). The products that are described in this data sheet are placed into TYPE3-M4 product categories "FM4 Family Peripheral Manual Main Part (002-04856)."

Features

32-bit ARM Cortex-M4F Core

- Processor version: r0p1
- Up to 200 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

On-chip Memories

- Flash memory

This series is based on two independent on-chip flash memories.

  - Up to 2048 Kbytes
  - Built-in flash accelerator system with 16 Kbytes trace buffer memory
  - Read access to flash memory that can be achieved without wait-cycle up to an operating frequency of 72 MHz. Even at the operating frequency more than 72 MHz, an equivalent single cycle access to flash memory can be obtained by the flash accelerator system.
  - Security function for code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

  - SRAM0: up to 192 Kbytes
  - SRAM1: 32 Kbytes
  - SRAM2: 32 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Maximum Access size: 256M byte
- Supports address/data multiplexing
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note**: It is necessary to use the Cypress provided software library to use the scramble function.

CAN Interface (Max two Channels)

- Compatible with CAN specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32-message buffer

CAN-FD Interface (One Channel)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 5 Mbps
- Message buffer for receiver: up to 192 messages
- Message buffer for transmitter: up to 32 messages
- CAN with flexible data rate (non-ISO CAN-FD)
- **Notes**:
  - CAN FD cannot communicate between non-ISO CAN FD and ISO CAN FD, because non-ISO CAN FD and ISO CAN FD are different frame format.
  - About the problem of "non-ISO CAN FD", see the White Paper from CiA(CAN in Automation). http://www.can-newsletter.org/engineering/standardization/141222_can-fd-and-crc-issued_white-paper_bosch

Multi-function Serial Interface (Max 16 channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 0 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)
  - LIN break delimiter generation (can change to 1- to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

DMA Controller (Eight channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller; 256 Channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

D/A Converter (Max 2 Channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 16 Channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144 pin package
- Some pins 5V tolerant I/O.
  See 4. Pin Descriptions and 5. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max three Units)

The multi-function timer is composed of the following blocks:

Minimum resolution: 5.00 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.
-

Quadrature Position/Revolution Counter (QPRC; Max four Channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32/16-bit down counters.
Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (2 Channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

Programmable Cyclic Redundancy Check (PRGCRC) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16, IEEE-802.3 CRC32 and generating polynomial are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7
- Generating polynomial

SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

I²S (Inter-IC Sound Bus) Interface (TX x 1 channel, RX x 1 channel)

- Supports three transfer protocols
  - I²S
  - Left justified
  - DSP mode
  - Separate clock generation block for flexible system integration options
- Master/slave mode selectable
- RX Only, TX Only or TX and RX simultaneous operation selectable
- Word length is programmable from 7-bits to 32 bits
- RX/TX FIFO integrated (RX: 66 words x 32-bits, TX: 66 words x 32-bits)
- DMA, interrupts, or polling based data transfer supported

High-Speed Quad SPI

Up to 66 MHz clock rates for very fast data transfers to and from SPI compatible devices.

Up to 256 Mbytes of memory mapped address space.

- Single data rate (SDR)
- Supports single, dual, and quad data modes
- Built-in direct mode and command sequencer mode
  - Direct mode: Access by use of transmission FIFO/reception FIFO (up to16 word x 32 bit)
  - Command sequencer mode: Automatic access assigned to external device area.

Clock and Reset

- Clocks

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

  - Main clock: 4 MHz to 48 MHz
  - Sub clock: 32.768 kHz
  - High-speed internal CR clock: 4 MHz
  - Low-speed internal CR clock: 100 kHz
  - Main PLL Clock

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Two power supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for VBAT: VBAT = 1.65 V to 5.5 V

Table of Contents

1. Product Lineup

Memory Size

Product Name		S6E2C48H/J/L	S6E2C49H/J/L	S6E2C4AH/J/L
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

Function

Product Name			S6E2C48H0A S6E2C49H0A S6E2C4AH0A	S6E2C48J0A S6E2C49J0A S6E2C4AJ0A	S6E2C48L0A S6E2C49L0A S6E2C4AL0A
Pin count			144	176/192	216
CPU			Cortex-M4F, MPU, NVIC 128 ch		
	Freq.		200 MHz		
Power supply voltage range			2.7V to 5.5V		
CAN			2 ch (Max)		
CAN-FD (non-ISO CAN-FD)			1 ch		
DMAC			8ch		
DSTC			256 ch		
External bus interface			Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash , NAND flash SDRAM	Addr: 25-bit (Max), Data: 8-/16-/32-bit CS: 9 (Max), SRAM, NOR flash , NAND flash, SDRAM
Multi-function serial interface (UART/CSIO/LIN/I²C)			16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO		
Base timer (PWC/Reload timer/PWM/PPG)			16 ch (Max)		
MF timer	A/D activation compare	6 ch	3 units (Max)		
	Input capture	4 ch			
	Free-run timer	3 ch			
	Output compare	6 ch			
	Waveform generator	3 ch			
	PPG	3 ch			
SD card interface			1 unit		
I²S			-	1 unit	
High-speed quad SPI			-	1 unit	
QPRC			4 ch (Max)		
Dual timer			1 unit		
Real-time clock			1 unit		
Watch counter			1 unit		
CRC accelerator			Yes (fixed, programmable)		
Watchdog timer			1 ch (SW) + 1 ch (HW)		
External interrupts			32 pins (Max)+ NMI × 1		
I/O ports			120 pins (Max)	152 pins (Max)	190 pins (Max)
12-bit A/D converter			24 ch (3 units)	32 ch (3 units)	
12-bit D/A converter			2 units (Max)		
CSV (clock supervisor)			Yes		
LVD (low-voltage detector)			2 ch		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		

Product Name	S6E2C48H0A S6E2C49H0A S6E2C4AH0A	S6E2C48J0A S6E2C49J0A S6E2C4AJ0A	S6E2C48L0A S6E2C49L0A S6E2C4AL0A
Debug function	SWJ-DP/ETM/HTM		
Unique ID	Yes		

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.*

2. Packages

Package \ Product Name	S6E2C48H0A S6E2C49H0A S6E2C4AH0A	S6E2C48J0A S6E2C49J0A S6E2C4AJ0A	S6E2C48L0A S6E2C49L0A S6E2C4AL0A
LQFP: LQS144 (0.5-mm pitch)	❍	-	-
LQFP: LQP176 (0.5-mm pitch)	-	❍	-
BGA : LBE192 (0.8-mm pitch)	-	❍	-
LQFP: LQQ216 (0.4-mm pitch)	-	-	❍

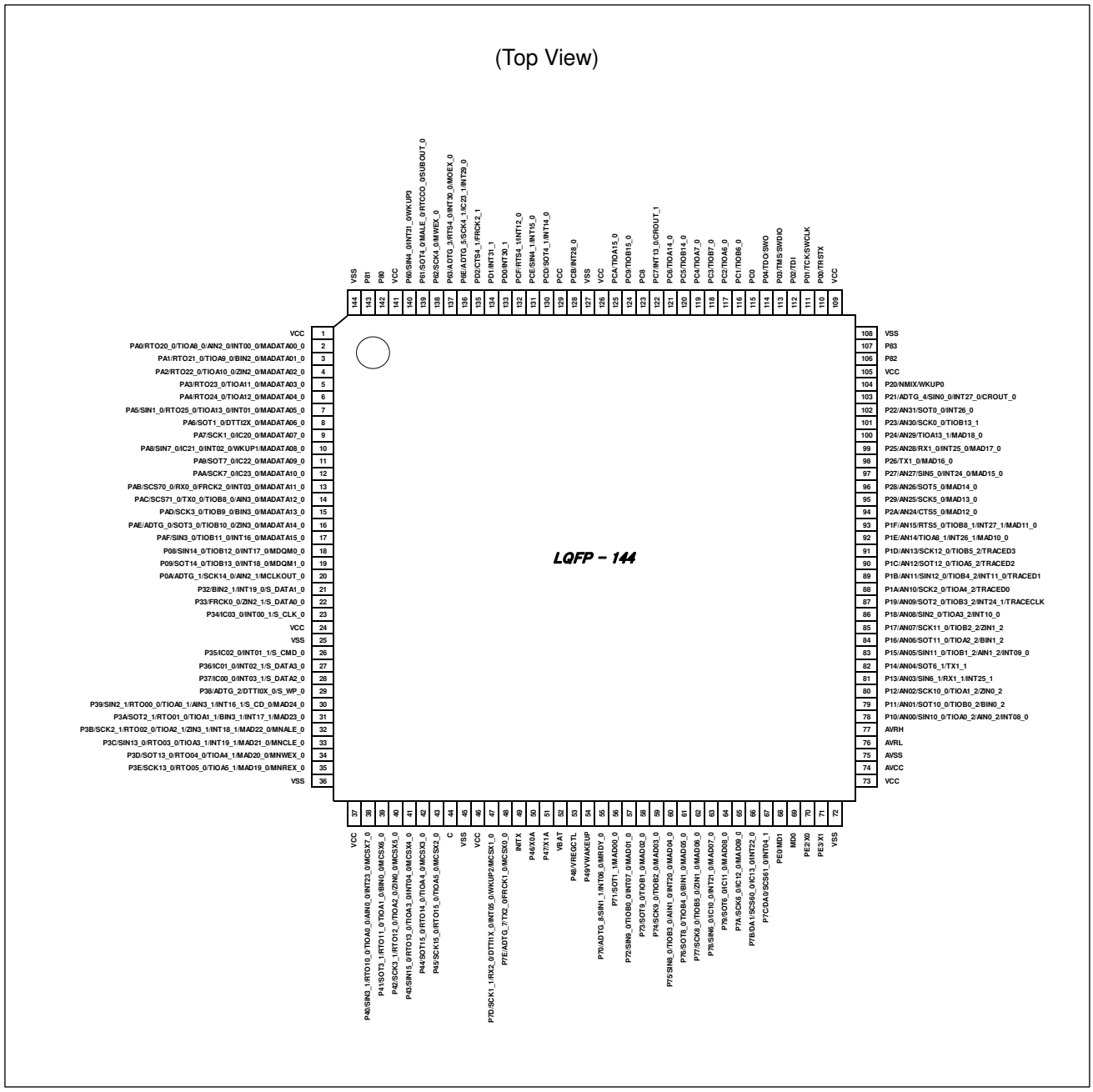
❍: Supported

Note:

- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignments

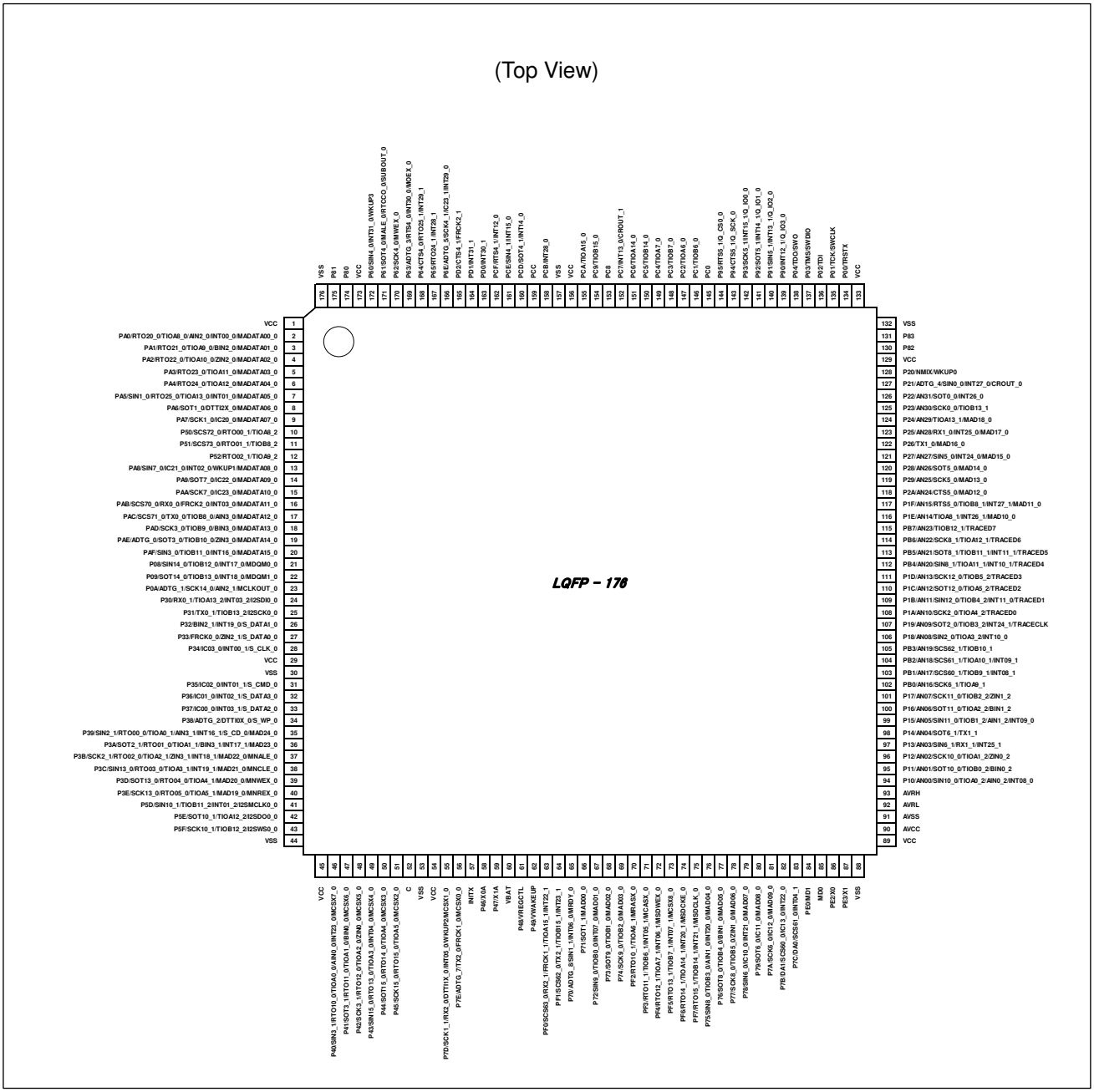
LQS144



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

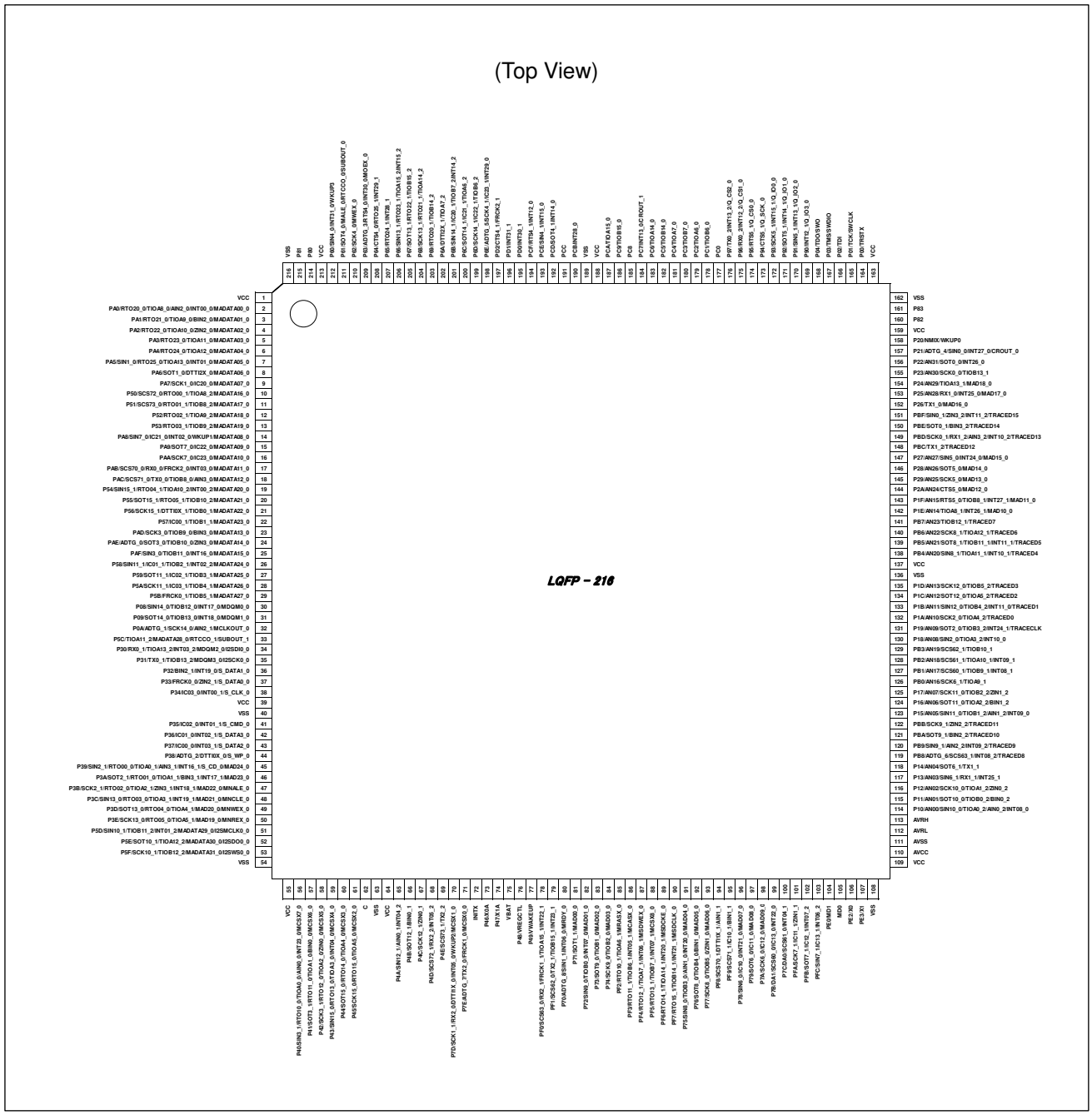
LQP176



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LQQ216



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

LBE192

(Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		P81	P80	VCC	VSS	PCD	PCB	VSS	VCC	PC8	VSS	TCK	VCC	
B	VSS	PA0	P60	P62	P64	PD1	PCA	PC1	P95	P92	TDO	TMS	TRSTX	VSS
C	VCC	PA1	PA2	P61	P63	PD2	PCC	PC5	PC0	P93	P90	TDI	P20	P83
D	PA5	PA4	PA6	PA7	PA3	P6E	PCE	PC6	PC2	P94	P91	P22	P21	P84
E	VSS	P50	P51	P52	PA8	P65	PCF	PC7	PC3	P26	P25	P24	P23	VCC
F	PA9	PAA	PAB	PAC	PAD	PAE	PD0	PC9	PC4	P2A	P29	P28	P27	PB5
G	VSS	PAF	P08	P09	P0A	P30	VSS	VSS	P1F	P1E	PB7	PB6	PB4	P1B
H	VCC	P32	P34	P31	VSS	P35	VSS	VSS	P18	PB2	P1D	P19	P1C	P1A
J	P33	P39	P38	P37	P36	P71	VSS	P74	PB1	PB0	P17	P16	P15	PB3
K	P3A	P3B	P3C	P3D	PF0	PF1	VSS	P73	P75	P79	P14	P12	P11	P13
L	P3E	P5D	P5E	P43	P7D	P70	VSS	P72	PF7	P78	P10	AVRH	AVRL	VSS
M	VSS	P5F	P42	P44	P7E	P49	VSS	PF3	PF6	P7A	P7C	AVSS	AVCC	VCC
N	VCC	P40	P41	P45	INITX	P48	VSS	PF2	PF4	P77	P7B	MD0	MD1	VSS
P		C	VSS	VCC	X0A	X1A	VSS	VBAT	PF5	P76	VSS	X0	X1	

PFBGA-192

Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
1	1	1	C1	VCC	-	-
2	2	2	B2	PA0 RTO20_0 (PPG20_0) TIOA8_0 AIN2_0 INT00_0 MADATA00_0	G	K
3	3	3	C2	PA1 RTO21_0 (PPG20_0) TIOA9_0 BIN2_0 MADATA01_0	G	I
4	4	4	C3	PA2 RTO22_0 (PPG22_0) TIOA10_0 ZIN2_0 MADATA02_0	G	I
5	5	5	D5	PA3 RTO23_0 (PPG22_0) TIOA11_0 MADATA03_0	G	I
6	6	6	D2	PA4 RTO24_0 (PPG24_0) TIOA12_0 MADATA04_0	G	I
7	7	7	D1	PA5 SIN1_0 RTO25_0 (PPG24_0) TIOA13_0 INT01_0 MADATA05_0	G	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
8	8	8	D3	PA6 SOT1_0 (SDA1_0)) DTTI2X_0 MADATA06_0	E	I
9	9	9	D4	PA7 SCK1_0 (SCL1_0) IC20_0 MADATA07_0	E	I
10	10	-	E2	P50 SCS72_0 RTO00_1 (PPG00_1) TIOA8_2 MADATA16_0	E	I
11	11	-	E3	P51 SCS73_0 RTO01_1 (PPG00_1) TIOB8_2 MADATA17_0	E	I
12	12	-	E4	P52 RTO02_1 (PPG02_1) TIOA9_2 MADATA18_0	E	I
13	-	-	-	P53 RTO03_1 (PPG02_1) TIOB9_2 MADATA19_0	E	I
14	13	10	E5	PA8 SIN7_0 IC21_0 INT02_0 WKUP1 MADATA08_0	I	Q
15	14	11	F1	PA9 SOT7_0 (SDA7_0) IC22_0 MADATA09_0	N	I
16	15	12	F2	PAA SCK7_0 (SCL7_0) IC23_0 MADATA10_0	N	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
17	16	13	F3	PAB SCS70_0 RX0_0 FRCK2_0 INT03_0 MADATA11_0	E	K
18	17	14	F4	PAC SCS71_0 TX0_0 TIOB8_0 AIN3_0 MADATA12_0	E	I
19	-	-	-	P54 SIN15_1 RTO04_1 (PPG04_1) TIOA10_2 INT00_2 MADATA20_0	E	K
20	-	-	-	P55 SOT15_1 (SDA15_1) RTO05_1 (PPG04_1) TIOB10_2 MADATA21_0	E	I
21	-	-	-	P56 SCK15_1 (SCL15_1) DTTI0X_1 TIOB0_1 MADATA22_0	E	I
22	-	-	-	P57 IC00_1 TIOB1_1 MADATA23_0	E	I
23	18	15	F5	PAD SCK3_0 (SCL3_0) TIOB9_0 BIN3_0 MADATA13_0	N	I
24	19	16	F6	PAE ADTG_0 SOT3_0 (SDA3_0) TIOB10_0 ZIN3_0 MADATA14_0	N	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
25	20	17	G2	PAF SIN3_0 TIOB11_0 INT16_0 MADATA15_0	I	K
26	-	-	-	P58 SIN11_1 IC01_1 TIOB2_1 INT02_2 MADATA24_0	E	K
27	-	-	-	P59 SOT11_1 (SDA11_1) IC02_1 TIOB3_1 MADATA25_0	E	I
28	-	-	-	P5A SCK11_1 (SCL11_1) IC03_1 TIOB4_1 MADATA26_0	E	I
29	-	-	-	P5B FRCK0_1 TIOB5_1 MADATA27_0	E	I
30	21	18	G3	P08 SIN14_0 TIOB12_0 INT17_0 MDQM0_0	E	K
31	22	19	G4	P09 SOT14_0 (SDA14_0) TIOB13_0 INT18_0 MDQM1_0	E	K
32	23	20	G5	P0A ADTG_1 SCK14_0 (SCL14_0) AIN2_1 MCLKOUT_0	L	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
33	-	-	-	P5C TIOA11_2 MADATA28_0 RTCCO_1 SUBOUT_1	E	I
34	24	-	G6	P30 RX0_1 TIOA13_2 INT03_2 MDQM2_0 I2SDI0_0	E	K
35	25	-	H4	P31 TX0_1 TIOB13_2 MDQM3_0 I2SCK0_0	E	I
36	26	21	H2	P32 BIN2_1 INT19_0 S_DATA1_0	L	K
37	27	22	J1	P33 FRCK0_0 ZIN2_1 S_DATA0_0	L	I
38	28	23	H3	P34 IC03_0 INT00_1 S_CLK_0	L	K
39	29	24	H1	VCC	-	-
40	30	25	H5	VSS	-	-
41	31	26	H6	P35 IC02_0 INT01_1 S_CMD_0	L	K
42	32	27	J5	P36 IC01_0 INT02_1 S_DATA3_0	L	K
43	33	28	J4	P37 IC00_0 INT03_1 S_DATA2_0	L	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
44	34	29	J3	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
45	35	30	J2	P39 SIN2_1 RTO00_0 (PPG00_0) TIOA0_1 AIN3_1 INT16_1 S_CD_0 MAD24_0	G	K
46	36	31	K1	P3A SOT2_1 (SDA2_1) RTO01_0 (PPG00_0) TIOA1_1 BIN3_1 INT17_1 MAD23_0	G	K
47	37	32	K2	P3B SCK2_1 (SCL2_1) RTO02_0 (PPG02_0) TIOA2_1 ZIN3_1 INT18_1 MAD22_0 MNALE_0	G	K
48	38	33	K3	P3C SIN13_0 RTO03_0 (PPG02_0) TIOA3_1 INT19_1 MAD21_0 MNCLE_0	G	K
49	39	34	K4	P3D SOT13_0 (SDA13_0) RTO04_0 (PPG04_0) TIOA4_1 MAD20_0 MNWEX_0	G	I
50	40	35	L1	P3E SCK13_0 (SCL13_0) RTO05_0 (PPG04_0) TIOA5_1 MAD19_0 MNREX_0	G	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
51	41	-	L2	P5D SIN10_1 TIOB11_2 INT01_2 MADATA29_0 I2SMCLK0_0	E	K
52	42	-	L3	P5E SOT10_1 (SDA10_1) TIOA12_2 MADATA30_0 I2SDO0_0	E	I
53	43	-	M2	P5F SCK10_1 (SCL10_1) TIOB12_2 MADATA31_0 I2SWS0_0	E	I
54	44	36	M1	VSS	-	-
55	45	37	N1	VCC	-	-
56	46	38	N2	P40 SIN3_1 RTO10_0 (PPG10_0) TIOA0_0 AIN0_0 INT23_0 MCSX7_0	G	K
57	47	39	N3	P41 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) TIOA1_0 BIN0_0 MCSX6_0	G	I
58	48	40	M3	P42 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) TIOA2_0 ZIN0_0 MCSX5_0	G	I
59	49	41	L4	P43 SIN15_0 RTO13_0 (PPG12_0) TIOA3_0 INT04_0 MCSX4_0	G	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
60	50	42	M4	P44 SOT15_0 (SDA15_0) RTO14_0 (PPG14_0) TIOA4_0 MCSX3_0	G	I
61	51	43	N4	P45 SCK15_0 (SCL15_0) RTO15_0 (PPG14_0) TIOA5_0 MCSX2_0	G	I
62	52	44	P2	C	-	-
63	53	45	P3	VSS	-	-
64	54	46	P4	VCC	-	-
65	-	-	-	P4A SIN12_1 AIN0_1 INT04_2	E	K
66	-	-	-	P4B SOT12_1 (SDA12_1) BIN0_1	E	I
67	-	-	-	P4C SCK12_1 (SCL12_1) ZIN0_1	E	I
68	-	-	-	P4D SCS72_1 RX2_2 INT05_2	E	K
69	-	-	-	P4E SCS73_1 TX2_2	E	I
70	55	47	L5	P7D SCK1_1 (SCL1_1) RX2_0 DTTI1X_0 INT05_0 WKUP2 MCSX1_0	L	Q
71	56	48	M5	P7E ADTG_7 TX2_0 FRCK1_0 MCSX0_0	L	I
72	57	49	N5	INITX	B	C
73	58	50	P5	P46 X0A	P	S
74	59	51	P6	P47 X1A	Q	T
75	60	52	P8	VBAT	-	-
76	61	53	N6	P48 VREGCTL	O	U

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
77	62	54	M6	P49 VWAKEUP	O	U
78	63	-	K5	PF0 SCS63_0 RX2_1 FRCK1_1 TIOA15_1 INT22_1	E	K
79	64	-	K6	PF1 SCS62_0 TX2_1 TIOB15_1 INT23_1	E	K
80	65	55	L6	P70 ADTG_8 SIN1_1 INT06_0 MRDY_0	I	K
81	66	56	J6	P71 SOT1_1 (SDA1_1) MAD00_0	E	I
82	67	57	L8	P72 SIN9_0 TIOB0_0 INT07_0 MAD01_0	E	K
83	68	58	K8	P73 SOT9_0 (SDA9_0) TIOB1_0 MAD02_0	E	I
84	69	59	J8	P74 SCK9_0 (SCL9_0) TIOB2_0 MAD03_0	E	I
85	70	-	N8	PF2 RTO10_1 (PPG10_1) TIOA6_1 MRASX_0	L	I
86	71	-	M8	PF3 RTO11_1 (PPG10_1) TIOB6_1 INT05_1 MCASX_0	L	K
87	72	-	N9	PF4 RTO12_1 (PPG12_1) TIOA7_1 INT06_1 MSDWEX_0	L	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
88	73	-	P9	PF5 RTO13_1 (PPG12_1) TIOB7_1 INT07_1 MCSX8_0	L	K
89	74	-	M9	PF6 RTO14_1 (PPG14_1) TIOA14_1 INT20_1 MSDCKE_0	L	K
90	75	-	L9	PF7 RTO15_1 (PPG14_1) TIOB14_1 INT21_1 MSDCLK_0	L	K
91	76	60	K9	P75 SIN8_0 TIOB3_0 AIN1_0 INT20_0 MAD04_0	E	K
92	77	61	P10	P76 SOT8_0 (SDA8_0) TIOB4_0 BIN1_0 MAD05_0	E	I
93	78	62	N10	P77 SCK8_0 (SCL8_0) TIOB5_0 ZIN1_0 MAD06_0	E	I
94	-	-	-	PF8 SCS70_1 DTTI1X_1 AIN1_1	E	I
95	-	-	-	PF9 SCS71_1 IC10_1 BIN1_1	E	I
96	79	63	L10	P78 SIN6_0 IC10_0 INT21_0 MAD07_0	E	K
97	80	64	K10	P79 SOT6_0 (SDA6_0) IC11_0 MAD08_0	L	I

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
98	81	65	M10	P7A SCK6_0 (SCL6_0) IC12_0 MAD09_0	L	I
99	82	66	N11	P7B DA1 SCS60_0 IC13_0 INT22_0	R	J
100	83	67	M11	P7C DA0 SCS61_0 INT04_1	R	J
101	-	-	-	PFA SCK7_1 (SCL7_1) IC11_1 ZIN1_1	E	I
102	-	-	-	PFB SOT7_1 (SDA7_1) IC12_1 INT07_2	E	K
103	-	-	-	PFC SIN7_1 IC13_1 INT06_2	E	K
104	84	68	N13	PE0 MD1	C	E
105	85	69	N12	MD0	J	D
106	86	70	P12	PE2 X0	A	A
107	87	71	P13	PE3 X1	A	B
108	88	72	N14	VSS	-	-
109	89	73	M14	VCC	-	-
110	90	74	M13	AVCC	-	-
111	91	75	M12	AVSS	-	-
112	92	76	L13	AVRL	-	-
113	93	77	L12	AVRH	-	-
114	94	78	L11	P10 AN00 SIN10_0 TIOA0_2 AIN0_2 INT08_0	F	M