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For More Information

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About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.



32-bit ARM® Cortex®-M4F FM4 Microcontroller

S6E2G Series are FM4 devices with up to 180 MHz CPU, 1 MB flash, 192 KB SRAM, 20x communication peripherals, 33x digital peripherals and 3x analog peripherals. They are designed for industrial automation and metering applications.

Devices in the S6E2G Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F processor with on-chip flash memory and SRAM. The series has peripherals such as motor control timers, A/D converters, and communications interfaces (USB, CAN, UART, CSIO (SPI), I²C, LIN). The products that are described in this data sheet are placed into TYPE5-M4 product categories in the "FM4 Family Peripheral Manual Main Part (002-04856)".

- 32-bit ARM Cortex-M4F Core
 - Up to 180 MHz frequency operation
- On-chip Memories
 - Flash memory: Up to 1024 Kbytes
 - SRAM memory:
 - SRAM0: up to 128 Kbytes
 - SRAM1: 32 Kbytes
 - SRAM2: 32 Kbytes
- Direct Memory Access (DMA) Controller (Eight Channels)
- Descriptor System Data Transfer Controller (DSTC); 256 channels
- External Bus Interface
- USB Interface (Max two channels): Host and Device
- CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only
- Multi-function Serial Interface (Max 10 Channels)
 - UART (Universal Asynchronous Receiver/Transmitter)
 - Clock Synchronous Serial Interface (CSIO (SPI))
 - Local Interconnect Network (LIN)
 - Inter-Integrated Circuit (I²C)
 - Inter-IC Sound (I²S)
- Base Timer (Max 16 channels)
- General Purpose I/O Port
 - Up to 121 high-speed general-purpose I/O ports in 144-pin package
 - Up to 153 high-speed general-purpose I/O ports in 176-pin package
- Multi-function Timer (Max two units)
- Real-Time Clock (RTC)
- Analog to Digital Converter (ADC) (Max 32 Channels)
- Dual Timer (32-/16-bit Down Counter)
- Quadrature Position/Revolution Counter (QPRC; Max two channels)
- Watch Counter
- External Interrupt Controller Unit
- Watchdog Timer (Two channels)
- Cyclic Redundancy Check (CRC) Accelerator
- SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only
- Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only
- Smartcard Interface (Max 2 channels)
- Five Clock Sources
- Six Reset Sources
- Clock Supervisor (CSV)
- Low-Voltage Detector (LVD)
- Six Low-power Consumption Modes
 - Sleep
 - Timer
 - RTC
 - Stop
 - Deep standby RTC
 - Deep standby stop
- Peripheral Clock Gating System
- Crypto Assist Function
- Debug
 - Serial wire JTAG debug port (SWJ-DP)
 - Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
 - AHB trace macrocells (HTM)
- 41-bit Unique ID
- Wide range voltage: VCC = 2.7 to 5.5 V

Ecosystem for Cypress FM4 MCUs

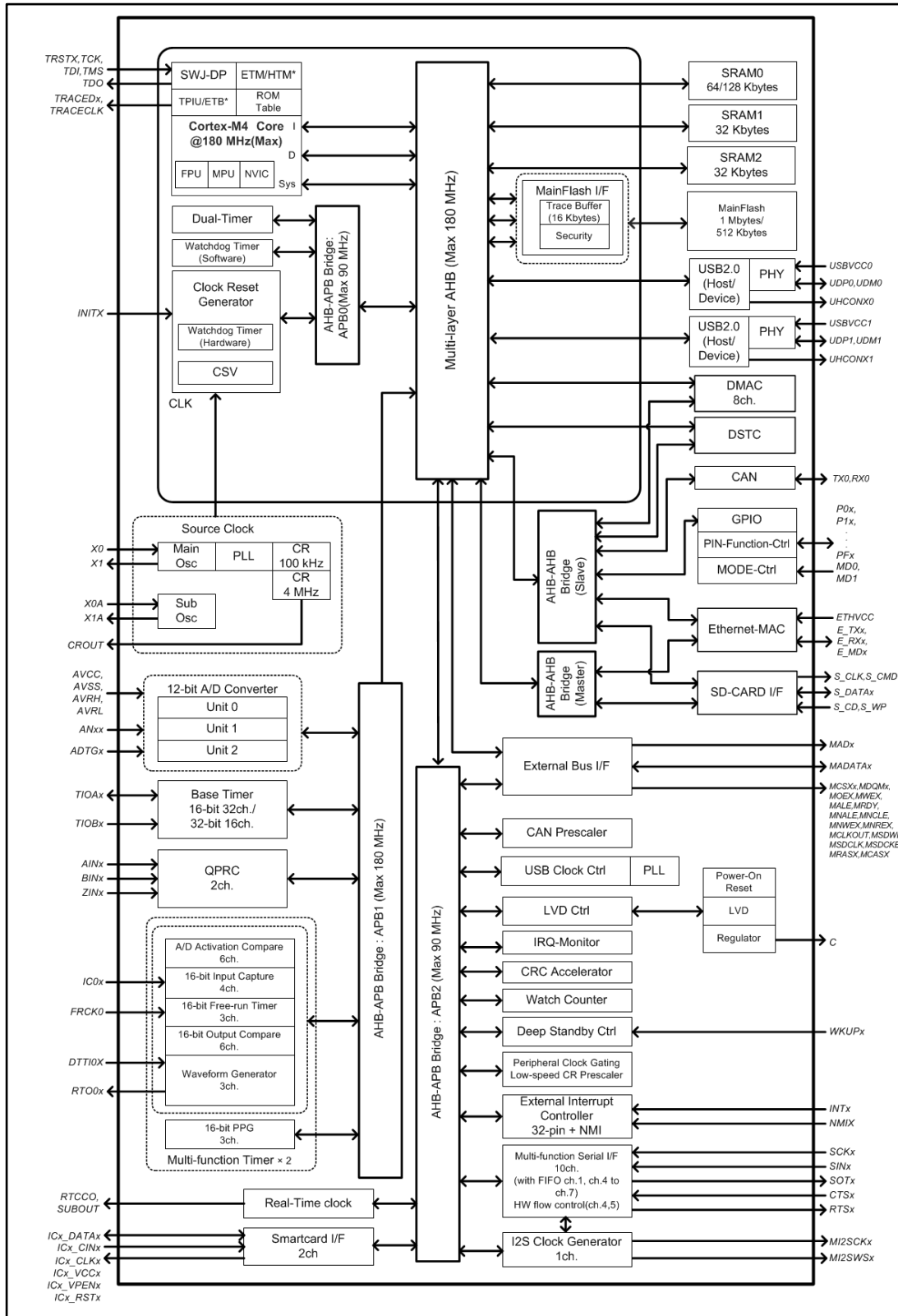
Cypress provides a wealth of data at www.cypress.com to help you to select the right MCU for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for FM4 MCUs:

- Overview: [Product Portfolio](#), [Product Roadmap](#)
- Product Selectors: [FM4 MCUs](#)
- Application notes: Cypress offers a large number of FM4 application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FM4 family of MCUs are:
 - [AN204468 - FM4 I²S USB MP3 Player Application 32-Bit Microcontroller FM4 Family](#): This application note describes the general structure of the I²S USB MP3Player software example, its single modules in detail and how it is used.
 - [AN204471 - FM4 S6E2CC Series External Memory Programmer](#): This document describes use of the MCU Universal Programmer as an off-line programmer for Quad SPI flash memory programming on the S6E2CC Series SK.
 - [AN203277 - FM 32-Bit Microcontroller Family Hardware Design Considerations](#): This application note reviews several topics for designing a hardware system around FM0+, FM3, and FM4 family MCUs. Subjects include power system, reset, crystal, and other pin connections, and programming and debugging interfaces.
 - [AN202488 - FM4 MB9BF56x and S6E2HG Series MCU - Servo Motor Speed Control](#): This document covers servo motor speed control solution on FM4 MCU - MB9BF56x and S6E2HG.
 - [AN99235 - FM4 S6E2HG Series MCU - 16-Bit PWM Using a Base Timer](#): Cypress FM4 Family of 32-bit ARM® Cortex®-M4 Microcontrollers FM4 S6E2H Series Motor Control ARM® Cortex®-M4 MCU
 - [AN202487 - Differences Among FM0+, FM3, and FM4 32-Bit Microcontrollers](#): Highlights the peripheral differences in Cypress's FM family MCUs. It provides dedicated sections for each peripheral and contains lists, tables, and descriptions of peripheral feature and register differences.
 - [AN204438 - How to Setup Flash Security for FM0+, FM3 and FM4 Families](#): This application note describes how to setup the Flash Security for FM0+, FM3, and FM4 devices
- Development kits:
 - [FM4-U120-9B560 - ARM® Cortex®-M4 MCU Starter Kit with USB and CMSIS-DAP](#)
 - [FM4-216-ETHERNET ARM® Cortex®-M4 MCU Development Kit with Ethernet, CAN and USB Host](#)
 - [FM4-176L-S6E2CC-ETH - ARM® Cortex®-M4 MCU Starter Kit with Ethernet and USB Host](#)
 - [FM4-176L-S6E2GM - ARM® Cortex®-M4 MCU Pioneer Kit with Ethernet and USB Host](#)
- Peripheral Manuals

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1. S6E2G Series Block Diagram



2. Product Lineup

Memory Size

Memory Type	Product Name		
	S6E2GM6 S6E2GK6 S6E2GH6 S6E2G36 S6E2G26	S6E2GM8 S6E2GK8 S6E2GH8 S6E2G38 S6E2G28	
On-chip flash memory	512 Kbytes	1024 Kbytes	
On-chip	SRAM	128 Kbytes	192 Kbytes
	SRAM0	64 Kbytes	128 Kbytes
	SRAM1	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes

Function Availability by Part

Description	Product Name				
	S6E2GM6 S6E2GM8	S6E2GK6 S6E2GK8	S6E2GH6 S6E2GH8	S6E2G36 S6E2G38	S6E2G26 S6E2G28
CPU	Cortex-M4F, MPU, NVIC 128 ch				
	Freq.	180 MHz			
Power supply voltage range	2.7 V to 5.5 V				
USB2.0 (Device/Host)	2 ch				
Ethernet-MAC	1 ch. (Max) MII: 1 ch / RMII: 1 ch (Max)	N/A		1ch. (Max) MII: 1 ch / RMII: 1 ch (Max)	
CAN	1 ch (Max)	N/A	1 ch (Max)	N/A	
SD card interface	1 unit			N/A	
DMAC	8 ch				
DSTC	256 ch				
External bus interface	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash SDRAM				
Multi-function serial interface (UART/CSIO(SPI)/LIN/I ² C/I ² S)	10ch (Max) ch 1, ch 4 to ch 7: FIFO, ch 0, ch 2, ch3, ch 8 to ch 15: No FIFO ch 1: I ² S				

Description		Product Name				
		S6E2GM6 S6E2GM8	S6E2GK6 S6E2GK8	S6E2GH6 S6E2GH8	S6E2G36 S6E2G38	S6E2G26 S6E2G28
Base timer (PWC/Reload timer/PWM/PPG)		16 ch (Max)				
MF timer	A/D activation compare	6 ch	2 units (Max)			
	Input capture	4 ch				
	Free-run timer	3 ch				
	Output compare	6 ch				
	Waveform generator	3 ch				
	PPG	3 ch				
Smartcard (ISO7816)		2 ch (Max)				
QPRC		2 ch (Max)				
Dual timer		1 unit				
Real-time clock		1 unit				
Watch counter		1 unit				
CRC accelerator		Yes (fixed)				
Watchdog timer		1 ch (SW) + 1 ch (HW)				
External interrupts		32 pins (Max)+ NMI × 1				
CSV (clock supervisor)		Yes				
LVD (low-voltage detector)		2 ch				
Built-in CR	High-speed	4 MHz				
	Low-speed	100 kHz				
Debug function		SWJ-DP/ETM/HTM				
Unique ID		Yes				

*1: Crypto Assist Function is built in following products.

S6E2GM6HHA, S6E2GM8HHA, S6E2GM6JHA, S6E2GM8JHA

Notes:

- Because of package pin limitations, not all functions within the device can be brought out to external pins. You must carefully work out the pin allocation needed for your design.
You must use the port relocate function of the I/O port according to your function use.
- See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.

3. Package-Dependent Features

All S6E2G Series of parts are available in both 144-pin LQFP and 176-pin LQFP.

Description	Base Part Number S6E2G			
	Package Suffix			
	H0A	HHA*	J0A	JHA*
LQFP: (0.5 mm pitch)	144 pins		176 pins	
I/O Ports	121 pins (Max)		153 pins (Max)	
12-bit ADC converter	24 (3 units)		32 ch (3 units)	
Crypto Assist Function	—	Yes	—	Yes

*HHA and JHA parts have the Crypto Assist Function built in. HHA and JHA options are not available for the S6E2GH or S6E2G3 parts. The HHA and JHA options are available on the S6E2GM, S6E2GK, and S6E2G2 parts.

Notes:

- For an explicit list of part numbers and the feature differences among them, see 13. Ordering Information
- See 14. Package Dimensions for detailed information on each package.

4. Product Features in Detail

32-bit ARM Cortex-M4F Core

- Up to 180 MHz frequency operation
- FPU built-in
- Support DSP instructions
- Memory protection unit (MPU): improves the reliability of an embedded system
- Integrated nested vectored interrupt controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit system timer (Sys Tick): system timer for OS task management

On-chip Memories

- Flash memory

This series is on-chip flash memories.

- Up to 1024 Kbytes
- Built-in flash accelerator for zero wait state
- Security function for code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to the I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to system bus of Cortex-M4F core.

- SRAM0: up to 128 Kbytes
- SRAM1: 32 Kbytes
- SRAM2: 32 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-/32-bit data width
- Up to 25-bit address bus
- Supports address/data multiplexing
- Supports external RDY function
- Supports scramble function
 - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
 - Possible to set two kinds of the scramble key
 - **Note:** It is necessary to use the Cypress provided software library to use the scramble function.

USB Interface (Max two channels)

The USB interface is composed of a Device and a Host.

- USB Device
 - USB 2.0 Full-speed supported
 - Max 6 EndPoint supported

- EndPoint 0 is control transfer
- EndPoint 1,2 can be selected bulk-transfer, interrupt-transfer or isochronous-transfer
- EndPoint 3 to 5 can select bulk-transfer or interrupt-transfer
 - EndPoint 1 to 5 comprise double buffer
 - The size of each endpoint is as follows.
 - Endpoint 0, 2 to 5: 64 byte
 - EndPoint 1: 256 byte

- USB Host

- USB2.0 Full-Speed/Low-Speed supported
- Bulk-transfer, interrupt-transfer, and isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet length supported
- Wake-up function supported

CAN Interface (Max one channel) Available on S6E2GM and S6E2GH Devices Only

- Compatible with CAN specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32-message buffer

Multi-function Serial Interface (Max 10 Channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 1 and channels 4 to 7.
- Operation mode is selectable for each channel from the following:
 - UART
 - CSIO (SPI)
 - LIN
 - I²C
 - I²S
- UART
 - Full-duplex double buffer
 - Selection with or without parity supported
 - Built-in dedicated baud rate generator
 - External clock available as a serial clock
 - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
 - Full-duplex double buffer
 - Built-in dedicated baud rate generator
 - Overrun error detect function available
 - Serial chip select function (ch 6 and ch 7 only)
 - Supports high-speed SPI (ch 4 and ch 6 only)
 - Data length 5 to 16-bit
- LIN
 - LIN protocol Rev.2.1 supported
 - Full-duplex double buffer
 - Master/slave mode supported
 - LIN break field generation (can change to 13- to 16-bit length)

- LIN break delimiter generation (can change to 1- to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)
- I²C
 - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
 - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported
- I²S
 - Using CSIO (SPI) (ch 1 only) and I²S clock generator
 - Supports two transfer protocol: I²S and MSB-justified
 - Master mode only

DMA Controller (Eight Channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller; 256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 Channels)

- 12-bit A/D Converter
 - Successive approximation type
 - Built-in three units
 - Conversion time: 0.5 μ s at 5 V
 - Priority conversion available (priority at two levels)
 - Scanning conversion mode
 - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

Base Timer (Max 16 channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer

- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer
- Event counter mode (External clock mode)

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 121 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.
See 6. Pin Descriptions and 7. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max two units)

The multi-function timer is composed of the following blocks:
Minimum resolution: 5.56 ns

- 16-bit free-run timer \times 3 ch/unit
- Input capture \times 4 ch/unit
- Output compare \times 6 ch/unit
- A/D activation compare \times 6 ch/unit
- Waveform generator \times 3 ch/unit
- 16-bit PPG timer \times 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC; Max two channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 32 pins
 - Both edges(Rise edge and Fall edge) detect
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs: a "hardware" watchdog and a "software" watchdog.

The hardware watchdog timer is clocked by low-speed internal CR oscillator. The hardware watchdog is thus active in any power saving mode except RTC mode and Stop mode.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator helps to verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 generator polynomial: 0x1021
- IEEE-802.3 CRC32 generator polynomial: 0x04C11DB7

SD Card Interface Available on S6E2GM, S6E2GH, and S6E2GK Devices Only

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Ethernet-MAC Available on S6E2GM, S6E2GK, and S6E2G2 Devices only

- Compliant with IEEE802.3 specification
- 10 Mbps/100 Mbps data transfer rates supported
- MII/RMII for external PHY device supported.
- MII: Max one channel
- RMII: Max one channel
- Full-duplex and half-duplex mode supported.
- Wake-ON-LAN supported
- Built-in dedicated descriptor-system DMAC
- Built-in 2 Kbytes transmit FIFO and 2 Kbytes receive FIFO.
- Compliant IEEE1558-2008 (PTP)

Smartcard Interface (Max 2 channels)

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
 - Transmitter: 8E2, 8O2, 8N2
 - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
 - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

Clock and Reset

- Clocks

Five clock sources (two external oscillators, two internal CR oscillators, and Main PLL) that are dynamically selectable.

 - Main clock: 4 MHz to 48 MHz
 - Sub clock: 30 kHz to 100 kHz
 - High-speed internal CR clock: 4 MHz
 - Low-speed internal CR clock: 100 kHz
 - Main PLL Clock

■ Resets

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timer reset
- Low-voltage detector reset
- Clock supervisor reset

Clock Supervisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include two-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, the low-voltage detector function generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

Crypto Assist Function

These features are enabled for the crypto assist function.

The dedicated middleware is necessary for this calculator operation.

- PKA (Public Key Accelerator)
 - PKA (Public Key Accelerator) is modular exponentiation calculation accelerator used of RSA Public Key crypto and so on.
 - Available bit length: Up to 2048-bit
- AES calculator
 - AES (Advanced Encryption Standard) calculator is a AES common key crypto accelerator which is compliant with FIPS (Federal Information Processing Standard Publication)197.
 - Available key length: 128/192/256-bit
 - CBC mode and ECB mode support
- External Bus Data Scramble
 - It enables to scramble input/output data of External Bus Interface.

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

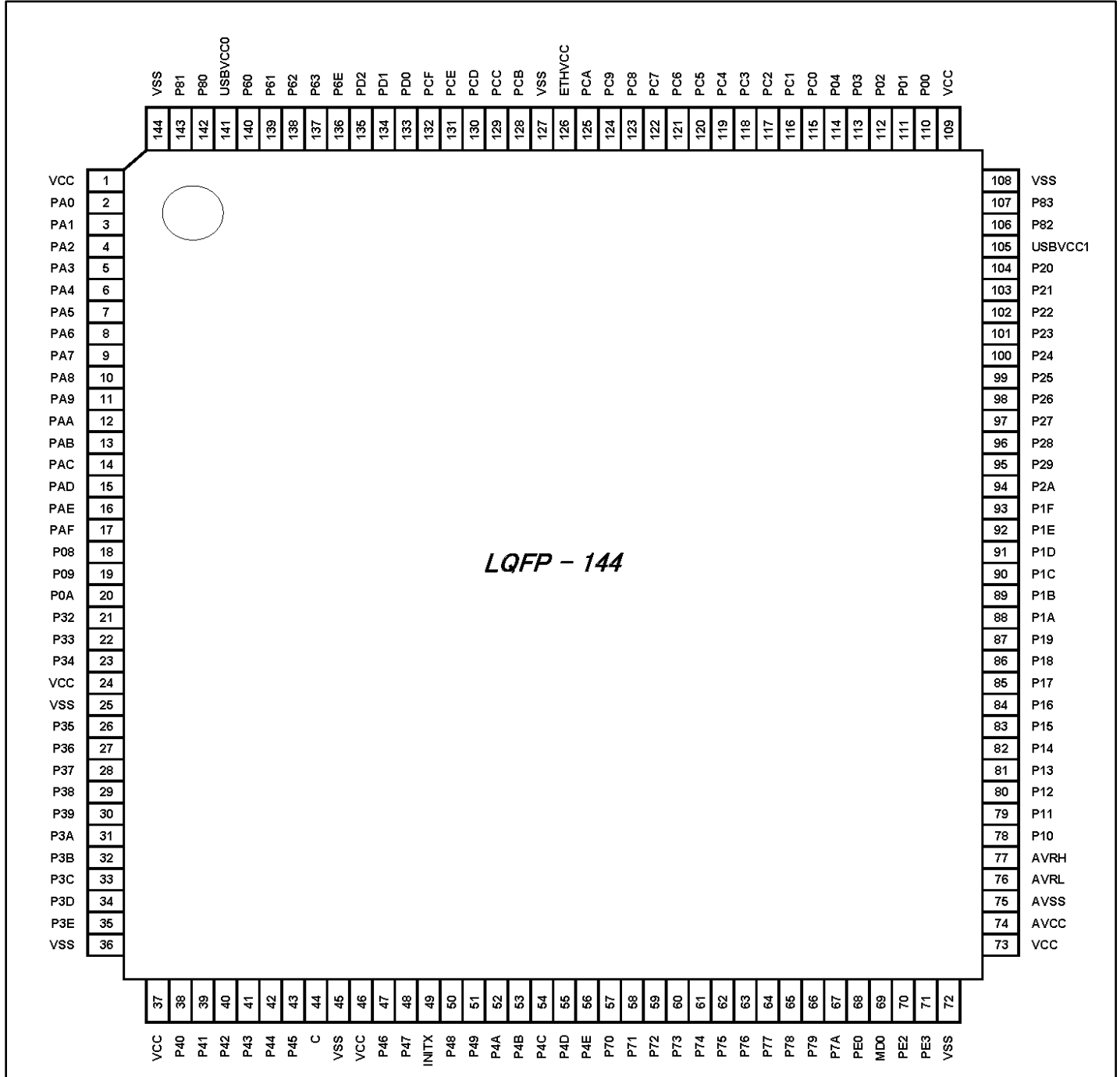
Unique value of the device (41-bit) is set.

Power Supply

- Four power supplies
 - Wide range voltage: VCC = 2.7 V to 5.5 V
 - Power supply for USB ch 0 I/O: USBVCC0 = 3.0 V to 3.6 V (when USB is used) = 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for USB ch 1 I/O: USBVCC1 = 3.0 V to 3.6 V (when USB is used) = 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for Ethernet-MAC I/O: ETHVCC = 3.0 V to 5.5 V (when Ethernet is used.)

5. Pin Assignments

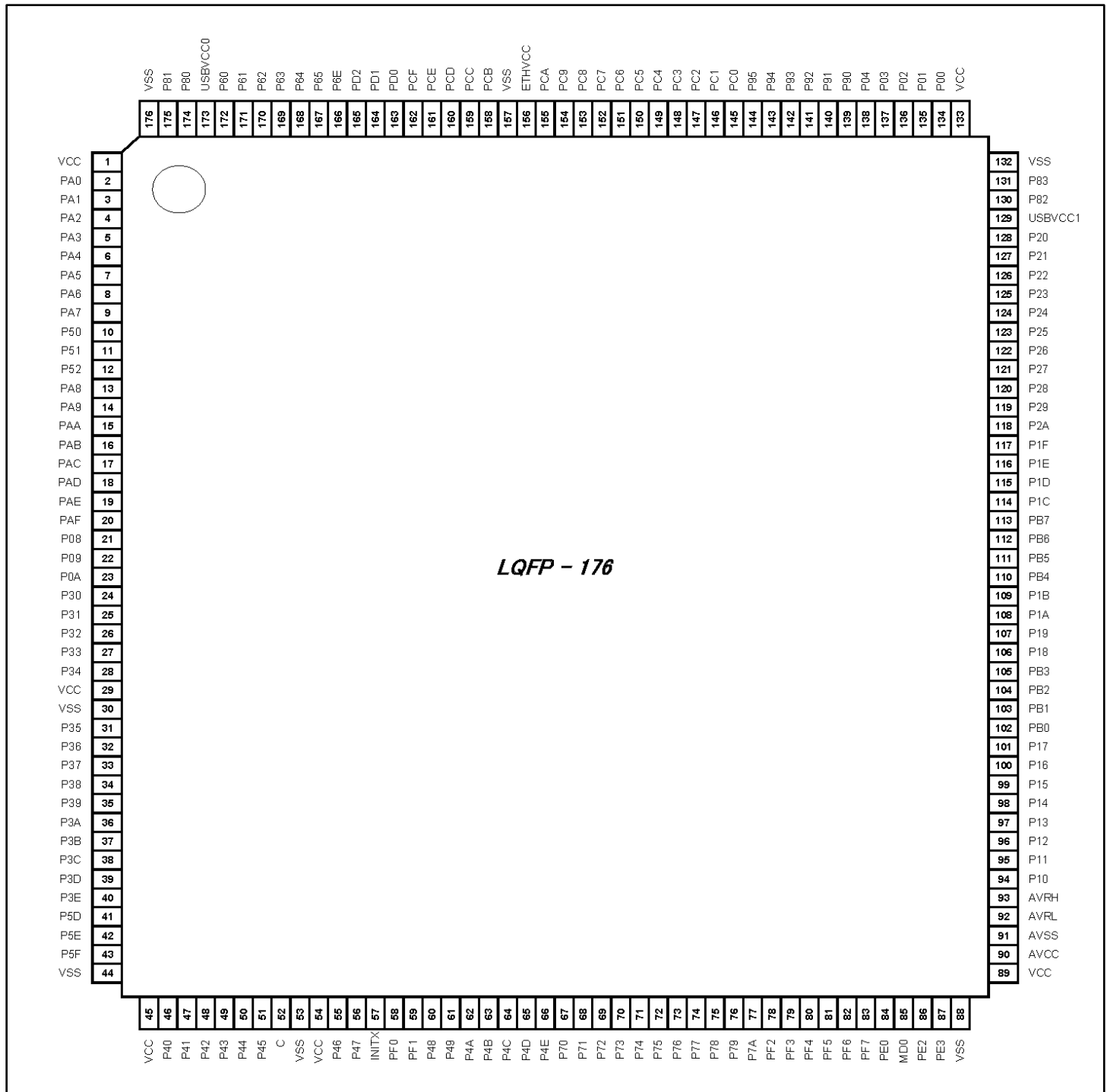
LQS144



Note:

- Only the GPIO function is shown on GPIO pins. See the table in [Pin Descriptions](#) for the full, multiplexed signal name.

LQP176



Note:

– Only the GPIO function is shown on GPIO pins. See the table in [Pin Descriptions](#) for the full, multiplexed signal name.

6. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
1	1	VCC	-	-
2	2	PA0	E	K
		RTO00_1 (PPG00_1)		
		TIOA8_0		
		INT00_0		
		MADATA00_0		
IC0_CIN_0				
3	3	PA1	E	I
		RTO01_1 (PPG01_1)		
		TIOA9_0		
		MADATA01_0		
IC0_DATA_0				
4	4	PA2	E	I
		RTO02_1 (PPG02_1)		
		TIOA10_0		
		MADATA02_0		
IC0_RST_0				
5	5	PA3	E	I
		RTO03_1 (PPG03_1)		
		TIOA11_0		
		MADATA03_0		
IC0_VPEN_0				
6	6	PA4	E	I
		RTO04_1 (PPG04_1)		
		TIOA12_0		
		MADATA04_0		
IC0_VCC_0				
7	7	PA5	E	K
		RTO05_1 (PPG05_1)		
		TIOA13_0		
		INT01_0		
		MADATA05_0		
IC0_CLK_0				

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
8	8	PA6	E	K
		DTTIOX_1		
		INT00_2		
		MADATA06_0		
9	9	PA7	E	K
		IC00_1		
		INT02_2		
		MADATA07_0		
		RTCCO_1		
		SUBOUT_1		
10	-	P50	E	I
		SCS72_0		
		IC01_1		
		TIOA8_2		
11	-	P51	E	I
		SCS73_0		
		IC02_1		
		TIOB8_2		
12	-	P52	E	I
		IC03_1		
		TIOA9_2		
13	10	PA8	I	Q
		SIN7_0		
		FRCK0_1		
		INT02_0		
		WKUP1		
		MADATA08_0		
14	11	PA9	N	I
		SOT7_0 (SDA7_0)		
		AIN1_1		
		MADATA09_0		
15	12	PAA	N	I
		SCK7_0 (SCL7_0)		
		BIN1_1		
		MADATA10_0		
16	13	PAB	E	K
		SCS70_0		
		ZIN1_1		
		INT03_0		
		MADATA11_0		
17	14	PAC	E	I
		SCS71_0		
		TIOB8_0		
		MADATA12_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
18	15	PAD	N	I
		SCK3_0 (SCL3_0)		
		TIOB9_0		
		MADATA13_0		
19	16	PAE	N	I
		ADTG_0		
		SOT3_0 (SDA3_0)		
		TIOB10_0		
		MADATA14_0		
20	17	PAF	I	K
		SIN3_0		
		TIOB11_0		
		INT16_0		
		MADATA15_0		
21	18	P08	E	K
		TIOB12_0		
		INT17_0		
		MDQM0_0		
22	19	P09	E	K
		TIOB13_0		
		INT18_0		
		MDQM1_0		
23	20	P0A	L	I
		ADTG_1		
		MCLKOUT_0		
24	-	P30	E	K
		MI2SWS1_1		
		RX0_1		
		TIOB11_2		
		INT01_2		
25	-	P31	E	I
		MI2SMCK1_1		
		TX0_1		
		TIOA12_2		
26	21	P32	L	K
		INT19_0		
		S_DATA1_0		
27	22	P33	L	I
		FRCK0_0		
		S_DATA0_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
28	23	P34	L	K
		IC03_0		
		INT00_1		
		S_CLK_0		
29	24	VCC	-	-
30	25	VSS	-	-
31	26	P35	L	K
		IC02_0		
		INT01_1		
		S_CMD_0		
32	27	P36	L	K
		IC01_0		
		INT02_1		
		S_DATA3_0		
33	28	P37	L	K
		IC00_0		
		INT03_1		
		S_DATA2_0		
34	29	P38	E	I
		ADTG_2		
		DTTIOX_0		
		S_WP_0		
35	30	P39	G	K
		RTO00_0 (PPG00_0)		
		TIOA0_1		
		AIN1_0		
		INT16_1		
		S_CD_0		
MAD24_0				
36	31	P3A	G	K
		RTO01_0 (PPG01_0)		
		TIOA1_1		
		BIN1_0		
		INT17_1		
		MAD23_0		
37	32	P3B	G	K
		RTO02_0 (PPG02_0)		
		TIOA2_1		
		ZIN1_0		
		INT18_1		
		MAD22_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
38	33	P3C	G	K
		SIN2_1		
		RTO03_0 (PPG03_0)		
		TIOA3_1		
		INT19_1		
		MAD21_0		
39	34	P3D	G	I
		SOT2_1 (SDA2_1)		
		RTO04_0 (PPG04_0)		
		TIOA4_1		
		MAD20_0		
40	35	P3E	G	I
		SCK2_1 (SCL2_1)		
		RTO05_0 (PPG05_0)		
		TIOA5_1		
		MAD19_0		
41	-	P5D	E	K
		SIN1_1		
		MI2SDI1_1		
		TIOB12_2		
		INT03_2		
42	-	P5E	E	I
		SOT1_1 (SDA1_1)		
		MI2SDO1_1		
		TIOA13_2		
43	-	P5F	E	I
		SCK1_1 (SCL1_1)		
		MI2SCK1_1		
		TIOB13_2		
44	36	VSS	-	-
45	37	VCC	-	-
46	38	P40	G	K
		SIN7_1		
		RTO10_0 (PPG10_0)		
		TIOA0_0		
		AIN0_0		
		INT23_0		
		MCSX7_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
47	39	P41	G	I
		SOT7_1 (SDA7_1)		
		RTO11_0 (PPG11_0)		
		TIOA1_0		
		BIN0_0		
		MCSX6_0		
48	40	P42	G	I
		SCK7_1 (SCL7_1)		
		RTO12_0 (PPG12_0)		
		TIOA2_0		
		ZIN0_0		
		MCSX5_0		
49	41	P43	G	K
		SCS70_1		
		RTO13_0 (PPG13_0)		
		TIOA3_0		
		INT04_0		
		MCSX4_0		
50	42	P44	G	I
		SCS71_1		
		RTO14_0 (PPG14_0)		
		TIOA4_0		
		MCSX3_0		
51	43	P45	G	I
		SCS72_1		
		RTO15_0 (PPG15_0)		
		TIOA5_0		
		MCSX2_0		
52	44	C	-	-
53	45	VSS	-	-
54	46	VCC	-	-
55	47	P46	D	S
		X0A		
56	48	P47	D	T
		X1A		
57	49	INITX	B	C

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
58	-	PF0	E	K
		SCS73_1		
		RX0_2		
		TIOA15_1		
		INT22_1		
59	-	PF1	E	K
		TX0_2		
		TIOB15_1		
		INT23_1		
60	50	P48	L	K
		SIN1_0		
		MI2SDI1_0		
		DTT11X_0		
		INT06_0		
		MRASX_0		
61	51	P49	L	I
		SOT1_0 (SDA1_0)		
		MI2SDO1_0		
		IC10_0		
		MCASX_0		
62	52	P4A	L	I
		SCK1_0 (SCL1_0)		
		MI2SCK1_0		
		IC11_0		
		MSDWEX_0		
63	53	P4B	L	K
		MI2SWS1_0		
		IC12_0		
		INT04_2		
		MCSX8_0		
64	54	P4C	L	K
		MI2SMCK1_0		
		IC13_0		
		INT05_2		
65	55	MSDCKE_0	L	K
		P4D		
		FRCK1_0		
		INT07_0		
		MSDCLK_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
66	56	P4E	L	Q
		SCK9_0 (SCL9_0)		
		INT05_0		
		WKUP2		
		MCSX1_0		
67	57	P70	L	I
		ADTG_7		
		SOT9_0 (SDA9_0)		
		MCSX0_0		
68	58	P71	I	K
		ADTG_8		
		SIN9_0		
		INT04_1		
		MRDY_0		
69	59	P72	E	I
		TIOB0_0		
		INT06_2		
		MAD00_0		
70	60	P73	E	K
		SIN8_0		
		TIOB1_0		
		INT20_0		
		MAD01_0		
71	61	P74	E	I
		SOT8_0 (SDA8_0)		
		TIOB2_0		
		MAD02_0		
72	62	P75	E	I
		SCK8_0 (SCL8_0)		
		TIOB3_0		
		MAD03_0		
73	63	P76	E	K
		SIN6_0		
		TIOB4_0		
		INT21_0		
		MAD04_0		
74	64	P77	L	I
		SOT6_0 (SDA6_0)		
		TIOB5_0		
		MAD05_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
75	65	P78	L	I
		SCK6_0 (SCL6_0)		
		AIN0_1		
		MAD06_0		
76	66	P79	E	K
		SCS60_0		
		BIN0_1		
		INT22_0		
		MAD07_0		
77	67	P7A	E	K
		SCS61_0		
		ZIN0_1		
		INT07_2		
		MAD08_0		
78	-	PF2	E	I
		SCS62_0		
		DTT11X_1		
		TIOA6_1		
		IC1_CLK_1		
79	-	PF3	E	K
		SCS63_0		
		FRCK1_1		
		TIOB6_1		
		INT05_1		
		IC1_VCC_1		
80	-	PF4	E	K
		IC10_1		
		TIOA7_1		
		INT06_1		
		IC1_VPEN_1		
81	-	PF5	E	K
		SIN3_1		
		IC11_1		
		TIOB7_1		
		INT07_1		
		IC1_RST_1		
82	-	PF6	E	K
		SOT3_1 (SDA3_1)		
		IC12_1		
		TIOA14_1		
		INT20_1		
		IC1_DATA_1		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
83	-	PF7	E	K
		SCK3_1 (SCL3_1)		
		IC13_1		
		TIOB14_1		
		INT21_1		
		IC1_CIN_1		
84	68	PE0	C	E
		MD1		
85	69	MD0	J	D
86	70	PE2	A	A
		X0		
87	71	PE3	A	B
		X1		
88	72	VSS	-	-
89	73	VCC	-	-
90	74	AVCC	-	-
91	75	AVSS	-	-
92	76	AVRL	-	-
93	77	AVRH	-	-
94	78	P10	F	M
		AN00		
		TIOA0_2		
		INT08_0		
		MNREX_0		
		IC1_CLK_0		
95	79	P11	F	L
		AN01		
		TIOB0_2		
		MNWEX_0		
		IC1_VCC_0		
96	80	P12	F	L
		AN02		
		TIOA1_2		
		MNCLE_0		
		IC1_VPEN_0		
97	81	P13	F	M
		AN03		
		SIN9_1		
		TIOB1_2		
		INT25_1		
		MNALE_0		
		IC1_RST_0		

Pin Number		Pin Name	I/O Circuit Type	Pin State Type
LQFP-176	LQFP-144			
98	82	P14	F	N
		AN04		
		SOT9_1 (SDA9_1)		
		TIOA2_2		
		IC1_DATA_0		
		TRACED0		
99	83	P15	F	N
		AN05		
		SCK9_1 (SCL9_1)		
		TIOB2_2		
		IC1_CIN_0		
		TRACED1		
100	84	P16	F	O
		AN06		
		SIN6_1		
		RX0_0		
		INT09_0		
		TRACED2		
101	85	P17	F	N
		AN07		
		SOT6_1 (SDA6_1)		
		TX0_0		
		TRACED3		
102	-	PB0	F	N
		AN16		
		SCK6_1 (SCL6_1)		
		TIOA9_1		
		TRACED8		
103	-	PB1	F	O
		AN17		
		SCS60_1		
		TIOB9_1		
		AIN0_2		
		INT08_1		
		TRACED9		
104	-	PB2	F	O
		AN18		
		SCS61_1		
		TIOA10_1		
		BIN0_2		
		INT09_1		
		TRACED10		