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MC9S12XHY256
Reference Manual
Covers MC9S12XHY Family

Data Sheet: Advance Information

This document contains information on a new product. Specifications and information here in are subject to change without notice.

S12
Microcontrollers

MC9S12XHY256RMV1

Rev. 1.01

03/2011

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A full list of family members and options is included in the appendices.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the CPU. For CPU information please refer to **CPU12-1** in the **CPU12 & CPU12X Reference Manual**.

Revision History

Date	Revision Level	Description
Jun,3,2010	0.11	update block: TIM SCI PIM Chapter1 update Table A-6., “5-V I/O Characteristics, item 11/12,unit is KΩ and uA update A.1.10.1, “Typical Run Current Measurement Conditions update Table A-6., “5-V I/O Characteristics, 4(a) , remove V C contitions update Table A-6., “5-V I/O Characteristics,4(b), remove temperature update Table A-10., “Run and Wait Current Characteristics, remove item update Table A-11., “Pseudo Stop and Full Stop Current, -10a/10b/11/12/13/14,remove temperature except -40/25/150 -15, change to FSP mode remove Typeical Run supply table update Table A-11., “Pseudo Stop and Full Stop Current, add LCP FSP mode
Jun,11,2010	0.12	update Appendix electrical parameter -Table A-6., “5-V I/O Characteristics 4a 9 10 11 12 Table A-11., “Pseudo Stop and Full Stop Current,10a,11a,12a,14,15 -Table A-4./A-721 LCD/Motor Driver pad can only be work under >4.5V -A.1.3.1/A-718, change to 4.5v to 5.5v -remove 12 bit resolution at table Table A-12./A-731 update chapter MMC to Ver04.11 3.1/3-157 update chapter MSCAN to Ver03.12 update Table D-2./D-768,all parts has 2x CAN and SCI
Mar,25,2011	1.01	update Appendix electrical parameter value Table A-11., “Pseudo Stop and Full Stop Current, Table A-9., “Module Run Supply Currents Table A-6., “5-V I/O Characteristics, item 4b update Appendix, change classifications or conditions Table A-6., “5-V I/O Characteristics, item 4b, change from 80c to 150c Table A-11., “Pseudo Stop and Full Stop Current,item 11b,change from P to C fix typo Table A-6., “5-V I/O Characteristics, 11 and 12, resistance not current

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Chapter 1
Device Overview MC9S12XHY-Family

1.1 Introduction

The MC9S12XHY family is an optimized, automotive, 16-bit microcontroller product line that is specifically designed for entry level instrument clusters. This family also services generic automotive applications requiring CAN, LCD, Motor driver control or LIN/SAE J2602. Typical examples of these applications include instrument clusters for automobiles and 2 or 3 wheelers, HVAC displays, general purpose motor control and body controllers.

The MC9S12XHY family uses many of the same features found on the MC9S12XS family and MC9S12HY/HA family, including error correction code (ECC) on flash memory, a separate data-flash module for diagnostic or data storage, a fast analog-to-digital converter (ATD) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12XHY family features a 40x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (MC) consisting of up to 16 high current outputs. The device is capable of stepper motor stall detection (SSD) via hardware or software, please contact Freescale sales office for detailed information on software SSD.

The MC9S12XHY family deliver all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of Freescale's existing 8-bit and 16-bit MCU families. Like the MC9S12HY/HA family, the MC9S12XHY family run 16-bit wide accesses without wait states for all peripherals and memories. The MC9S12XHY family is available in 112-pin LQFP and 100-pin LQFP package options. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

1.2 Features

This section describes the key features of the MC9S12XHY family.

1.2.1 MC9S12XHY Family Comparison

Table 1-1 provides a summary of different members of the MC9S12XHY family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1-1. MC9S12XHY Family

Feature	MC9S12XHY128		MC9S12XHY256	
CPU	HCS12X V1			
Flash memory (ECC)	128Kbytes		256 Kbytes	
Data flash (ECC)	8 Kbytes			
RAM	8 Kbytes		12kbyte	
Pin Quantity	100	112	100	112
CAN	2			
SCI	2			
SPI	1			
IIC	1			
Timer 0	8 ch x 16-bit			
Timer 1	8 ch x 16-bit			
PWM	8 ch x 8-bit or 4ch x16-bit			
ADC (10-bit)	8 ch	12ch	8ch	12 ch
Stepper Motor Controller	4			
Stepper Stall Detecter	4			
LCD Driver (FPxBP)	38x4	40x4	38x4	40x4
Key Wakeup Pins	23	25	23	25
Frequency Modulated PLL	Yes			
External osc (4–16 MHz Pierce with loop control)	Yes			

Table 1-1. MC9S12XHY Family

Feature	MC9S12XHY128	MC9S12XHY256
Internal 1 MHz RC osc	No	
Supply voltage	4.5 V – 5.5 V	
RTI, LVI, CRG, RST, COP, DBG, POR, API	Yes	
Execution speed	Static-40MHz	

1.2.2 Chip-Level Features

On-chip modules available within the family include the following features:

- CPU12XV1 CPU core
- Up to 256 Kbyte on-chip flash with ECC
- 8Kbyte data flash with ECC
- Up to 12Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 4–16 MHz amplitude controlled Pierce oscillator
- Two timer modules (TIM0 and TIM1) supporting input/output channels that provide a range of 16-bit input capture, output compare, counter and pulse accumulator functions
- Pulse width modulation (PWM) module with up to 8 x 8-bit channels
- Up to 12-channel, 10-bit resolution successive approximation analog-to-digital converter (ATD)
- Up to 40x4 LCD driver
- PWM motor controller (MC) with up to 16 high current drivers
- Output slew rate control on Motor driver pad
- One serial peripheral interface (SPI) module
- One Inter-IC bus interface (IIC) module
- Two serial communication interface (SCI) module supporting LIN communications
- Two multi-scalable controller area network (MSCAN) module (supporting CAN protocol 2.0A/B)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API)
- Stepper Motor Controller with up to drivers for up to 4 motors
- Four Stepper Stall Detector modules (one for each motor)
- Up to 25 key wakup inputs

1.3 Module Features

The following sections provide more details of the modules implemented on the MC9S12XHY family.

1.3.1 S12 16-Bit Central Processor Unit (CPU)

The CPU12X is a high-speed, 16-bit processing unit that has a programming model identical to that of the industry standard M68HC11 central processor unit (CPU).

- Upward compatible with S12 instruction set, with the exception of five Fuzzy instructions (MEM, WAV, WAVR, REV, REVW) which have been removed
- Enhanced indexed addressing
- Access to large data segments independent of PPAGE

1.3.2 On-Chip Flash with ECC

On-chip flash memory on the MC9S12XHY features the following:

- Up to 256Kbyte of program flash memory
  - 64data bits plus 8 syndrome ECC (error correction code) bits allow single bit error correction and double fault bit detection
  - Erase sector size 1024bytes
  - Automated program and erase algorithm
  - Protection scheme to prevent accidental program or erase
  - Security option to prevent unauthorized access
  - Sense-amp margin level setting for reads
- 8Kbyte data flash space
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 256 bytes
  - Automated program and erase algorithm
  -

1.3.3 On-Chip SRAM

- Up to 12Kbytes of general-purpose RAM

1.3.4 Main External Oscillator (XOSC)

- Loop control Pierce oscillator using a 4 MHz to 16 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals

1.3.5 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
    - -

1.3.6 Clocks and reset generation(CRG)

- COP watchdog
- Real time interrupt
- Clock monitor
- Fast wake up from STOP in self clock mode

1.3.7 System Integrity Support

- Power-on reset (POR)
- System reset generation
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Real time interrupt (RTI)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection
  - Initialized out of reset using option bits located in flash memory
- Clock monitor supervising the correct function of the oscillator
- Temperature sensor

1.3.8 Timer (TIM0)

- 8x 16-bit channels for input capture
- 8x 16-bit channels for output compare
- 16-bit free-running counter with 8-bit precision prescaler
- 1 x 16-bit pulse accumulator

1.3.9 Timer (TIM1)

- 8x 16-bit channels for input capture
- 8x 16-bit channels for output compare

- 16-bit free-running counter with 8-bit precision prescaler
- 1 x 16-bit pulse accumulator

1.3.10 Liquid crystal display driver (LCD)

- Configurable for up to 40 frontplanes and 4 backplanes or general-purpose input or output
- 5 modes of operation allow for different display sizes to meet application requirements
- Unused frontplane and backplane pins can be used as general-purpose I/O

1.3.11 Motor Controller (MC)

- PWM motor controller (MC) with up to 16 high current drivers
- Each PWM channel switchable between two drivers in an H-bridge configuration
- Left, right and center aligned outputs
- Support for sine and cosine drive
- Dithering
- Output slew rate control

1.3.12 Pulse Width Modulation Module (PWM)

- 8channel x 8-bit or 4channel x 16-bit pulse width modulator
  - — Programmable period and duty cycle per channel
  - — Center-aligned or left-aligned outputs
  - — Programmable clock select logic with a wide range of frequencies

1.3.13 Inter-IC bus Module (IIC)

- 1 Inter-IC (IIC) bus module which has following feature
  - — Multi-master operation
  - — Soft programming for one of 256 different serial clock frequencies
  - — General Call(Broadcast) mode support
  - — 10-bit address support

1.3.14 Controller Area Network Module (MSCAN)

- 1 Mbit per second, CAN 2.0 A, B software compatible
  - — Standard and extended data frames
  - — 0–8 bytes data length
  - — Programmable bit rate up to 1 Mbps
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization
- Flexible identifier acceptance filter programmable as:

  - 2 x 32-bit
  - 4 x 16-bit
  - 8 x 8-bit
- Wakeup with integrated low pass filter option
- Loop back for self test
- Listen-only mode to monitor CAN bus
- Bus-off recovery by software intervention or automatically
- 16-bit time stamp of transmitted/received messages

1.3.15 Serial Communication Interface Module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN

1.3.16 Serial Peripheral Interface Module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.3.17 Analog-to-Digital Converter Module (ATD)

- Up to 12-channel, 10-bit analog-to-digital converter
  - 3 us single conversion time
  - 8-/10 bit resolution
  - Left or right justified result data
  - Internal oscillator for conversion in stop modes
  - Wakeup from low power modes on analog comparison > or <= match
  - Continuous conversion mode
  - Multiple channel scans
- Pins can also be used as digital I/O

1.3.18 On-Chip Voltage Regulator (VREG)

- Linear voltage regulator with bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR) circuit
- Low-voltage reset (LVR)

1.3.19 Background Debug (BDM)

- Background debug module (BDM) with single-wire interface
- Non-intrusive memory access commands
- Supports in-circuit programming of on-chip nonvolatile memory

1.3.20 Debugger (DBG)

- Three comparators A, B, C, and D to monitor CPU buses
- Trace buffer with depth of 64 entries
- Comparator A and C compares full address bus and 16-bit data bus with mask register
- Three modes: simple address/data match, inside address range, or outside address range

1.3.21 SSD

- Programmable Full Step State
- Programmable Integration polarity
- Blanking (recirculation) state
- 16-bit Integration Accumulator register
- 16-Bit Modulus Down Counter with interrupt
- Multiplex two stepper motors

1.3.22 INT (interrupt module)

- Seven levels of nested interrupts
- Flexible assignment of interrupt sources to each interrupt level.
- External non-maskable high priority interrupt (XIRQ)
- The following inputs can act as Wake-up Interrupts
  - IRQ and non-maskable XIRQ
  - CAN receive pins
  - SCI receive pins
  - Depending on the package option up to 25 pins on ports R, S, T and AD, configurable as rising or falling edge sensitive
-

1.4 Block Diagram

Figure 1-1 shows a block diagram of the MC9S12XHY-Family devices

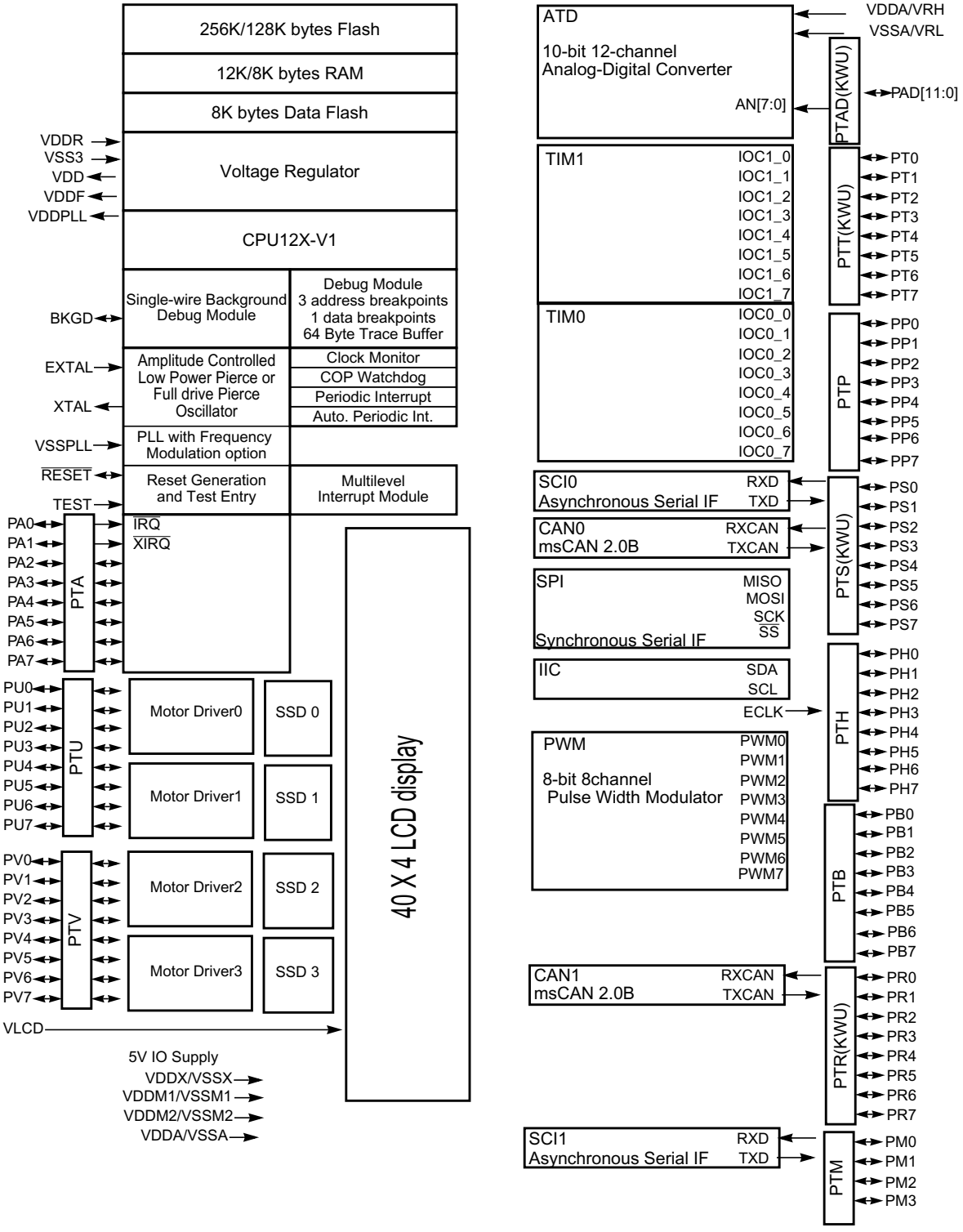

Figure 1-1. MC9S12XHY-Family 112 LQFP Block Diagram

1.5 Device Memory Map

Table 1-2 shows the device register memory map.

Table 1-2. Device Register Memory Map

Address	Module	Size (Bytes)	reference pages
0x0000–0x0009	PIM (port integration module)	10	768
0x000A–0x000B	MMC (memory map control)	2	769
0x000C–0x000D	PIM (port integration module)	2	769
0x000E–0x000F	Reserved	2	
0x0010–0x0017	MMC (memory map control)	8	769
0x0018–0x0019	Reserved	2	
0x001A–0x001B	Device ID register	2	770
0x001C–0x001F	PIM (port integration module)	4	770
0x0020–0x002F	DBG (debug module)	16	771
0x0030–0x0033	Reserved	4	
0x0034–0x003F	ECRG (clock and reset generator)	12	772
0x0040–0x006F	TIM0 (timer module)	48	773
0x0070–0x009F	ATD (analog-to-digital converter 10 bit 8-channel)	48	775
0x00A0–0x00C7	PWM (pulse-width modulator 8 channels)	40	776
0x00C8–0x00CF	SCI0 (serial communications interface)	8	778
0x00D0–0x00D7	SCI1 (serial communications interface)	8	779
0x00D8–0x00DF	SPI (serial peripheral interface)	8	779
0x00E0–0x00E7	IIC (Inter IC bus)	8	780
0x00E8–0x00FF	Reserved	24	
0x0100–0x0113	FTMR control registers	20	781
0x0114–0x011F	Reserved	12	
0x0120-0x012F	INT (interrupt module)	16	782
0x0130–0x013F	Reserved	16	
0x0140–0x017F	CAN0	64	783
0x0180–0x01BF	CAN1	64	785
0x1C0–0x1FF	MC(motor controller)	64	786
0x0200–0x021F	LCD	32	788
0x0220–0x0227	Stepper Stall Detector 0 (SSD0)	8	789
0x0228–0x022F	Stepper Stall Detector 1 (SSD1)	8	790
0x0230–0x0237	Stepper Stall Detector 2 (SSD2)	8	790
0x0238–0x023F	Stepper Stall Detector 3 (SSD3)	8	791

Address	Module	Size (Bytes)	reference pages
0x0240–0x029F	PIM (port integration module)	96	791
0x02A0–0x02CF	TIM1(timer module)	48	795
0x02D0–0x02EF	Reserved	32	
0x02F0–0x02F7	Voltage regulator	8	797
0x02F8–0x02FF	Reserved	8	
0x0300–0x03FF	Reserved	256	
0x0400–0x07FF	Reserved	1024	

NOTE

Reserved register space shown in Table 1-2 is not allocated to any module. This register space is reserved for future use. Writing to these locations have no effect. Read access to these locations returns zero.

Figure 1-2 shows MC9S12XHY family CPU and BDM local address translation to the global memory map. It indicates also the location of the internal resources in the memory map.

Accessing the reserved area in the range of 0x0C00 to 0x0FFF will return undefined data values.

A CPU access to any unimplemented space causes an illegal address reset.

The range between 0x10_0000 and 0x13_FFFF is mapped to DFLASH (Data Flash). The DFLASH block sizes are listed in Table 1-3.

Table 1-3. Derivative Dependent Memory Parameters of Device Internal Resources

Device	FLASH_LOW	SIZE/ PPAGE(1)	RAM_LOW	SIZE/ RPAGE(2)	DF_HIGH	SIZE/ EPAGE(3)
S12XHY256	0x7C_0000	256K / 16	0x0F_D000	12K / 3	0x10_1FFF	8K / 8
S12XHY128	0x7E_0000	128K / 8	0x0F_E000	8K / 2	0x10_1FFF	8K / 8

1. Number of 16K pages addressable via PPAGE register
2. Number of 4K pages addressing the RAM.
3. Number of 1K pages addressing the DFLASH