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MC9S12XHZ512

Data Sheet

Covers
MC9S12XHZ384, MC9S12XHZ256

HCS12X
Microcontrollers

MC9S12XHZ512
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The following revision history table summarizes changes contained in this document. This document contains information for all constituent modules, with the exception of the S12X CPU. For S12X CPU information please refer to CPU12XV2 in the CPU12/CPU12X Reference Manual.

Revision History

Date	Revision Level	Description
January 5, 2006	01.00	New Book
April 20, 2006	01.01	Updated block guide versions
July 28, 2006	01.02	Made minor corrections
January 8, 2007	01.03	Added MC9S12XHZ384 and MC9S12XHZ256
August 20, 2007	01.04	Updated slew rates
November 4, 2008	01.05	Corrected typos on pinout diagram
October 14, 2010	01.06	Added PartID. Minor updates to ECT, SCI, IIC and XGATE sections.

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Chapter 1
MC9S12XHZ Family Device Overview

1.1 Introduction

Targeted at automotive instrumentation applications, the MC912XHZ family of microcontrollers is a fully pin-compatible extension to the existing MC9S12HZ family. It offers not only a larger memory but also incorporates all the architectural benefits of the new S12X-based family to deliver significantly higher performance. The MC9S12XHZ family retains the low cost, power consumption, EMC and code-size efficiency advantages currently associated with the MC9S12 products.

Based around S12X core, the MC912XHZ family runs 16-bit wide accesses without wait states for all peripherals and memories. The MC912XHZ family also features a new flexible interrupt handler, which allows multilevel nested interrupts.

The MC912XHZ family features the performance boosting XGATE co-processor. The XGATE is programmable in “C” language and runs at twice the bus frequency of the S12. Its instruction set is optimized for data movement, logic and bit manipulation instructions. Any peripheral module can be serviced by the XGATE.

The MC912XHZ family contains up to 512K bytes of Freescale Semiconductor’s industry leading, full automotive qualified Split-Gate Flash memory, with 4K bytes of additional integrated data EEPROM and up to 32K bytes of static RAM.

The MC912XHZ family features a 32x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (MC) consisting of up to 24 high current outputs suited to drive six stepper motors with stall detectors (SSD) to simultaneously calibrate the pointer reset position of each motor. It also features two MSCAN modules, each with a FIFO receiver buffer arrangement, and input filters optimized for Gateway applications handling numerous message identifiers.

In addition, the MC912XHZ family is composed of standard on-chip peripherals including two asynchronous serial communications interfaces (SCI0 and SCI1), one serial peripheral interface (SPI), two IIC-bus interface (IIC0 and IIC1), an 8-channel 16-bit enhanced capture timer (ECT), a 16-channel, 10-bit analog-to-digital converter (ADC), and one 8-channel pulse width modulator (PWM).

The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. The new fast-exit from STOP mode feature can further improve system power consumption. In addition to the I/O ports available in each module, 8 general-purpose I/O pins are available with interrupt and wake-up capability from stop or wait mode.

The MC912XHZ family is available in 112-pin LQFP and 144-pin LQFP packages. The 144-pin LQFP package option provides a full 16-bit wide non-multiplexed external bus interface.

1.1.1 Features

- HCS12X Core
  - 16-bit HCS12X CPU
    - Upward compatible with MC9S12 instruction set
    - Interrupt stacking and programmer's model identical to MC9S12
    - Instruction queue
    - Enhanced indexed addressing
    - Enhanced instruction set
  - EBI (external bus interface)
  - MMC (module mapping control)
  - INT (interrupt controller)
  - DBG (debug module to monitor HCS12X CPU and XGATE bus activity)
  - BDM (background debug mode)
- XGATE (peripheral coprocessor)
  - Parallel processing module off loads the CPU by providing high-speed data processing and transfer
  - Data transfer between Flash EEPROM, RAM, peripheral modules, and I/O ports
- Memory
  - 512K, 384K, 256K byte Flash EEPROM
  - 4K byte EEPROM
  - 32K, 28K, 16K byte RAM
- CRG (clock and reset generator)
  - Low noise/low power Pierce oscillator
  - PLL
  - COP watchdog
  - Real time interrupt
  - Clock monitor
  - Fast wake-up from stop mode
- Analog-to-digital converter
  - 16 channels, 10-bit resolution
  - External conversion trigger capability
- ECT (enhanced capture timer)
  - 16-bit main counter with 8-bit prescaler
  - 8 programmable input capture or output compare channels
  - Four 8-bit or two 16-bit pulse accumulators
- PIT (periodic interrupt timer)
  - Four timers with independent time-out periods
  - Time-out periods selectable between 1 and 2^{24} bus clock cycles

- 8 PWM (pulse-width modulator) channels
  - Programmable period and duty cycle
  - 8-bit 8-channel or 16-bit 4-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Two 1-Mbps, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit, or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error, and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self-test operation
- Two IIC (Inter-IC bus) Modules
  - Compatible with IIC bus standard
  - Multi-master operation
  - Broadcast mode
- Serial interfaces
  - Two asynchronous serial communication interfaces (SCI) with additional LIN support and selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
  - Synchronous Serial Peripheral Interface (SPI)
- Liquid crystal display (LCD) driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general-purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general-purpose I/O
- PWM motor controller (MC) with 24 high current drivers
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control
- Six stepper stall detectors (SSD)
  - Full step control during return to zero
  - Voltage detector and integrator / sigma delta converter circuit
  - 16-bit accumulator register
  - 16-bit modulus down counter

- On-Chip Voltage Regulator
  - Two parallel, linear voltage regulators with bandgap reference
  - Low-voltage detect (LVD) with low-voltage interrupt (LVI)
  - Power-on reset (POR) circuit
  - 3.3-V–5.5-V operation
  - Low-voltage reset (LVR)
  - Ultra low-power wake-up timer
- 144-pin LQFP and 112-pin LQFP packages
  - I/O lines with 5-V input and drive capability
  - Input threshold on external bus interface inputs switchable for 3.3-V or 5-V operation
  - 5-V A/D converter inputs
  - 8 key wake up interrupts with digital filtering and programmable rising/falling edge trigger
- Operation at 80 MHz equivalent to 40-MHz bus speed
- Development support
  - Single-wire background debug™ mode (BDM)
  - Four on-chip hardware breakpoints

1.1.2 Modes of Operation

User modes:

- Normal and emulation operating modes
  - Normal single-chip mode
  - Normal expanded mode
  - Emulation of single-chip mode
  - Emulation of expanded mode
- Special Operating Modes
  - Special single-chip mode with active background debug mode
  - Special test mode (**Freescale use only**)

Low-power modes:

- System stop modes
  - Pseudo stop mode
  - Full stop mode
- System wait mode

1.1.3 Block Diagram

Figure 1-1 shows a block diagram of the MC912XHZ family.

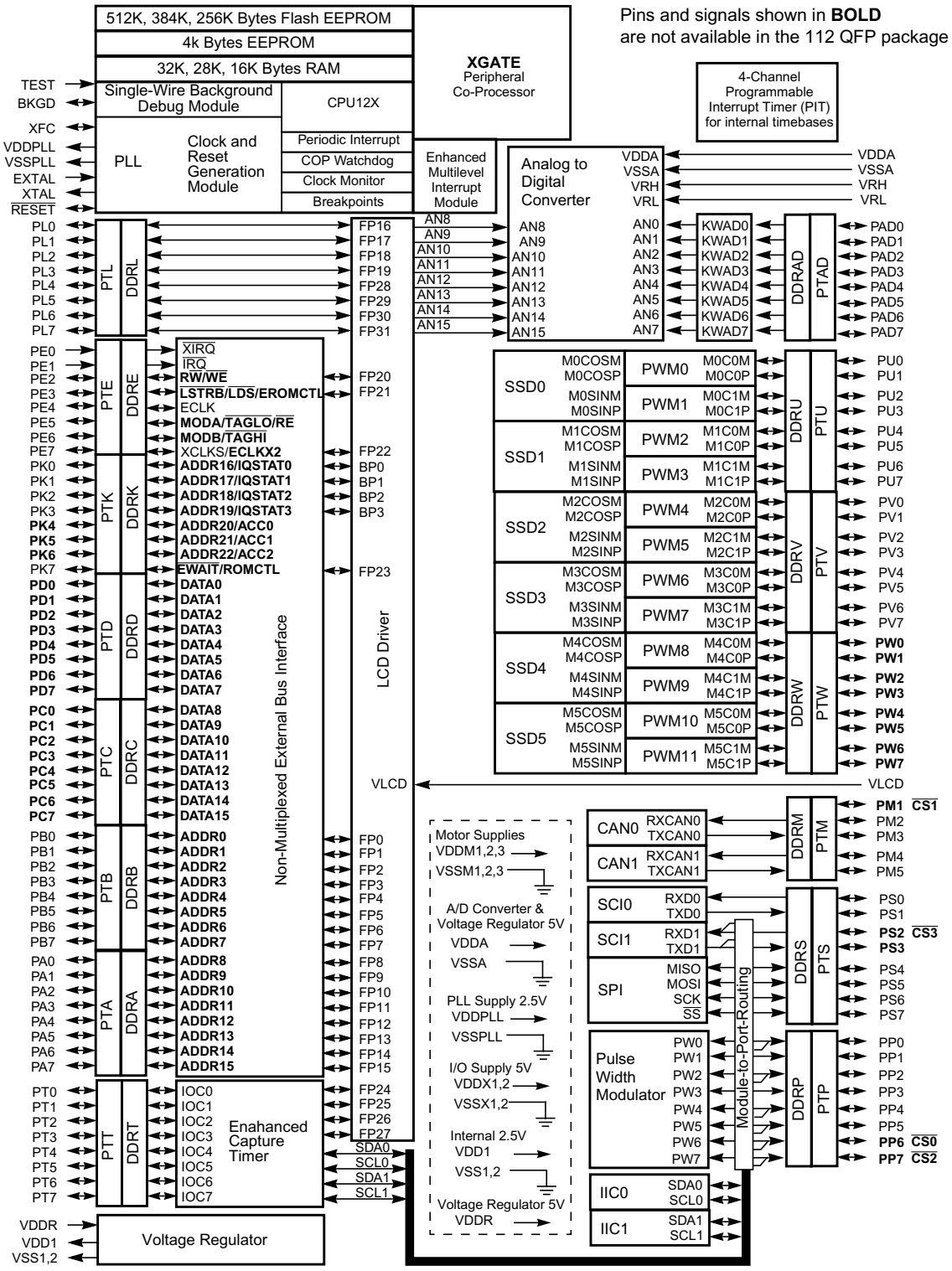

Figure 1-1. MC9S12XHZ Family Block Diagram