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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# MC9S12ZVC-Family Reference Manual and Datasheet

***S12 MagniV Microcontrollers***

MC9S12ZVCRMV2
Rev. 2.0
26-March-2018

*nxp.com*

The MC9S12ZVC family of microcontrollers is targeted at use in safety relevant systems and has been developed using an ISO26262 compliant development system under the NXP Safe Assure Program. For more details of the NXP Safe Assure program, refer to : NXP Safe Assure

For more details of how to use the device in safety relevant systems refer to the MC9S12ZVC Safety Manual at nxp.com

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to nxp.com/

A full list of family members and options is included in device overview section.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the S12Z CPU. For S12ZCPU information please refer to the CPU S12Z Reference Manual.

## Revision History

| Date | Revision Level | Description |
|---|---|---|
| 22-August-2016 | Rev 1.6 | Added item 18 and 19 Table E-1 Bandgap voltage and temperature dependency<br>Changed item 5 Table H-2 ACMP input offset<br>Added operating condition for C part to Table A-5 |
| 13-October-2016 | Rev 1.7 | Corrected Table 1-1 Two SCIs for 48pin packages. Corrected typo in table H-2 item 5 |
| 2-January-2018 | Rev 1.8 | Corrected Package Information for 64LQFP Exposed Pad |
| 29-January-2018 | Rev 1.9 | Corrected Package Information for 64LQFP Exposed Pad |
| 26-March-2018 | Rev 2.0 | Updated Appendix A MCU Electrical Specifications |

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# Chapter 1
# Device Overview MC9S12ZVC-Family

## Revision History

| Rev. No. (Item No.) | Date (Submitted By) | Substantial Change(s) |
|---|---|---|
| V0.01 | 9-April-2013 | • Initial Version |
| V0.02 | 22-August-2013 | • Added Section 1.13.3 Flash IFR Mapping<br>• Updated Section 1.14.1 ADC Calibration |
| V0.03 | 10-September-2013 | • Added Table 1-3<br>• Added S12ZVCA and S12ZVC Table 1-1 |
| V0.04 | 7-February-2014 | • Added 12K RAM, new maskset and part ID, feedback from shared review |
| V0.05 | 6-March-2014 | • Changed maskset N23N<br>• Changed Package 48 LQFP without EP |
| V0.06 | 28-April-2014 | • Removed VRL functionality from PAD4 |

## 1.1 Introduction

The MC9S12ZVC-Family is a new member of the S12 MagniV product line integrating a battery level (12V) voltage regulator, supply voltage monitoring, high voltage inputs and a CAN physical interface. It's primarily targeting at CAN nodes like sensors, switch panels or small actuators. It offers various low-power modes and wakeup management to address state of the art power consumption requirements.

Some members of the MC9S12ZVC-Family are also offered for high temperature applications requiring AEC-Q100 Grade 0 (-40°C to +150°C ambient operating temperature range).

The MC9S12ZVC-Family is based on the enhanced performance, linear address space S12Z core and delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings.

## 1.2 Features

This section describes the key features of the MC9S12ZVC-Family. It documents the superset of features within the family. Section 1.2.1 MC9S12ZVC-Family Comparison provides information to help access the correct information for a particular part within the family.

### 1.2.1 MC9S12ZVC-Family Comparison

Table 1-1 provides a summary of the MC9S12ZVC-Family. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

**Table 1-1. MC9S12ZVC-Family devices**

| Feature | S12ZVCA | | | | S12ZVCA | | | | S12ZVC | | | | S12ZVC | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **192** | **128** | **96** | **64** | **192** | **128** | **96** | **64** | **192** | **128** | **96** | **64** | **192** | **128** | **96** | **64** |
| Package option | 64-pin LQFP-EP | | | | 48-pin LQFP | | | | 64-pin LQFP-EP | | | | 48-pin LQFP | | | |
| Temperature Option (°C ambient) | -40 to 105/125/150 | | | | -40 to 85/105/125 | | | | -40 to 105/125/150 | | | | -40 to 85/105/125 | | | |
| Core | S12Z | | | | S12Z | | | | S12Z | | | | S12Z | | | |
| Flash memory (ECC) [KByte] | 192 | 128 | 96 | 64 | 192 | 128 | 96 | 64 | 192 | 128 | 96 | 64 | 192 | 128 | 96 | 64 |
| EEPROM (ECC) [KByte] (4-byte erasable) | 2 | 2 | 2 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 2 | 1 | 2 | 2 | 2 | 1 |
| RAM (ECC) [KByte] | 12 | 8 | 8 | 4 | 12 | 8 | 8 | 4 | 12 | 8 | 8 | 4 | 12 | 8 | 8 | 4 |
| High Speed CAN Physical Layer | 1 | | | | 1 | | | | 1 | | | | 1 | | | |
| High Voltage Inputs | 2 | | | | 2 | | | | 2 | | | | 2 | | | |
| Vreg for CAN PHY with ext. ballast (BCTLC) | yes | | | | yes | | | | yes | | | | yes | | | |
| VDDX/VSSX pins | 2/2 | | | | 2/2 | | | | 2/2 | | | | 2/2 | | | |
| msCAN | 1 | | | | 1 | | | | 1 | | | | 1 | | | |
| SCI | 2 | | | | 2 | | | | 2 | | | | 2 | | | |
| SPI | 2 | | | | 1 | | | | 2 | | | | 1 | | | |
| IIC | 1 | | | | 1 | | | | 1 | | | | 1 | | | |
| SENT (Transmitter) | 1 | | | | 1 | | | | 1 | | | | 1 | | | |
| 16-bit Timer channels | 8 | | | | 4 | | | | 8 | | | | 4 | | | |
| 16-bit Timer channels (20 ns resolution[1]) | 4 | | | | 4 | | | | 4 | | | | 4 | | | |
| 16-bit PWM channels (20 ns resolution[(1)]) | 4 | | | | 3 | | | | 4 | | | | 3 | | | |
| 16-bit PWM channels | 4 | | | | 4 | | | | 4 | | | | 4 | | | |
| 12-bit ADC channels | 16 | | | | 10 | | | | - | | | | - | | | |
| 10-bit ADC channels | - | | | | - | | | | 16 | | | | 10 | | | |
| 8-bit DAC | 1 | | | | 1 | | | | - | | | | - | | | |
| ACMP 5V (with rail-to-rail inputs) | 2 | | | | 2 | | | | - | | | | - | | | |
| EVDD (20 mA source) | 1 | | | | 1 | | | | 1 | | | | 1 | | | |
| Open Drain (5V GPIOs with disabled PMOS) | 10 | | | | 5 | | | | 10 | | | | 5 | | | |
| N-GPIO (25mA sink) | 4 | | | | 4 | | | | 4 | | | | 4 | | | |
| General purpose I/O | 42 | | | | 28 | | | | 42 | | | | 28 | | | |

1 at 25 MHz bus frequency

## 1.3 Chip-Level Features

On-chip modules available within the family include the following features:

- S12Z CPU core
- Up to 192 Kbyte on-chip flash with ECC
- Up to 2 Kbyte EEPROM with ECC
- Up to 12Kbyte on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range
- 4-20MHz amplitude controlled pierce oscillator
- Internal COP (watchdog) module
- Analog-to-digital converter (ADC) with 12-bit resolution and up to 16 channels available on external pins
- Two analog comparators (ACMP) with rail-to-rail inputs
- One 8-bit 5V digital-to-analog converter (DAC)
- Up to two serial peripheral interface (SPI) modules
- Up to two serial communication interface (SCI) modules
- SENT Transmitter Interface
- MSCAN (1 Mbit/s, CAN 2.0 A, B software compatible) module
- One on-chip CAN physical layer module
- 8-channel timer module (TIM0) with input capture/output compare
- 4-channel timer module (TIM1) with input capture/output compare (fast max 64MHz)
- Inter-IC (IIC) module
- 4-channel 16-bit Pulse Width Modulation module (PWM0)
- 4-channel 16-bit Pulse Width Modulation module (PWM1) (fast max 64MHz)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API), supports cyclic wakeup from Stop mode
- Four pins to support 25 mA drive strength to VSSX
- One pin to support 20 mA drive strength from VDDX (EVDD)
- Two High Voltage Input (HVI) pins
- Supply $V_{SUP}$ monitoring with warning
- On-chip temperature sensor, temperature value can be measured with ADC or can generate a high temperature interrupt

## 1.4 Module Features

The following sections provide more details of the integrated modules.

### 1.4.1 S12Z Central Processor Unit (CPU)

The S12Z CPU is a revolutionary high-speed core, with code size and execution efficiencies over the S12X CPU. The S12Z CPU also provides a linear memory map eliminating the inconvenience and performance impact of page swapping.

- Harvard Architecture - parallel data and code access
- 3-stage pipeline
- 32-bit wide instruction and databus
- 32-bit ALU
- 24-bit addressing (16 MB linear address space)
- Instructions and Addressing modes optimized for C-Programming and Compiler
  - MAC unit 32bit += 32bit*32bit
  - Hardware divider
  - Single cycle multi-bit shifts (Barrel shifter)
  - Special instructions for fixed point math
- Unimplemented opcode traps
- Unprogrammed byte value (0xFF) defaults to SWI instruction

#### 1.4.1.1 Background Debug Controller (BDC)

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

#### 1.4.1.2 Debugger (DBG)

- Three comparators (A, B and D)
  - Comparator A compare the full address bus and full 32-bit data bus
  - Comparators B and D compare the full address bus onlyEach comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax

- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIGState transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)

## 1.4.2 Embedded Memory

### 1.4.2.1 Memory Access Integrity

- Illegal address detection
- ECC support on embedded NVM and system RAM

### 1.4.2.2 Flash

On-chip flash memory on the MC9S12ZVC-Family on the features the following:

- Up to 192Kbytes of program flash memory
  - Automated program and erase algorithm
  - Protection scheme to prevent accidental program or erase

### 1.4.2.3 EEPROM

- 2 Kbytes EEPROM
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 4 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

### 1.4.2.4 SRAM

- 12 Kbytes of general-purpose RAM with ECC
  - Single bit error correction and double bit error detection code based on 16-bit data words

## 1.4.3 Clocks, Reset and Power Management Unit (CPMU)

- Real time interrupt (RTI)
- Clock monitor, supervising the correct function of the oscillator (CM)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory