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MC9S12ZVHY/MC9S12ZVHL Families Reference Manual

S12 MagniV Microcontrollers

MC9S12ZVHYRMV1
Rev. 1.05
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A full list of family members and options is included in the appendices.This document contains information for all constituent modules, with the exception of the S12Z CPU. For S12ZCPU information please refer to the CPU S12Z Reference Manual.

The following revision history table summarizes changes contained in this document. .

Revision History

Date	Revision	Description
Sep, 2013	1.00	First release for external web site - Add ZVHY 32K - Update OSC etc. electrical spec
Nov, 2013	1.01	- Updated Appendix A electrical spec - Updated SCI/ADC/SPI/BDC/FTMRZ sections (see section rev. history)
Mar, 2014	1.02	- Added ZVHL part and corresponding LINPHY information. - Updated STOP mode BDC dependency text. - Changed V_{LVRXA} minimum from 2.97V to 2.95V - Added frequency spec. for WSTAT to operating conditions table - Removed incorrect device overview reference to over-temperature protection - Corrected vector mapping of ADC CONIF_OIE interrupt - Updated CPMU section (see section rev. history)
Jun, 2014	1.03	- Corrected ordering information controller family encoding in Appendix N
Sep, 2014	1.04	- Updated BKGD pin I/O specification - Specified ADC accuracy for a range of VDDA and VREF
Jun, 2015	1.05	- Added reference to safety constrained applications - Corrected ADC reference result to right justified - Split VDDX electrical parameter into separate cases, with and without PNP - Enhanced CPMU chapter (see CPMU revision history) - Added startup from reset cycle count parameter - Updated BATS electrical parameter values for LB1, HB1 and HB2. - Corrected BKGD pin voltage condition in Table A-8 - Removed incorrect CPU feature from feature list - Corrected BDC clock name (see BDC revision history)

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Chapter 1
Device Overview MC9S12ZVHY/MC9S12ZVHL Families

Table 1-1. Revision History

Version Number	Revision Date	Description of Changes
0.05	Sep 2012	• Update ADC conversion reference IFR location • Correct 100LQFP pinout signals typos • Fix base on review feedback • Add FTMRZ related connection
0.06	Nov 2012	• Update for 1N39G
0.07	July 2013	• Add 32K device
0.08	Jan 2014	• Add ZVHL part
0.09	Jun 2015	• Added reference to safety constrained applications • Corrected ADC reference result to right justified

1.1 Introduction

The MC9S12ZVHY/MC9S12ZVHL Families are optimized automotive 16-bit microcontroller product families, focused on low-cost, high-performance and application component count reduction. They integrate many components of the MagniV mixed signal microcontroller S12ZVH-family, including a 5V regulator system to supply the microcontroller and other components. The MC9S12ZVHY is targeted at automotive and motorcycle instrument cluster applications requiring stepper motor gauges and segment LCD displays. Please contact Freescale local representatives for advice on extremely safety constrained applications. The MC9S12ZVHL is targeted at automotive and motorcycle instrument cluster applications requiring stepper motor gauges, segment LCD displays and LIN communications.

The devices features a 4x40 liquid crystal display (LCD) controller/driver and a pulse width modulated motor controller (MC) consisting of up to 16 high current outputs. The devices are capable of stepper motor stall detection (SSD) via hardware or software, please contact Freescale sales office for detailed information on software SSD.

The MC9S12ZVHY/MC9S12ZVHL Families deliver an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant PCB space savings. These families deliver all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of Freescale's existing S12(X) MCU families. The MC9S12ZVHY/MC9S12ZVHL Families also feature the revolutionary S12Z CPU with code size and execution efficiencies even higher than our class leading S12X CPU. They also provides a linear memory map for all members of the family, eliminating the inconvenience and performance impact of page swapping. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

1.2 Features

This section describes the key features of the MC9S12ZVHY/MC9S12ZVHL Families.

1.2.1 MC9S12ZVHY/MC9S12ZVHL Families Member Comparison

Table 1-2 provides a summary of feature set differences within the MC9S12ZVHY/MC9S12ZVHL Families. LINPHY function is only available on MC9S12ZVHL family.

Table 1-2. Derivative Comparison

Feature	MC9S12ZVHY64/ZVHL64		MC9S12ZVHY32/ZVHL32	
Package	100 pins (LQFP)	144 pins (LQFP)	100 pins (LQFP)	144 pins (LQFP)
CPU	HCS12Z		HCS12Z	
Flash memory (ECC)	64 KB		32 KB	
EEPROM (ECC)	2 KB		2KB	
RAM (ECC)	4 KB		2 KB	
Stepper Motor Drive (with HW SSD)	2		2	
Segment LCD	4 x 32	4 x 40	4 x 32	4 x 40
Simple Sound Generator (SSG)	Yes		Yes	
SCI	2		2	
LIN Physical Layer	Only avaiable on ZVHL		Only available on ZVHL	
SPI	1		1	
IIC	1		1	
CAN (digital communication module)	1		1	
Timer	Two 8ch x 16-bit (not all IOC avaiable on pins)	Two 8ch x 16-bit	Two 8ch x 16-bit (not all IOC avaiable on pins)	Two 8ch x 16-bit
PWM	8 ch (8-bit) / 4ch (16-bit)		8 ch (8-bit) / 4ch (16-bit)	
RTC	Yes		Yes	
ADC Resolution	10-bit resolution		10-bit resolution	
ADC Inputs	4 pins + internal signals	8 pins + internal signals	4 pins + internal signals	8 pins + internal signals
Frequency modulated PLL	Yes		Yes	

Feature	MC9S12ZVHY64/ZVHL64		MC9S12ZVHY32/ZVHL32	
Internal 1 MHz RC oscillator	Yes		Yes	
Autonomous window watchdog	1 (with independent clock source)		1 (with independent clock source)	
Key Wakeup I/Os	19	24	19	24
General purpose I/Os (5 V)(1)	up to 73 for ZVHY up to 78 for ZVHL	up to 100	up to 73 for ZVHY up to 78 for ZVHL	up to 100
Direct Battery Voltage sense pin	Yes		Yes	
Vsup sense	Yes		Yes	
Chip temperature sensor	1 General sensor		1 General sensor	
VSUP Supply voltage	5.5 V – 18 V (normal operation) up to 40V (protected operation)		5.5 V – 18 V (normal operation) up to 40V (protected operation)	
VDDX Output current	Determined by power dissipation of external ballast		Determined by power dissipation of external ballast	
Maximum Bus Frequency	32 MHz		32 MHz	

1. Maximum I/O count based on multiplexing with peripherals.

1.3 Maskset 0N39G and 1N39G device compare

0N39G and 1N39G device module versions differ as shown in Table 1-3.

NOTE User should take care when switching from 0N39G to 1N39G device

Table 1-3. Device Difference for 0N39G and 1N39G

	0N39G	1N39G
SCI	V5	V6
BDC	V1	V2
MCU	no ADC reference voltage to IFR	ADC reference voltage to IFR

1.4 Chip-Level Features

On-chip modules available within the family include the following features:

- S12Z CPU core
- Up to 64 KB on-chip flash with ECC
- 2 KB EEPROM with ECC
- Up to 4 KB on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter