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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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MC9S12ZVMB-Family
Reference Manual

S12 MagniV
Microcontrollers

Rev. 1.3
07 MAR 2017
MC9S12ZVMBRM

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The MC9S12ZVMB-Family is targeted for safety relevant systems and has been developed using an ISO26262 compliant development system under the NXP Safe Assure program. For details of device usage in safety relevant systems refer to the MC9S12ZVMB Safety Manual.

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This document contains information for all modules except the CPU. For CPU information please refer to the CPU S12Z Reference Manual. The following revision history table summarizes changes to this document. The individual module sections contain revision history tables with more detailed information..

Table 0-1. Revision History

Date	Revision	Description
26 Nov 2015	1.1	Updated family member comparison table Corrected Figure 1-10 Updated ordering information in Appendix K
24 Mar 2016	1.2	Added Grade0 row to device summary Table 1-2 Corrected number of external ADC channels Section 1.4.11 Specified unused VSUPHS must be connected to VSUP or VDDX Section 1.7.3.6 Adjusted VREG temperature sensor electrical parameter valuesTable B-1 Changed ADC maximum frequency from 8.34MHz to 8MHz Table C-1 Adjusted HVI input resistance in PIM chapter Figure 2-42 Corrected pin name from VRH0 to VRH_0 Figure 1-4 Minor formating and error corrections (see PIM, GDU, SRAM_ECC revision histories) Corrected write access limitations for GDU registers Added bootstrap switch diode to GDU Figure 18-17 Added GDU current sense unity bandwidth and input resistance to Table E-1 Changed RESET pin input pulse passed parameter minimum value Table A-11 Added bootstrap diode resistance parameter Table E-1
16 Sep 2016	1.3 DRAFT A	Added to applications list in device overview Added temperature sensor application information Section 1.13.1 Renamed CPMU alternate temperature sensor to DVBE temperature sensor Enhanced power dissipation info Table A-7, Figure A-2 Updated PT2 leakage values Table A-10 Updated current consumption values Table A-16, Table A-17 Updated DVBE temperature sensor values Table B-1 Updated VBG temperature dependence value, Table B-1 Added desaturation thresholds to GDU electrical specification Table E-1 Updated VLS current limit threshold Table E-1 Added parameter GHD division ratio through phase mux.Table E-1
07 Mar 2017	1.3	Clarified VDDX range for test and characterization Table A-10, Table C-1 Updated ISUPS values at 105°C Table A-17 Updated V_{DVBE} parameter value Table B-1 Updated temperature sensor application information Section 1.13.1 Updated GDU t_{delon}, t_{deloff} parameter values Table E-1 Added R_{bsdon} and I_{VBS} parameter values Table E-1 Updated gate drive footnote Table E-1 Updated current injection considerations C.1.1.4/C-692, Table A-12

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Chapter 1
Device Overview MC9S12ZVMB-Family

Table 1-1. Revision History

Version Number	Revision Date	Sections Affected	Description of Changes
0.4	11.Jun.2015	General	Initial version for S12ZVMB64 product
0.5	16.Jul.2015	General	Removed async_event connections Added GDU to TIM1 IC2 connection Changed pin order to improve VLS bond out
0.6	17.Jul.2016	Section 1.1	Added applications

1.1 Introduction

The S12 MagniV product line is a highly optimized, automotive family of devices which integrate, beside the typical digital peripherals, additional analog battery level (12 V) components.

The MC9S12ZVMB-Family is a new member of the S12 MagniV product line based on the enhanced performance, linear address space S12Z core and delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings.

The particular differentiating features of this family are the enhanced S12Z core, the combination of an ADC synchronized to PWM signals using a Programmable Trigger Unit (PTU) and the integration of “high-voltage” analog modules, including the voltage regulator (VREG), Gate Drive Unit (GDU) and a Local Interconnect Network (LIN) physical layer. These features enable a fully integrated single chip solution to drive external power MOSFETs for motor drive applications.

The MC9S12ZVMB-Family includes error correction code (ECC) on RAM and flash memory, EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (PLL) that improves the EMC performance. The MC9S12ZVMB-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of existing S12 families. In addition to the peripheral module I/O ports, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12ZVMB-Family is a general-purpose family of devices suitable for a range of applications, including:

- Brush DC motors that need driving in 2 directions, along with PWM control for
  - Window lift
  - Trunk opener
  - Sun roof

— Sliding doors
— Seat positioning

1.2 Features

This section describes the key features of the MC9S12ZVMB-Family.

1.2.1 MC9S12ZVMB-Family member comparison

Table 1-2 provides a summary of feature set differences within the MC9S12ZVMB-Family. All other features are common to all family members.

Table 1-2. MC9S12ZVMB-Family devices

Feature	S12ZVMBA				S12ZVMB			
Flash memory	64 KB	48 KB	64 KB	48 KB	64 KB	48 KB	64 KB	48 KB
Package option	LQFP48		LQFP64		LQFP48		LQFP64	
Grade 0 qualification (Ta up to 150°C)	Yes		No		Yes		No	
EEPROM	512 Byte							
RAM	4 KB							
Physical Layer	LIN							
High Voltage Inputs	3							
High Side Drivers	2							
FET pre-driver (GDU)	2 HS + 2 LS Max. PWM frequency 20 kHz				2 HS + 2 LS Max. PWM frequency 1 kHz			
Integrated Current Sense Op-Amp	1							
VREG ballast transistor support	yes							
SCI	2(1)							
SPI	1							
16-Bit Timer channels	4+4							
15-bit PMF channels(2)	6							
ADC channels mapped to pins	5		9		5		9	
EVDD (20 mA source)	1							
NGPIO (25 mA sink)	1							
General purpose I/O	15		24		15		24	

1. One SCI internally mapped to LIN physical layer

2. Four PWM channels internally mapped to GDU, 2 PWM channels for GPIO/HS

1.2.2 ADC module versions

This device family features ADC V3. The ADC module description includes a superset of features for V1, V2 and V3. It also summarizes these minor version differences.

1.2.3 S12ZVMBA versions

The FET-Predriver on the S12ZVMB version cannot be driven directly from the PMF PWM channels at a frequency of greater than 1KHz. Otherwise the S12ZVMB device is identical to the S12ZVMBA device.

1.3 Chip-Level features

On-chip modules available within the family include the following features:

- S12Z CPU core
- 64 KB or 48 KB on-chip flash with ECC
- 512 Byte EEPROM with ECC
- 4 KB on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 1 MHz internal RC oscillator with +/-1.3% accuracy over junction temperature range up to 150°C
- 4-20 MHz amplitude controlled pierce oscillator
- Internal COP (watchdog) module
- 6-channel, 15-bit pulse width modulator with fault protection (PMF)
- Low-side and High-side FET pre-drivers for each phase
  - Gate drive pre-regulator (11 V LDO)
  - High-side gate supply generated using bootstrap circuit with internal diode and external capacitor
  - Sustaining charge pump with two external capacitors and diodes
  - High-side drain (GHD) monitoring on internal ADC channel using GHD/5 voltage
- Analog-to-digital converter (ADC) with 10-bit resolution and up to 9 channels available on external pins
- One serial peripheral interface (SPI) module
- One serial communication interface (SCI) module with interface to internal LIN physical layer transceiver (with RX connected to a timer channel for frequency calibration purposes, if desired)
- One additional SCI (not connected to LIN physical layer)
- On-chip LIN physical layer transceiver fully compliant with the LIN 2.2 and SAE J2602-2 standards
- Two 4-channel timer modules (TIM) with input capture/output compare
- One programmable trigger unit (PTU) for ADC trigger synchronization
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- One current sense circuit for over-current detection or torque measurement

- Autonomous periodic interrupt (API)
- Two High-side Driver outputs
- Three High Voltage Input (HVI) pins
- One 20mA high-current output for use as Hall sensor supply
- Supply voltage sensor with low battery warning
- One high current (25 mA sink) NGPIO
- Chip temperature sensor

1.4 Module features

The following sections provide more details of the integrated modules.

1.4.1 S12Z central processor unit (CPU)

The S12Z CPU is a revolutionary high-speed core, with code size and execution efficiencies over the S12X CPU. The S12Z CPU also provides a linear memory map eliminating the inconvenience and performance impact of page swapping.

- Harvard Architecture - parallel data and code access
- 3 stage pipeline
- 32-Bit wide instruction and databus
- 32-Bit arithmetic logic unit (ALU)
- 24-bit addressing, of 16 MByte linear address space
- Instruction and addressing modes optimized for C-programming & compilation
  - Multiply and accumulate (MAC) unit 32bit += 32bit*32bit
  - Hardware divider
  - Single cycle multi-bit shifts (Barrel shifter)
  - Special instructions for fixed point math
- Unimplemented opcode traps
- Unprogrammed byte value (0xFF) defaults to SWI instruction

1.4.1.1 Background debug controller (BDC)

- Background debug controller (BDC) with single-wire interface
  - Non-intrusive memory access commands
  - Supports in-circuit programming of on-chip nonvolatile memory

1.4.1.2 Debugger (DBG)

- Three comparators (A, B and D)
  - Comparator A compares the full address bus and full 32-bit data bus
  - Comparators B and D compare the full address bus only

  - Each comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range match
  - Outside address range match
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)

1.4.2 Embedded memory

1.4.2.1 Memory access integrity

- Illegal address detection
- ECC support on embedded NVM and SRAM

1.4.2.2 Flash

On-chip flash memory features the following:

- Up to 64KB of program flash memory
  - 32 data bits plus 7 syndrome ECC (error correction code) bits allow single bit fault correction and double bit fault detection
  - Erase sector size of 512 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads
  - Protection scheme to prevent accidental program or erase

1.4.2.3 EEPROM

- Up to 512 Bytes EEPROM
  - 16 data bits plus 6 syndrome ECC bits
  - Single bit error correction, double bit error detection
  - Erase sector size 4 bytes, program with word resolution
  - Automated program and erase algorithm
  - User margin level setting for reads

1.4.2.4 SRAM

- Up to 4 Kbytes of general-purpose RAM with ECC
  - Single bit error correction and double bit error detection

1.4.3 Clocks, reset & power management unit (CPMU)

- Real time interrupt (RTI)
- Clock monitor, supervising the correct function of the oscillator (CM)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory
- System reset generation
- Autonomous periodic interrupt (API) (combination with cyclic, watchdog)
  - Trimmable RC oscillator timebase that can remain active in STOP mode
- Low Power Operation
  - RUN mode - main full performance operating mode with the entire device clocked
  - WAIT mode - the internal CPU clock is switched off, so the CPU does not execute instructions
  - Pseudo STOP - system clocks are stopped but the oscillator, RTI, COP, and API modules can be enabled
  - STOP - the oscillator is stopped in this mode, all clocks are switched off and all counters and dividers remain frozen, with the exception of the COP and API which can optionally run from ACLK

1.4.3.1 Internal phase-locked loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - Internal 1 MHz RC oscillator (IRC)
    - External 4-20 MHz crystal oscillator/resonator

1.4.3.2 Internal RC oscillator (IRC)

- Trimmable internal 1 MHz reference clock.
  - Trimmed accuracy for temperature options V, M: ±1.3%max.
  - Trimmed accuracy for temperature option W: ±1.45%max

1.4.4 External oscillator (XOSCLCP)

- Amplitude controlled Pierce oscillator using 4 MHz to 20 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Trans conductance sized for optimum start-up margin for typical crystals
  - Oscillator pins shared with GPIO functionality

1.4.5 4 channel timer (TIM)

- 4 x 16-bit channels Timer module for input capture or output compare
- 16-bit free-running counter with 8-bit precision prescaler

1.4.6 Pulse width modulator with fault protection (PMF)

- 6 x 15-bit channel PWM resolution
- Each pair of channels can be combined to generate a PWM signal (with independent control of edges of PWM signal)
- Dead time insertion available for each complementary pair
- Center-aligned or edge-aligned outputs
- Programmable clock select logic with a wide range of frequencies
- Programmable fault detection

1.4.7 Programmable trigger unit (PTU)

- Synchronizes ADC triggers based on PMF signal edges
- One 16 bit counter as time base for all trigger events
- One trigger generator(TG0) Up to 32 trigger events per trigger generator
- Global Load OK support, to guarantee coherent update of all control loop modules
- Trigger values stored in system memory
- Software generated reload event and trigger event generation for debugging

1.4.8 LIN physical layer transceiver

- Compliant with LIN physical layer 2.2 specification
- Compliant with the SAE J2602-2 LIN standard
- Standby mode with glitch-filtered wake-up
- Slew rate selection optimized for the baud rates:

  - 10.4 kBit/s
  - 20 kBit/s
  - Fast Mode (up to 250 kBit/s)
- Selectable pull-up of 34 k or 330 k (in Shutdown Mode, 330 k only)
- Current limitation for LIN Bus pin falling edge.
- Over-current protection.
- LIN TxD-dominant timeout feature monitoring the LPTxD signal.
- Automatic transmitter shutdown in case of an over-current or TxD-dominant timeout.
- Fulfills the OEM “Hardware Requirements for LIN (CAN and FlexRay) Interfaces in Automotive Applications” v1.3.

1.4.9 Serial communication interface module (SCI)

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 16-bit baud rate selection
- Programmable character length
- Programmable polarity for transmitter and receiver
- Active edge receive wakeup
- Break detect and transmit collision detect supporting LIN

1.4.10 Serial peripheral interface module (SPI)

- Configurable 8- or 16-bit data size
- Full-duplex or single-wire bidirectional
- Double-buffered transmit and receive
- Master or slave mode
- MSB-first or LSB-first shifting
- Serial clock phase and polarity options

1.4.11 Analog-to-digital converter module (ADC)

- Selectable 10-bit or 8-bit resolution
- Up to 12 external channels & 8 internal channels
- 2.2us for single 10-bit resolution conversion
- Left or right aligned result data
- Continuous conversion mode
- Programmers model with list based command and result storage architecture

- ADC directly writes results to RAM, preventing stall of further conversions
- Internal signals monitored by the ADC module
  - VRH, VRL, (VRL+VRH)/2
  - Vsup monitor
  - VREG Vbg, and Temperature Sensor
  - Delta VBE Temperature Sensor
  - GDU phase, GDU DC-link
  - High Voltage Inputs (PL[2:0])
- External pins can also be used as digital I/O with keyboard wake-up interrupt capability

1.4.12 Supply voltage sensor (BATS)

- Monitoring of supply (VSUP) voltage
- Internal ADC interface from an internal resistive divider
- Optional generation of low or high voltage interrupts

1.4.13 On-chip voltage regulator system (VREG)

- Voltage regulator
  - Linear voltage regulator directly supplied by VSUP
  - Low-voltage detect on VSUP
  - Power-on reset (POR)
  - Low-voltage reset (LVR) for VDDX domain
  - Over-temperature interrupt
- Internal voltage regulator
  - Linear voltage regulator with bandgap reference
  - Low-voltage detect on VDDA
  - Power-on reset (POR) circuit
  - Low-voltage reset for VDD domain

1.4.14 Gate drive unit (GDU)

- Low-side and High-side FET pre-drivers for 2 phases of 2 half bridges
- Gate drive pre-regulator LDO (Low Dropout Voltage Regulator)
- High-side gate supply done via bootstrap circuit with internal diode and external capacitor
- Sustaining charge pump with two external capacitors and diodes
- FET-Predriver short circuit (desaturation) detection
- Over and under voltage detection and shutdown
- Over current monitor with optional shutdown
- Monitoring of FET High-side drain (GHD) voltage