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MC9S12ZVM-Family
Reference Manual and Datasheet

S12 MagniV
Microcontrollers

Rev. 2.11
28 OCT 2016
MC9S12ZVMRM

nxp.com

The ZVMC256, ZVML31, ZVM32 and ZVM16 devices are targeted for safety relevant systems and have been developed using an ISO26262 compliant development system under the NXP SafeAssure program. For details of device usage in safety relevant systems refer to the MC9S12ZVMB Safety Manual.

The document revision on the Internet is the most current. To verify this is the latest revision, refer to:

nxp.com.

This document contains information for all modules except the CPU. For CPU information please refer to the CPU S12Z Reference Manual. This revision history table summarizes changes to this document. The individual module sections contain revision history tables with more detailed information.

NOTE
This reference manual documents the S12ZVM-Family.
It contains a superset of features within the family.
Some module versions differ from one part to another within the family.
Section 1.2.1 MC9S12ZVM-Family Member Comparison provides support to access the correct information for a particular part within the family.

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Table 0-1. Revision History

Date	Revision	Description
22 MAY2014	1.4	Updated family derivative table for S12ZVML32, S12ZVM32 and S12ZVM16 devices Added 64KB, 32KB and 16KB derivative information to flash module chapter Added pin routing options for S12ZVM32 and S12ZVM16 devices Added HV Phy information for the S12ZVM32 and S12ZVM16 derivatives Updated Part ID assignment table and ordering information for S12ZVM32 and S12ZVM16 Corrected PLL VCO maximum frequency specification Changed V_{LVLSA} maximum from 7V to 6.9V Added electrical parameter for HD division ratio through the phase multiplexer Corrected preferred VRL reference from VRL_1 to VRL_0 Included NVM timing parameters for the S12ZVM32 and S12ZVM16 devices Added GDU S12ZVM32 and S12ZVM16 specific differences and electrical specifications Added references to f_{WSTAT} Added VDDX short circuit fall back current and temperature/input dependency specs.
22 SEP 2014	1.5	Removed incorrect references to PACLK in TIM chapter Improved clarity of routing options in PIM chapter. Updated S12ZVM- Family derivative table. Added 48LQFP thermal package parameters Extended LINPHY specification range minimum to 5V Updated BKGD pin I/O specification Specified ADC accuracy for a range of VDDA and VREF.
20 MAR 2015	2.0	Added ZVMC256 information Added mask set 2N95G information Added more detailed PTU minimum trigger spacing description Updated CPMU, PIM and GDU chapters for ZVMC256 Improved CPMU specification clarity (see CPMU revision history) Removed electrical parameter classification Added reset startup timing parameter Updated BATS parameters Extended BKGD V_{IL} condition from 3.15V to 3.13V Extended GDU operating range from 26V to 26.6V Temperature sensor output at 150C changed from 2.25V to 2.33V. Added GDU VBS current parameter Updated package thermal information for ZVM32 and ZVM16 parts Added VBG temperature and voltage dependency parameters Added device stop current at 105C.
22 APR 2015	2.1	Updated Stop and Wait current parameter values (I_{SUPS}, I_{SUPW}) Corrected 80LQFP-EP pin name from VSS2 to VSS1 Updated ZVMC256 VDDS regulator parameters. Changed PL0 ESD specification Minor corrections to PIM, PMF, SRAM and ADC chapters (see module revision histories)
27 APR 2015	2.2	Updated Stop current parameter values (I_{SUPS}) Updated LINPHY parameter range limit to 5.5V Added more information about VDDS1, VDDS2, SNPS1, SNPS2 to CPMU chapter. Reintroduced EPRES bit for GDU V4 Added 80LQFP-EP mechanical package information

Table 0-1. Revision History

Date	Revision	Description
20 NOV 2015	2.3	Added devices to Part ID list Table 1-6 Added explanation of GSUF dependency on xN14N mask set Table 1-19 Minor corrections to reset source and interrupt vector tables Table 1-15 Added device level POR information Figure 1-8 Minor correction to PIM chapter Added constraints to EXTCON, SCS2 and SCS1 bits in CPMU chapter Added PMF version difference table Table 15-3 Corrected footnotes and parameter spelling in GDU register summary Noted GDU sense amplifier dependence on GFDE bit Documented that flash option (FOPT) register can be written in special mode Added pulsed absolute maximum rating for HSx pins Table A-2 Extended VDDS1 and VDDS2 maximum ratings Table A-2 Added thermal resistance parameter values for 80LQFP-EP package Added VREG configuration to Run/Wait/Stop current measurement configurationTable A-16 Removed de-saturation thresholds from electrical spec. tables Added footnote for GDU tdelon/tdeloff electrical parameters Added max. and min. values for GDU HD signal division through phase mux. Removed incorrect limit from BATS electrical parameter table headers Extended CANPHY maximum ratings to 175°C Updated SRAM_ECC chapter to cover ZVMC256 Minor correction to PMF chapter Updated typical Stop IDD and Pseudo Stop IDD values for ZVMC256 based on validation data Added ZVMC256 parameter for Stop IDD with CANPHY and API enabled Table A-19 Renamed bit GSLEWMOD to TDEL (GDU V6). Removed GSLEWMOD bit (GDU V5) Noted temperature sensor slope is subject to further characterization
14 DEC 2015	2.4	Added T1IC0RR to PIM MODRR2 register Updated temperature sensor electrical specification, Table B-1 Added GDU current sense amp unity bandwidth parameter Table E-1, Table E-2 Added GDU current sense input resistance footnote Table E-1, Table E-2
14 JAN 2016	2.5	Clarified non production mask sets Table 1-4, Table 1-6 Updated ordering information in Appendix L Changed RESET pin input pulse passed parameter minimum specification value.Table A-13 Replaced Freescale with NXP in logo and page footers Added maximum value for GDU parameter VBSx current whilst high side inactive Table E-2
07 MAR 2016	2.6	Added 3N95G mask set information Table 1-19, Table 1-4, Table 1-6 Added list of ISO26262 compliant devices Moved GDU mask set dependent features to device overview section Table 1-19 Added new 64LQFP-EP package diagrams Table K.2 Added minimum value for GDU parameter VBSx current whilst high side inactive Table E-2 Updated V_{CSAoff} parameter limits for GDU V5 and GDU V6 Table E-1, Table E-2 Added ADCCMD1[7:6] device dependencies in register listing Section M.13, Section M.14 Simplified GDU device dependencies in register listing Section M.15 Corrected High Temperature Interrupt spec. (cannot wake up from STOP) Table 1-16 Added footnote to Table A-14 ZVMC256: added typical Run/Wait IDD values, updated 85°C Stop IDD Table A-18, Table A-19 Added bootstrap diode resistance parameter Table E-2 Updated GDU boost coil current limit specification Table E-2, Table E-1 Reverted to original current sense amp. offset values Table E-2, Table E-1 Added package to mask set mapping table Table K-1
08 MAR 2016	2.7	Changed maximum value of V_{BSTOFF} Table E-2, Table E-1 Updated 48LQFP-EP Mechanical Information Diagram Section K.1

Table 0-1. Revision History

Date	Revision	Description
19 APR 2016	2.8	Added PAD pin leakage specification at 125°C Table A-12 Updated t_{HGON}, t_{HGOFF} parameter values Table E-1 Specified VRH drop when using VDDS1 or VDDS2 as VRH on ZVMC256 Section C.1.1.5 Added min. and max. desaturation comparator filter times to electrical spec. Table E-1 Updated 64LQFP-EP thermal parameters Table A-9, Table A-10
06 JUN 2016	2.9	Fixed corrupted symbol fonts Table A-3, Table A-5 Corrected wrong IFR reference Section 20.3.2.10 Clarified PAD8 leakage better Table A-12 Added I_{SUPR} and I_{SUPW} maximum values at T_J = 175°C for ZVMC256 Table A-18 Added Pseudo STOP maximum current for ZVMC256 Table A-20 Removed bandgap temperature dependency footnote, Table B-1 Changed ZVMC256 SNPS monitor threshold min/max values Table B-2 Changed VLS current limit threshold to 112mA Table E-1, Table E-2 Removed desaturation comparator filter times from GDU chapter. Added desaturation comparator levels to Table E-1, Table E-2 Added low side desaturation comparator functional range as footnote Table E-1, Table E-2
29 JUN 2016	2.10	Updated GDU VBS filter Figure 18-20 Removed incorrect reference to temperature sensor influencing GDU outputs Section 1.13.3.4 Changed Stop IDD (ISUPS) specifications for ZVMC256 Table A-19
28 OCT 2016	2.11	Added IOC0 signal mapping to 48LQFP package Figure 1-6 Fixed corrupted symbol fonts in PIM chapter Added diode to VDDC pin Figure 1-18 Updated Stop mode current ISUPS maximum values Table A-19 Updated tdelon, tdeloff values Table E-1

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Chapter 3
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Chapter 4
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Chapter 5
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Chapter 6
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Appendix A
MCU Electrical Specifications

Appendix B
CPMU Electrical Specifications (VREG, OSC, IRC, PLL)

Appendix C
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Chapter 1
Device Overview MC9S12ZVM-Family

Table 1-1. Revision History

Version Number	Revision Date	Sections Affected	Description of Changes
1.8	04.Sep.2014	Section 1.2.1	• Added S12ZVML31 information to derivative table
2.0	10.Oct.2014	General	• Added ZVMC256 information
2.01	06.Feb.2015	General	• Added 2N95G maskset information. • Added TIM1 for ZVMC256
2.02	25.Aug.2016	Figure 1-6, Table 1-8 Section 1.13.3.6	• Clarified IOC0 device pin mapping dependencies • Clarified IOC0 device pin mapping dependencies • Removed Temperature Sensor from list of Dynamic motor control fault inputs

1.1 Introduction

The MC9S12ZVM-Family is an automotive 16-bit microcontroller family using the NVM + UHV technology that offers the capability to integrate 40 V analog components. This family reuses many features from the existing S12/S12X portfolio. The particular differentiating features of this family are the enhanced S12Z core, the combination of dual-ADC synchronized with PWM generation and the integration of “high-voltage” analog modules, including the voltage regulator (VREG), Gate Drive Unit (GDU), and either Local Interconnect Network (LIN) physical layer or CAN Physical layer. These features enable a fully integrated single chip solution to drive up to 6 external power MOSFETs for BLDC or PMSM motor drive applications.

The MC9S12ZVM-Family includes error correction code (ECC) on RAM and flash memory, EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12ZVM-Family allows the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12ZVM-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of existing S12(X) families. The MC9S12ZVM-Family is available in different pin-out options, using 80-pin, 64-pin and 48-pin LQFP-EP packages to accommodate LIN, CAN and external PWM based application interfaces. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12ZVM-Family is a general-purpose family of devices suitable for a range of applications, including:

- 3-phase sensorless BLDC motor control for
  - — Fuel pump