



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**MC9S08DN60**  
**MC9S08DN48**  
**MC9S08DN32**  
**MC9S08DN16**

Data Sheet

***HCS08***  
***Microcontrollers***

MC9S08DN60  
Rev 3  
6/2008

[freescale.com](http://freescale.com)



# MC9S08DN60 Series Features

## 8-Bit HCS08 Central Processor Unit (CPU)

---

- 40-MHz HCS08 CPU (20-MHz bus)
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

## On-Chip Memory

---

- Flash read/program/erase over full operating voltage and temperature
  - MC9S08DN60 = 60K
  - MC9S08DN48 = 48K
  - MC9S08DN32 = 32K
  - MC9S08DN16 = 16K
- Up to 2K EEPROM in-circuit programmable memory; 8-byte single-page or 4-byte dual-page erase sector; Program and Erase while executing Flash; Erase abort
- Up to 2K random-access memory (RAM)

## Power-Saving Modes

---

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time interrupt for use in run, wait, and stop

## Clock Source Options

---

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Multi-purpose Clock Generator (MCG) — PLL and FLL modes (FLL capable of 1.5% deviation using internal temperature compensation); Internal reference clock with trim adjustment (trimmed at factory, with trim value stored in flash); External reference with oscillator/resonator options

## System Protection

---

- Watchdog computer operating properly (COP) reset with option to run from backup dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- Flash block protect
- Loss-of-lock protection

## Development Support

---

- Single-wire background debug interface
- On-chip, in-circuit emulation (ICE) with real-time bus capture

## Peripherals

---

- **ADC** — 16-channel, 12-bit resolution, 2.5  $\mu$ s conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage
- **SCI** — One SCI supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; General Call Address; Interrupt driven byte-by-byte data transfer
- **TPMx** — One 6-channel (TPM1) and one 2-channel (TPM2); Selectable input capture, output compare, or buffered edge-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; Real-time clock capabilities using external crystal and RTC for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components

## Input/Output

---

- 53 general-purpose input/output (I/O) pins and 1 input-only pin
- 24 interrupt pins with selectable polarity on each pin
- Hysteresis and configurable pull device on all input pins.
- Configurable slew rate and drive strength on all output pins.

## Package Options

---

- 64-pin low-profile quad flat-pack (LQFP) — 10x10 mm
- 48-pin low-profile quad flat-pack (LQFP) — 7x7 mm
- 32-pin low-profile quad flat-pack (LQFP) — 7x7 mm



# MC9S08DN60 Data Sheet

Covers MC9S08DN60  
MC9S08DN48  
MC9S08DN32  
MC9S08DN16

MC9S08DN60  
Rev 3  
6/2008

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.

© Freescale Semiconductor, Inc., 2007-2008. All rights reserved.

## Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com/>

The following revision history table summarizes changes contained in this document.

| Revision Number | Revision Date | Description of Changes   |
|-----------------|---------------|--|
| 1               | 6/2006        | Advance Information version for alpha samples customers  |
| 2               | 9/2007        | Product Launch. Removed the 64-pin QFN package. Changed from standard to extended mode for MSCAN registers in register summary. Corrected Block diagrams for SCI. Updated the latest Temp Sensor information. Made FTSTMOD reserved. Updated device to use the ADC 12-bit module. Revised the MCG module. Updated the TPM block module to version 3. Added the TPM block module version 2 as an appendix for devices using 3M05C (or earlier) mask sets. Heavily revised the Electricals appendix. |
| 3               | 6/2008        | Sustaining Update. Incorporated PS Issues # 2765, 3177, 3236, 3292, 3311, 3312, 3326, 3335, 3345, 3382, 2795, 3382 and 3386 PLL Jitter Spec update. Also, added internal reference clock trim adjustment statement to Features page. Updated the TPM module to the latest version. Adjusted values in Table A-13 Control Timing row 2 and in Table A-6 DC Characteristics row 24 so that it references 5.0 V instead of 3.0 V.   |

© Freescale Semiconductor, Inc., 2007-2008. All rights reserved.

This product incorporates SuperFlash<sup>®</sup> Technology licensed from SST.

# List of Chapters

| Chapter    | Title   | Page |
|------------|---|------|
| Chapter 1  | Device Overview .....                               | 19   |
| Chapter 2  | Pins and Connections .....                          | 23   |
| Chapter 3  | Modes of Operation .....                            | 31   |
| Chapter 4  | Memory .....  | 37   |
| Chapter 5  | Resets, Interrupts, and General System Control..... | 63   |
| Chapter 6  | Parallel Input/Output Control.....                  | 79   |
| Chapter 7  | Central Processor Unit (S08CPUV3).....              | 109  |
| Chapter 8  | Multi-Purpose Clock Generator (S08MCGV1) .....      | 129  |
| Chapter 9  | Analog Comparator (S08ACMPV3) .....                 | 161  |
| Chapter 10 | Analog-to-Digital Converter (S08ADC12V1).....       | 167  |
| Chapter 11 | Inter-Integrated Circuit (S08IICV2) .....           | 193  |
| Chapter 12 | Serial Peripheral Interface (S08SPIV3) .....        | 213  |
| Chapter 13 | Serial Communications Interface (S08SCIV4).....     | 229  |
| Chapter 14 | Real-Time Counter (S08RTCV1) .....                  | 249  |
| Chapter 15 | Timer Pulse-Width Modulator (S08TPMV3).....         | 259  |
| Chapter 16 | Development Support .....                           | 287  |
| Appendix A | Electrical Characteristics.....                     | 309  |
| Appendix B | Timer Pulse-Width Modulator (TPMV2) .....           | 331  |
| Appendix C | Ordering Information and Mechanical Drawings.....   | 345  |





# Contents

| Section Number              | Title  | Page |
|-----------------------------|--|------|
| <b>Chapter 1</b>            |  |      |
| <b>Device Overview</b>      |  |      |
| 1.1                         | Devices in the MC9S08DN60 Series .....               | 19   |
| 1.2                         | MCU Block Diagram .....                              | 20   |
| 1.3                         | System Clock Distribution .....                      | 21   |
| <b>Chapter 2</b>            |  |      |
| <b>Pins and Connections</b> |  |      |
| 2.1                         | Device Pin Assignment .....                          | 23   |
| 2.2                         | Recommended System Connections .....                 | 26   |
| 2.2.1                       | Power .....  | 27   |
| 2.2.2                       | Oscillator .....                                     | 27   |
| 2.2.3                       | RESET .....  | 27   |
| 2.2.4                       | Background / Mode Select (BKGD/MS) .....             | 28   |
| 2.2.5                       | ADC Reference Pins ( $V_{REFH}$ , $V_{REFL}$ ) ..... | 28   |
| 2.2.6                       | General-Purpose I/O and Peripheral Ports .....       | 28   |
| <b>Chapter 3</b>            |  |      |
| <b>Modes of Operation</b>   |  |      |
| 3.1                         | Introduction .....                                   | 31   |
| 3.2                         | Features .....                                       | 31   |
| 3.3                         | Run Mode .....                                       | 31   |
| 3.4                         | Active Background Mode.....                          | 31   |
| 3.5                         | Wait Mode .....                                      | 32   |
| 3.6                         | Stop Modes.....                                      | 33   |
| 3.6.1                       | Stop3 Mode .....                                     | 33   |
| 3.6.2                       | Stop2 Mode .....                                     | 34   |
| 3.6.3                       | On-Chip Peripheral Modules in Stop Modes .....       | 35   |
| <b>Chapter 4</b>            |  |      |
| <b>Memory</b>               |  |      |
| 4.1                         | MC9S08DN60 Series Memory Map.....                    | 37   |
| 4.2                         | Reset and Interrupt Vector Assignments .....         | 38   |
| 4.3                         | Register Addresses and Bit Assignments.....          | 40   |
| 4.4                         | RAM.....   | 47   |
| 4.5                         | Flash and EEPROM .....                               | 47   |
| 4.5.1                       | Features .....                                       | 47   |

| Section Number | Title   | Page |
|----------------|---|------|
| 4.5.2          | Program and Erase Times .....                     | 48   |
| 4.5.3          | Program and Erase Command Execution .....         | 48   |
| 4.5.4          | Burst Program Execution .....                     | 50   |
| 4.5.5          | Sector Erase Abort .....                          | 52   |
| 4.5.6          | Access Errors .....                               | 53   |
| 4.5.7          | Block Protection .....                            | 54   |
| 4.5.8          | Vector Redirection .....                          | 54   |
| 4.5.9          | Security .....                                    | 54   |
| 4.5.10         | EEPROM Mapping .....                              | 56   |
| 4.5.11         | Flash and EEPROM Registers and Control Bits ..... | 56   |

## Chapter 5 Resets, Interrupts, and General System Control

|       |   |    |
|-------|---|----|
| 5.1   | Introduction .....  | 63 |
| 5.2   | Features .....  | 63 |
| 5.3   | MCU Reset .....   | 63 |
| 5.4   | Computer Operating Properly (COP) Watchdog .....                      | 64 |
| 5.5   | Interrupts .....  | 65 |
| 5.5.1 | Interrupt Stack Frame .....   | 66 |
| 5.5.2 | External Interrupt Request (IRQ) Pin .....                            | 66 |
| 5.5.3 | Interrupt Vectors, Sources, and Local Masks .....                     | 67 |
| 5.6   | Low-Voltage Detect (LVD) System .....                                 | 68 |
| 5.6.1 | Power-On Reset Operation .....  | 69 |
| 5.6.2 | Low-Voltage Detection (LVD) Reset Operation .....                     | 69 |
| 5.6.3 | Low-Voltage Warning (LVW) Interrupt Operation .....                   | 69 |
| 5.7   | MCLK Output .....   | 69 |
| 5.8   | Reset, Interrupt, and System Control Registers and Control Bits ..... | 70 |
| 5.8.1 | Interrupt Pin Request Status and Control Register (IRQSC) .....       | 71 |
| 5.8.2 | System Reset Status Register (SRS) .....                              | 72 |
| 5.8.3 | System Background Debug Force Reset Register (SBDFR) .....            | 73 |
| 5.8.4 | System Options Register 1 (SOPT1) .....                               | 74 |
| 5.8.5 | System Options Register 2 (SOPT2) .....                               | 75 |
| 5.8.6 | System Device Identification Register (SDIDH, SDIDL) .....            | 76 |
| 5.8.7 | System Power Management Status and Control 1 Register (SPMSC1) .....  | 77 |
| 5.8.8 | System Power Management Status and Control 2 Register (SPMSC2) .....  | 78 |

## Chapter 6 Parallel Input/Output Control

|       |  |    |
|-------|--|----|
| 6.1   | Port Data and Data Direction .....           | 79 |
| 6.2   | Pull-up, Slew Rate, and Drive Strength ..... | 80 |
| 6.3   | Pin Interrupts .....                         | 81 |
| 6.3.1 | Edge Only Sensitivity .....                  | 81 |

| Section Number | Title  | Page |
|----------------|--|------|
| 6.3.2          | Edge and Level Sensitivity .....             | 82   |
| 6.3.3          | Pull-up/Pull-down Resistors .....            | 82   |
| 6.3.4          | Pin Interrupt Initialization .....           | 82   |
| 6.4            | Pin Behavior in Stop Modes.....              | 82   |
| 6.5            | Parallel I/O and Pin Control Registers ..... | 83   |
| 6.5.1          | Port A Registers .....                       | 84   |
| 6.5.2          | Port B Registers .....                       | 88   |
| 6.5.3          | Port C Registers .....                       | 92   |
| 6.5.4          | Port D Registers .....                       | 95   |
| 6.5.5          | Port E Registers .....                       | 99   |
| 6.5.6          | Port F Registers .....                       | 102  |
| 6.5.7          | Port G Registers .....                       | 105  |

## Chapter 7 Central Processor Unit (S08CPUV3)

|       |  |     |
|-------|--|-----|
| 7.1   | Introduction .....                         | 109 |
| 7.1.1 | Features .....                             | 109 |
| 7.2   | Programmer's Model and CPU Registers ..... | 110 |
| 7.2.1 | Accumulator (A) .....                      | 110 |
| 7.2.2 | Index Register (H:X) .....                 | 110 |
| 7.2.3 | Stack Pointer (SP) .....                   | 111 |
| 7.2.4 | Program Counter (PC) .....                 | 111 |
| 7.2.5 | Condition Code Register (CCR) .....        | 111 |
| 7.3   | Addressing Modes.....                      | 113 |
| 7.3.1 | Inherent Addressing Mode (INH) .....       | 113 |
| 7.3.2 | Relative Addressing Mode (REL) .....       | 113 |
| 7.3.3 | Immediate Addressing Mode (IMM) .....      | 113 |
| 7.3.4 | Direct Addressing Mode (DIR) .....         | 113 |
| 7.3.5 | Extended Addressing Mode (EXT) .....       | 114 |
| 7.3.6 | Indexed Addressing Mode .....              | 114 |
| 7.4   | Special Operations.....                    | 115 |
| 7.4.1 | Reset Sequence .....                       | 115 |
| 7.4.2 | Interrupt Sequence .....                   | 115 |
| 7.4.3 | Wait Mode Operation .....                  | 116 |
| 7.4.4 | Stop Mode Operation .....                  | 116 |
| 7.4.5 | BGND Instruction .....                     | 117 |
| 7.5   | HCS08 Instruction Set Summary .....        | 118 |

## Chapter 8 Multi-Purpose Clock Generator (S08MCGV1)

|       |                    |     |
|-------|--------------------|-----|
| 8.1   | Introduction ..... | 129 |
| 8.1.1 | Features .....     | 131 |

| Section Number | Title  | Page |
|----------------|--|------|
| 8.1.2          | Modes of Operation .....                             | 133  |
| 8.2            | External Signal Description .....                    | 133  |
| 8.3            | Register Definition .....                            | 134  |
| 8.3.1          | MCG Control Register 1 (MCGC1) .....                 | 134  |
| 8.3.2          | MCG Control Register 2 (MCGC2) .....                 | 135  |
| 8.3.3          | MCG Trim Register (MCGTRM) .....                     | 136  |
| 8.3.4          | MCG Status and Control Register (MCGSC) .....        | 137  |
| 8.3.5          | MCG Control Register 3 (MCGC3) .....                 | 138  |
| 8.4            | Functional Description .....                         | 140  |
| 8.4.1          | Operational Modes .....                              | 140  |
| 8.4.2          | Mode Switching .....                                 | 144  |
| 8.4.3          | Bus Frequency Divider .....                          | 145  |
| 8.4.4          | Low Power Bit Usage .....                            | 145  |
| 8.4.5          | Internal Reference Clock .....                       | 145  |
| 8.4.6          | External Reference Clock .....                       | 145  |
| 8.4.7          | Fixed Frequency Clock .....                          | 146  |
| 8.5            | Initialization / Application Information .....       | 146  |
| 8.5.1          | MCG Module Initialization Sequence .....             | 146  |
| 8.5.2          | MCG Mode Switching .....                             | 147  |
| 8.5.3          | Calibrating the Internal Reference Clock (IRC) ..... | 158  |

## Chapter 9 Analog Comparator (S08ACMPV3)

|       |   |     |
|-------|---|-----|
| 9.1   | Introduction .....                                | 161 |
| 9.1.1 | ACMP Configuration Information .....              | 161 |
| 9.1.2 | Features .....                                    | 163 |
| 9.1.3 | Modes of Operation .....                          | 163 |
| 9.1.4 | Block Diagram .....                               | 164 |
| 9.2   | External Signal Description .....                 | 164 |
| 9.3   | Memory Map/Register Definition .....              | 165 |
| 9.3.1 | ACMPx Status and Control Register (ACMPxSC) ..... | 165 |
| 9.4   | Functional Description .....                      | 166 |

## Chapter 10 Analog-to-Digital Converter (S08ADC12V1)

|        |  |     |
|--------|--|-----|
| 10.1   | Introduction .....                         | 167 |
| 10.1.1 | Analog Power and Ground Signal Names ..... | 167 |
| 10.1.2 | Channel Assignments .....                  | 167 |
| 10.1.3 | Alternate Clock .....                      | 168 |
| 10.1.4 | Hardware Trigger .....                     | 168 |
| 10.1.5 | Temperature Sensor .....                   | 169 |
| 10.1.6 | Features .....                             | 171 |

| Section Number | Title  | Page |
|----------------|--|------|
| 10.1.7         | ADC Module Block Diagram .....               | 171  |
| 10.2           | External Signal Description .....            | 172  |
| 10.2.1         | Analog Power ( $V_{DDAD}$ ) .....            | 173  |
| 10.2.2         | Analog Ground ( $V_{SSAD}$ ) .....           | 173  |
| 10.2.3         | Voltage Reference High ( $V_{REFH}$ ) .....  | 173  |
| 10.2.4         | Voltage Reference Low ( $V_{REFL}$ ) .....   | 173  |
| 10.2.5         | Analog Channel Inputs (AD $x$ ) .....        | 173  |
| 10.3           | Register Definition .....                    | 173  |
| 10.3.1         | Status and Control Register 1 (ADCSC1) ..... | 173  |
| 10.3.2         | Status and Control Register 2 (ADCSC2) ..... | 175  |
| 10.3.3         | Data Result High Register (ADCRH) .....      | 175  |
| 10.3.4         | Data Result Low Register (ADCRL) .....       | 176  |
| 10.3.5         | Compare Value High Register (ADCCVH) .....   | 176  |
| 10.3.6         | Compare Value Low Register (ADCCVL) .....    | 177  |
| 10.3.7         | Configuration Register (ADCCFG) .....        | 177  |
| 10.3.8         | Pin Control 1 Register (APCTL1) .....        | 178  |
| 10.3.9         | Pin Control 2 Register (APCTL2) .....        | 179  |
| 10.3.10        | Pin Control 3 Register (APCTL3) .....        | 180  |
| 10.4           | Functional Description .....                 | 181  |
| 10.4.1         | Clock Select and Divide Control .....        | 182  |
| 10.4.2         | Input Select and Pin Control .....           | 182  |
| 10.4.3         | Hardware Trigger .....                       | 182  |
| 10.4.4         | Conversion Control .....                     | 182  |
| 10.4.5         | Automatic Compare Function .....             | 185  |
| 10.4.6         | MCU Wait Mode Operation .....                | 185  |
| 10.4.7         | MCU Stop3 Mode Operation .....               | 186  |
| 10.4.8         | MCU Stop2 Mode Operation .....               | 186  |
| 10.5           | Initialization Information .....             | 187  |
| 10.5.1         | ADC Module Initialization Example .....      | 187  |
| 10.6           | Application Information .....                | 189  |
| 10.6.1         | External Pins and Routing .....              | 189  |
| 10.6.2         | Sources of Error .....                       | 190  |

## Chapter 11 Inter-Integrated Circuit (S08IICV2)

|        |                                   |     |
|--------|-----------------------------------|-----|
| 11.1   | Introduction .....                | 193 |
| 11.1.1 | Features .....                    | 195 |
| 11.1.2 | Modes of Operation .....          | 195 |
| 11.1.3 | Block Diagram .....               | 196 |
| 11.2   | External Signal Description ..... | 196 |
| 11.2.1 | SCL — Serial Clock Line .....     | 196 |
| 11.2.2 | SDA — Serial Data Line .....      | 196 |

| Section Number | Title  | Page |
|----------------|--|------|
| 11.3           | Register Definition .....                    | 196  |
| 11.3.1         | IIC Address Register (IICA) .....            | 197  |
| 11.3.2         | IIC Frequency Divider Register (IICF) .....  | 197  |
| 11.3.3         | IIC Control Register (IICC1) .....           | 200  |
| 11.3.4         | IIC Status Register (IICS) .....             | 201  |
| 11.3.5         | IIC Data I/O Register (IICD) .....           | 202  |
| 11.3.6         | IIC Control Register 2 (IICC2) .....         | 202  |
| 11.4           | Functional Description .....                 | 203  |
| 11.4.1         | IIC Protocol .....                           | 203  |
| 11.4.2         | 10-bit Address .....                         | 207  |
| 11.4.3         | General Call Address .....                   | 208  |
| 11.5           | Resets .....                                 | 208  |
| 11.6           | Interrupts .....                             | 208  |
| 11.6.1         | Byte Transfer Interrupt .....                | 208  |
| 11.6.2         | Address Detect Interrupt .....               | 208  |
| 11.6.3         | Arbitration Lost Interrupt .....             | 208  |
| 11.7           | Initialization/Application Information ..... | 210  |

## Chapter 12

### Serial Peripheral Interface (S08SPIV3)

|        |   |     |
|--------|---|-----|
| 12.1   | Introduction .....                          | 213 |
| 12.1.1 | Features .....                              | 215 |
| 12.1.2 | Block Diagrams .....                        | 215 |
| 12.1.3 | SPI Baud Rate Generation .....              | 217 |
| 12.2   | External Signal Description .....           | 218 |
| 12.2.1 | SPSCK — SPI Serial Clock .....              | 218 |
| 12.2.2 | MOSI — Master Data Out, Slave Data In ..... | 218 |
| 12.2.3 | MISO — Master Data In, Slave Data Out ..... | 218 |
| 12.2.4 | $\overline{SS}$ — Slave Select .....        | 218 |
| 12.3   | Modes of Operation .....                    | 219 |
| 12.3.1 | SPI in Stop Modes .....                     | 219 |
| 12.4   | Register Definition .....                   | 219 |
| 12.4.1 | SPI Control Register 1 (SPIC1) .....        | 219 |
| 12.4.2 | SPI Control Register 2 (SPIC2) .....        | 220 |
| 12.4.3 | SPI Baud Rate Register (SPIBR) .....        | 221 |
| 12.4.4 | SPI Status Register (SPIS) .....            | 222 |
| 12.4.5 | SPI Data Register (SPID) .....              | 223 |
| 12.5   | Functional Description .....                | 224 |
| 12.5.1 | SPI Clock Formats .....                     | 224 |
| 12.5.2 | SPI Interrupts .....                        | 227 |
| 12.5.3 | Mode Fault Detection .....                  | 227 |

**Chapter 13**  
**Serial Communications Interface (S08SCIV4)**

|        |  |     |
|--------|--|-----|
| 13.1   | Introduction .....                               | 229 |
| 13.1.1 | Features .....                                   | 231 |
| 13.1.2 | Modes of Operation .....                         | 231 |
| 13.1.3 | Block Diagram .....                              | 232 |
| 13.2   | Register Definition .....                        | 234 |
| 13.2.1 | SCI Baud Rate Registers (SCI1BDH, SCI1BDL) ..... | 234 |
| 13.2.2 | SCI Control Register 1 (SCI1C1) .....            | 235 |
| 13.2.3 | SCI Control Register 2 (SCI1C2) .....            | 236 |
| 13.2.4 | SCI Status Register 1 (SCI1S1) .....             | 237 |
| 13.2.5 | SCI Status Register 2 (SCI1S2) .....             | 239 |
| 13.2.6 | SCI Control Register 3 (SCI1C3) .....            | 240 |
| 13.2.7 | SCI Data Register (SCI1D) .....                  | 241 |
| 13.3   | Functional Description .....                     | 241 |
| 13.3.1 | Baud Rate Generation .....                       | 241 |
| 13.3.2 | Transmitter Functional Description .....         | 242 |
| 13.3.3 | Receiver Functional Description .....            | 243 |
| 13.3.4 | Interrupts and Status Flags .....                | 245 |
| 13.3.5 | Additional SCI Functions .....                   | 246 |

**Chapter 14**  
**Real-Time Counter (S08RTCV1)**

|        |   |     |
|--------|---|-----|
| 14.1   | Introduction .....                            | 249 |
| 14.1.1 | RTC Clock Signal Names .....                  | 249 |
| 14.1.2 | Features .....                                | 251 |
| 14.1.3 | Modes of Operation .....                      | 251 |
| 14.1.4 | Block Diagram .....                           | 252 |
| 14.2   | External Signal Description .....             | 252 |
| 14.3   | Register Definition .....                     | 252 |
| 14.3.1 | RTC Status and Control Register (RTCSC) ..... | 253 |
| 14.3.2 | RTC Counter Register (RTCCNT) .....           | 254 |
| 14.3.3 | RTC Modulo Register (RTCMOD) .....            | 254 |
| 14.4   | Functional Description .....                  | 254 |
| 14.4.1 | RTC Operation Example .....                   | 255 |
| 14.5   | Initialization/Application Information .....  | 256 |

**Chapter 15**  
**Timer Pulse-Width Modulator (S08TPMV3)**

|        |                          |     |
|--------|--------------------------|-----|
| 15.1   | Introduction .....       | 259 |
| 15.1.1 | Features .....           | 261 |
| 15.1.2 | Modes of Operation ..... | 261 |



| Section Number | Title  | Page |
|----------------|--|------|
| 15.1.3         | Block Diagram .....  | 262  |
| 15.2           | Signal Description .....                                   | 264  |
| 15.2.1         | Detailed Signal Descriptions .....                         | 264  |
| 15.3           | Register Definition .....                                  | 268  |
| 15.3.1         | TPM Status and Control Register (TPMxSC) .....             | 268  |
| 15.3.2         | TPM-Counter Registers (TPMxCNTH:TPMxCNTL) .....            | 269  |
| 15.3.3         | TPM Counter Modulo Registers (TPMxMODH:TPMxMODL) .....     | 270  |
| 15.3.4         | TPM Channel n Status and Control Register (TPMxCnSC) ..... | 271  |
| 15.3.5         | TPM Channel Value Registers (TPMxCnVH:TPMxCnVL) .....      | 272  |
| 15.4           | Functional Description .....                               | 274  |
| 15.4.1         | Counter .....  | 274  |
| 15.4.2         | Channel Mode Selection .....                               | 276  |
| 15.5           | Reset Overview .....                                       | 279  |
| 15.5.1         | General .....  | 279  |
| 15.5.2         | Description of Reset Operation .....                       | 279  |
| 15.6           | Interrupts .....   | 279  |
| 15.6.1         | General .....  | 279  |
| 15.6.2         | Description of Interrupt Operation .....                   | 280  |
| 15.7           | The Differences from TPM v2 to TPM v3.....                 | 281  |

## Chapter 16 Development Support

|        |   |     |
|--------|---|-----|
| 16.1   | Introduction .....  | 287 |
| 16.1.1 | Forcing Active Background .....                             | 287 |
| 16.1.2 | Features .....  | 288 |
| 16.2   | Background Debug Controller (BDC) .....                     | 288 |
| 16.2.1 | BKGD Pin Description .....                                  | 289 |
| 16.2.2 | Communication Details .....                                 | 290 |
| 16.2.3 | BDC Commands .....  | 294 |
| 16.2.4 | BDC Hardware Breakpoint .....                               | 296 |
| 16.3   | On-Chip Debug System (DBG) .....                            | 297 |
| 16.3.1 | Comparators A and B .....                                   | 297 |
| 16.3.2 | Bus Capture Information and FIFO Operation .....            | 297 |
| 16.3.3 | Change-of-Flow Information .....                            | 298 |
| 16.3.4 | Tag vs. Force Breakpoints and Triggers .....                | 298 |
| 16.3.5 | Trigger Modes .....   | 299 |
| 16.3.6 | Hardware Breakpoints .....                                  | 301 |
| 16.4   | Register Definition .....                                   | 301 |
| 16.4.1 | BDC Registers and Control Bits .....                        | 301 |
| 16.4.2 | System Background Debug Force Reset Register (SBD FR) ..... | 303 |
| 16.4.3 | DBG Registers and Control Bits .....                        | 304 |

## Appendix A Electrical Characteristics

|      |  |     |
|------|--|-----|
| A.1  | Introduction .....                               | 309 |
| A.2  | Parameter Classification .....                   | 309 |
| A.3  | Absolute Maximum Ratings .....                   | 309 |
| A.4  | Thermal Characteristics .....                    | 310 |
| A.5  | ESD Protection and Latch-Up Immunity .....       | 312 |
| A.6  | DC Characteristics .....                         | 313 |
| A.7  | Supply Current Characteristics .....             | 315 |
| A.8  | Analog Comparator (ACMP) Electricals .....       | 316 |
| A.9  | ADC Characteristics .....                        | 316 |
| A.10 | External Oscillator (XOSC) Characteristics ..... | 320 |
| A.11 | MCG Specifications .....                         | 321 |
| A.12 | AC Characteristics .....                         | 323 |
|      | A.12.1 Control Timing .....                      | 323 |
|      | A.12.2 Timer/PWM .....                           | 324 |
|      | A.12.3 SPI .....                                 | 326 |
| A.13 | Flash and EEPROM .....                           | 329 |
| A.14 | EMC Performance .....                            | 330 |
|      | A.14.1 Radiated Emissions .....                  | 330 |

## Appendix B Timer Pulse-Width Modulator (TPMV2)

|     |  |     |
|-----|--|-----|
|     | B.0.1 Features .....   | 331 |
|     | B.0.2 Block Diagram .....  | 331 |
| B.1 | External Signal Description .....                                  | 333 |
|     | B.1.1 External TPM Clock Sources .....                             | 333 |
|     | B.1.2 TPMxCHn — TPMx Channel n I/O Pins .....                      | 333 |
| B.2 | Register Definition .....  | 333 |
|     | B.2.1 Timer Status and Control Register (TPMxSC) .....             | 334 |
|     | B.2.2 Timer Counter Registers (TPMxCNTH:TPMxCNTL) .....            | 335 |
|     | B.2.3 Timer Counter Modulo Registers (TPMxMODH:TPMxMODL) .....     | 336 |
|     | B.2.4 Timer Channel n Status and Control Register (TPMxCnSC) ..... | 337 |
|     | B.2.5 Timer Channel Value Registers (TPMxCnVH:TPMxCnVL) .....      | 338 |
| B.3 | Functional Description .....                                       | 339 |
|     | B.3.1 Counter .....  | 339 |
|     | B.3.2 Channel Mode Selection .....                                 | 340 |
|     | B.3.3 Center-Aligned PWM Mode .....                                | 342 |
| B.4 | TPM Interrupts .....   | 343 |
|     | B.4.1 Clearing Timer Interrupt Flags .....                         | 343 |
|     | B.4.2 Timer Overflow Interrupt Description .....                   | 343 |
|     | B.4.3 Channel Event Interrupt Description .....                    | 344 |

| <b>Section Number</b> | <b>Title</b>                       | <b>Page</b> |
|-----------------------|------------------------------------|-------------|
| B.4.4                 | PWM End-of-Duty-Cycle Events ..... | 344         |

**Appendix C**  
**Ordering Information and Mechanical Drawings**

|       |                                 |     |
|-------|---------------------------------|-----|
| C.1   | Ordering Information .....      | 345 |
| C.1.1 | MC9S08DN60 Series Devices ..... | 345 |
| C.2   | Mechanical Drawings .....       | 345 |

# Chapter 1

## Device Overview

Controller Area Network MC9S08DN60 Series devices provide peripheral flexibility and offer a pin and code compatibility with MC9S08DV60 and MC9S08DZ60 Series devices when the CAN module is required.

### 1.1 Devices in the MC9S08DN60 Series

This data sheet covers members of the MC9S08DN60 Series of MCUs:

- MC9S08DN60
- MC9S08DN48
- MC9S08DN32
- MC9S08DN16

Table 1-1 summarizes the feature set available in the MC9S08DN60 Series.

**Table 1-1. MC9S08DN60 Series Features by MCU and Pin Count**

| Feature             | MC9S08DN60 |                  |    | MC9S08DN48 |                  |    | MC9S08DN32 |                  |    | MC9S08DN16       |    |
|---------------------|------------|------------------|----|------------|------------------|----|------------|------------------|----|------------------|----|
|                     |            |                  |    |            |                  |    |            |                  |    |                  |    |
| Flash size (bytes)  | 62080      |                  |    | 49152      |                  |    | 33792      |                  |    | 16896            |    |
| RAM size (bytes)    | 2048       |                  |    | 2048       |                  |    | 1536       |                  |    | 1024             |    |
| EEPROM size (bytes) | 2048       |                  |    | 1536       |                  |    | 1024       |                  |    | 512              |    |
| Pin quantity        | 64         | 48               | 32 | 64         | 48               | 32 | 64         | 48               | 32 | 48               | 32 |
| ACMP1               | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| ACMP2               | yes        | yes <sup>1</sup> | no | yes        | yes <sup>1</sup> | no | yes        | yes <sup>1</sup> | no | yes <sup>1</sup> | no |
| ADC channels        | 16         | 16               | 10 | 16         | 16               | 10 | 16         | 16               | 10 | 16               | 10 |
| DBG                 | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| IIC                 | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| IRQ                 | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| MCG                 | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| RTC                 | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| SCI1                | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| SPI                 | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| TPM1 channels       | 6          | 6                | 4  | 6          | 6                | 4  | 6          | 6                | 4  | 6                | 4  |
| TPM2 channels       | 2          |                  |    |            |                  |    |            |                  |    |                  |    |
| XOSC                | yes        |                  |    |            |                  |    |            |                  |    |                  |    |
| COP Watchdog        | yes        |                  |    |            |                  |    |            |                  |    |                  |    |

<sup>1</sup> ACMP20 is not available.

## 1.2 MCU Block Diagram

Figure 1-1 is the MC9S08DN60 Series system-level block diagram.

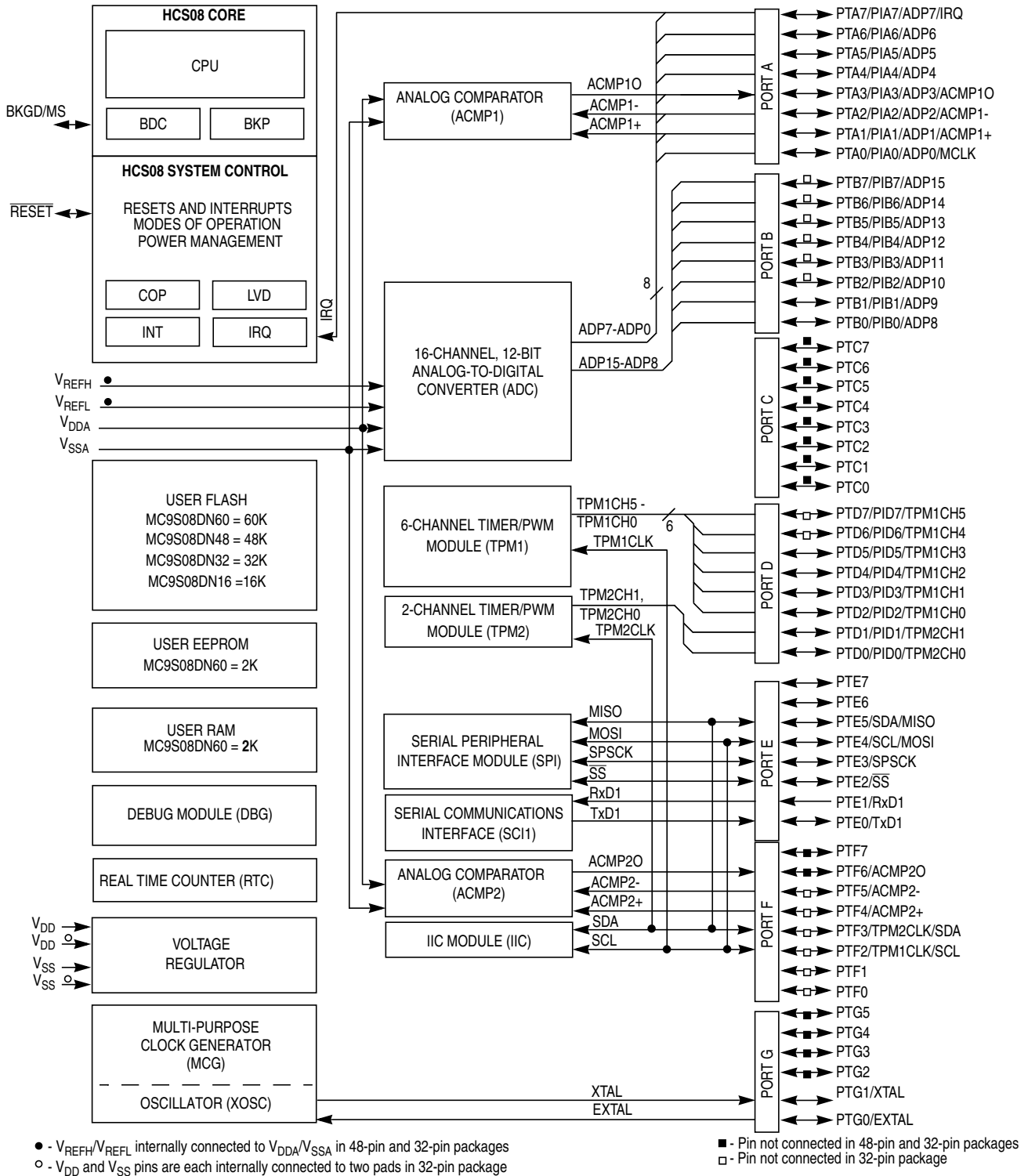


Figure 1-1. MC9S08DN60 Block Diagram

Table 1-2 provides the functional version of the on-chip modules.

**Table 1-2. Module Versions**

| Module                                | Version        |
|---------------------------------------|----------------|
| Central Processor Unit (CPU)          | 3              |
| Multi-Purpose Clock Generator (MCG)   | 1              |
| Analog Comparator (ACMP)              | 3              |
| Analog-to-Digital Converter (ADC)     | 1              |
| Inter-Integrated Circuit (IIC)        | 2              |
| Serial Peripheral Interface (SPI)     | 3              |
| Serial Communications Interface (SCI) | 4              |
| Real-Time Counter (RTC)               | 1              |
| Timer Pulse Width Modulator (TPM)     | 3 <sup>1</sup> |
| Debug Module (DBG)                    | 2              |

<sup>1</sup> 3M05C and older masks have TPM version 2.

### 1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function.

The following are the clocks used in this MCU:

- BUSCLK — The frequency of the bus is always half of MCGOUT.
- LPO — Independent 1-kHz clock that can be selected as the source for the COP and RTC modules.
- MCGOUT — Primary output of the MCG and is twice the bus frequency.
- MCGLCLK — Development tools can select this clock source to speed up BDC communications in systems where BUSCLK is configured to run at a very slow frequency.
- MCGERCLK — External reference clock can be selected as the RTC clock source. It can also be used as the alternate clock for the ADC.
- MCGIRCLK — Internal reference clock can be selected as the RTC clock source.
- MCGFFCLK — Fixed frequency clock can be selected as clock source for the TPM1 and TPM2.
- TPM1CLK — External input clock source for TPM1.
- TPM2CLK — External input clock source for TPM2.

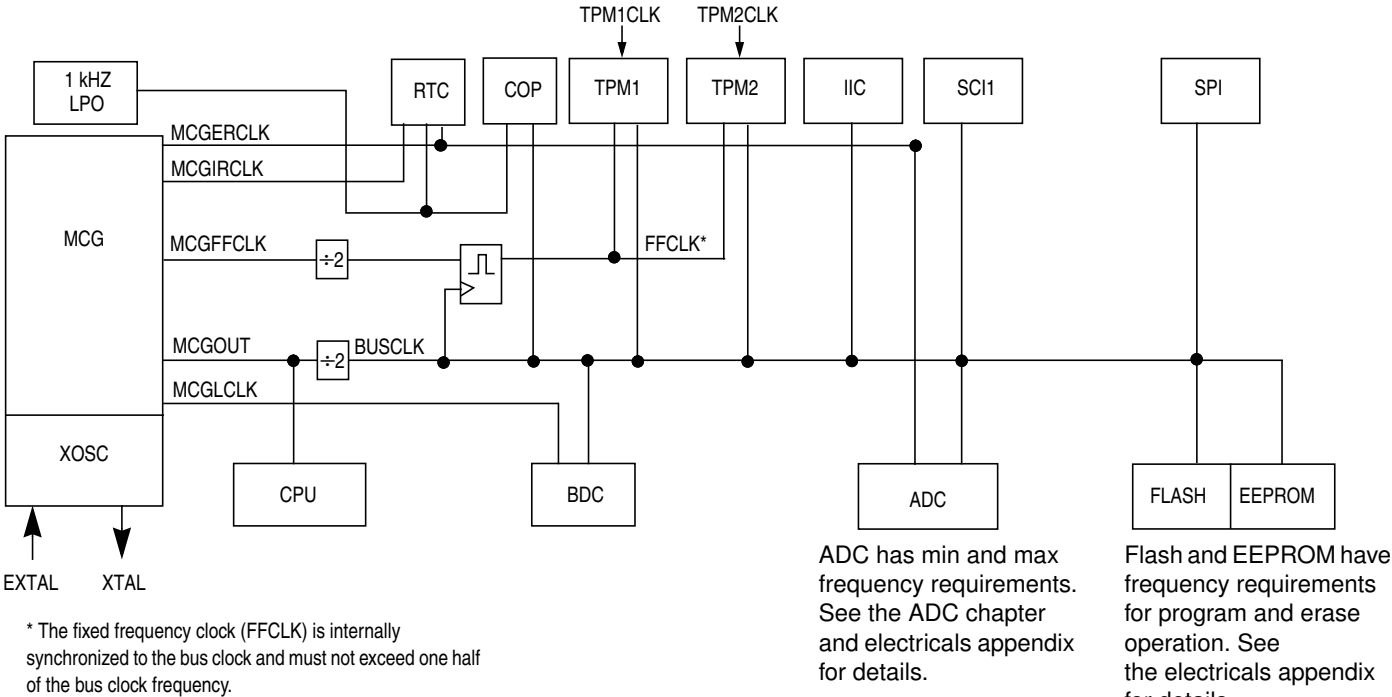


Figure 1-2. MC9S08DN60 System Clock Distribution Diagram

# Chapter 2

## Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

### 2.1 Device Pin Assignment

This section shows the pin assignments for MC9S08DN60 Series MCUs in the available packages.

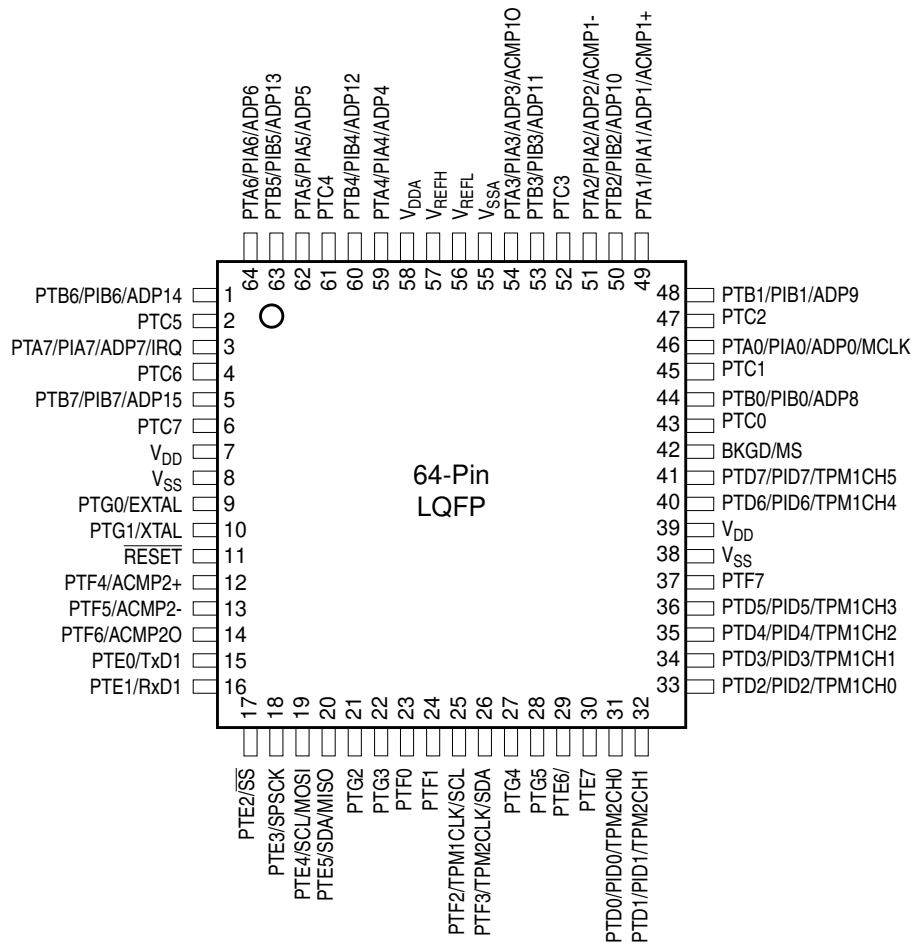
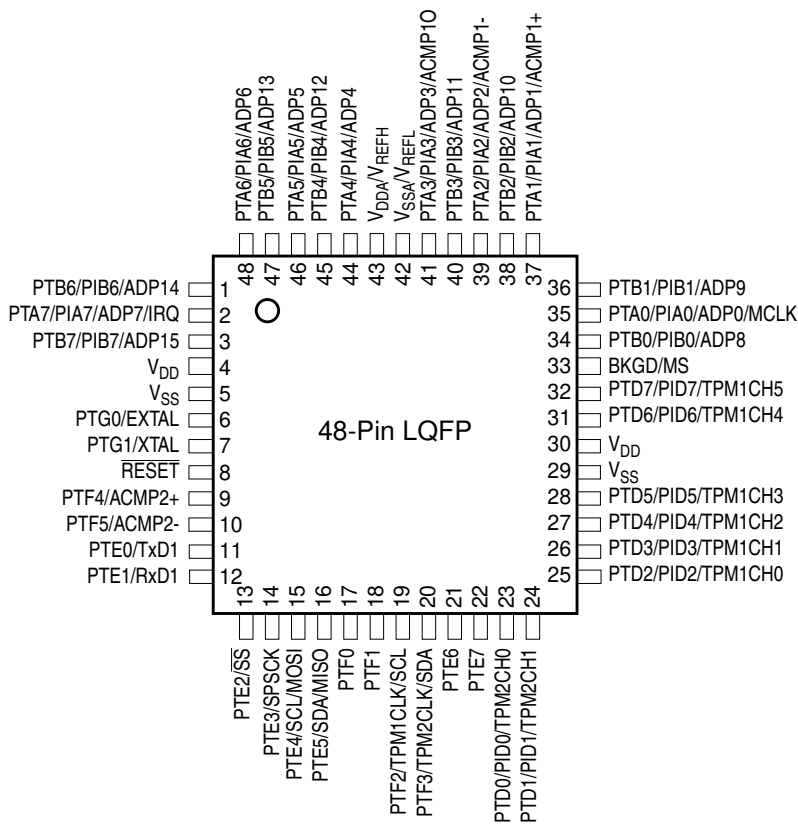


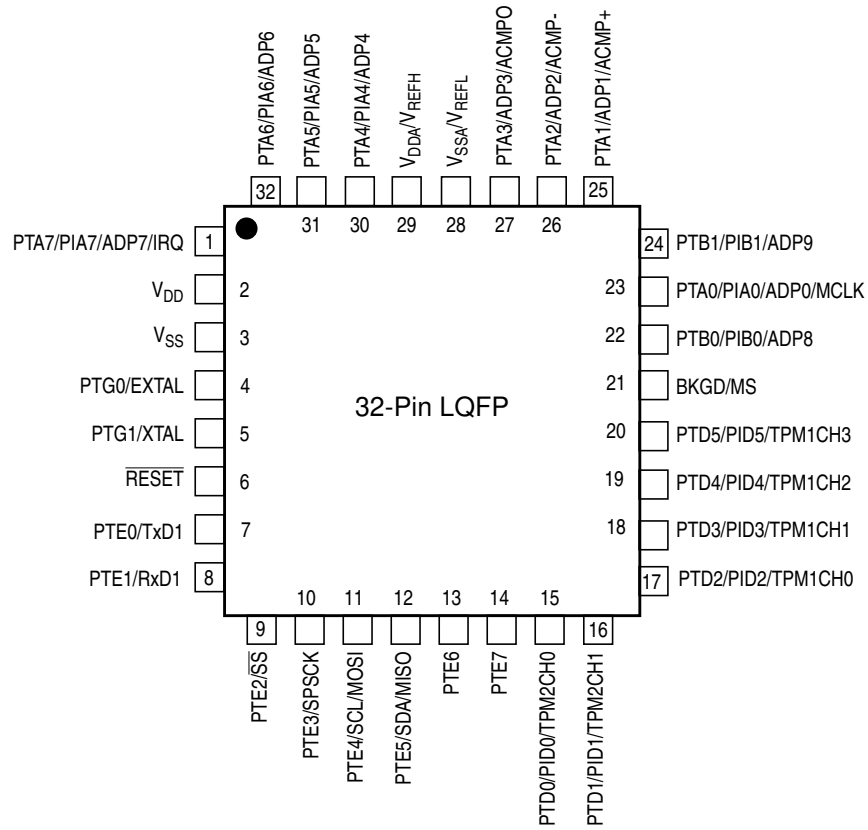
Figure 2-1. 64-Pin LQFP





V<sub>REFH</sub> and V<sub>REFL</sub> are internally connected to V<sub>DDA</sub> and V<sub>SSA</sub>, respectively.

**Figure 2-2. 48-Pin LQFP**



V<sub>REFH</sub> and V<sub>REFL</sub> are internally connected to V<sub>DDA</sub> and V<sub>SSA</sub>, respectively.

**Figure 2-3. 32-Pin LQFP**