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MC9S08DZ60
MC9S08DZ48
MC9S08DZ32
MC9S08DZ16

Data Sheet

HCS08
Microcontrollers

MC9S08DZ60
Rev. 4
6/2008

freescale.com

MC9S08DZ60 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (20-MHz bus)
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- Flash read/program/erase over full operating voltage and temperature
  - MC9S08DZ60 = 60K
  - MC9S08DZ48 = 48K
  - MC9S08DZ32 = 32K
  - MC9S08DZ16 = 16K
- Up to 2K EEPROM in-circuit programmable memory; 8-byte single-page or 4-byte dual-page erase sector; Program and Erase while executing Flash; Erase abort
- Up to 4K random-access memory (RAM)

Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time interrupt for use in run, wait, and stop

Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Multi-purpose Clock Generator (MCG) — PLL and FLL modes (FLL capable of 1.5% deviation using internal temperature compensation); Internal reference clock with trim adjustment (trimmed at factory, with trim value stored in flash); External reference with oscillator/resonator options

System Protection

- Watchdog computer operating properly (COP) reset with option to run from backup dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- Flash block protect
- Loss-of-lock protection

Development Support

- Single-wire background debug interface
- On-chip, in-circuit emulation (ICE) with real-time bus capture

Peripherals

- **ADC** — 24-channel, 12-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel
- **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage
- **MSCAN** — CAN protocol - Version 2.0 A, B; standard and extended data frames; Support for remote frames; Five receive buffers with FIFO storage scheme; Flexible identifier acceptance filters programmable as: 2 x 32-bit, 4 x 16-bit, or 8 x 8-bit
- **SCIx** — Two SCIs supporting LIN 2.0 Protocol and SAE J2602 protocols; Full duplex non-return to zero (NRZ); Master extended break generation; Slave extended break detection; Wakeup on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; General Call Address; Interrupt driven byte-by-byte data transfer
- **TPMx** — One 6-channel (TPM1) and one 2-channel (TPM2); Selectable input capture, output compare, or buffered edge-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; Real-time clock capabilities using external crystal and RTC for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components

Input/Output

- 53 general-purpose input/output (I/O) pins and 1 input-only pin
- 24 interrupt pins with selectable polarity on each pin
- Hysteresis and configurable pull device on all input pins.
- Configurable slew rate and drive strength on all output pins.

Package Options

- 64-pin low-profile quad flat-pack (LQFP) — 10x10 mm
- 48-pin low-profile quad flat-pack (LQFP) — 7x7 mm
- 32-pin low-profile quad flat-pack (LQFP) — 7x7 mm

MC9S08DZ60 Data Sheet

Covers MC9S08DZ60
MC9S08DZ48
MC9S08DZ32
MC9S08DZ16

MC9S08DZ60
Rev. 4
6/2008

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	6/2006	Advance Information for alpha samples customers
2	9/2007	Product Launch. Removed the 64-pin QFN package. Changed from standard to extended mode for MSCAN registers in register summary. Corrected Block diagrams for SCI. Updated the latest Temp Sensor information. Made FTSTMOD reserved. Updated device to use the ADC 12-bit module. Revised the MCG module. Updated the CPU Instruction Set table. Updated the TPM block module to version 3. Added the TPM block module version 2 as an appendix for devices using 3M05C (or earlier) mask sets. Heavily revised the Electricals appendix.
3	10/2007	Removed two tables that were inadvertently included in the MC9S08DZ60 version of the book.
4	6/2008	Sustaining update. Incorporated PS Issues # 2765, 3177, 3236, 3292, 3311, 3312, 3326, 3335, 3345, 3382, 2795, 3382 and 3386 PLL Jitter Spec update. Also, added internal reference clock trim adjustment statement to Features page. Updated the TPM module to the latest version. Adjusted values in Table A-13 Control Timing row 2 and in Table A-6 DC Characteristics row 24 so that it references 5.0 V instead of 3.0 V.

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List of Chapters

Contents

Section Number **Title** **Page**

Chapter 1
Device Overview

Chapter 2
Pins and Connections

Chapter 3
Modes of Operation

Chapter 4
Memory

Chapter 5
Resets, Interrupts, and General System Control

Chapter 6
Parallel Input/Output Control

Chapter 7
Central Processor Unit (S08CPUV3)

Chapter 8
Multi-Purpose Clock Generator (S08MCGV1)

Chapter 9
Analog Comparator (S08ACMPV3)

Chapter 10
Analog-to-Digital Converter (S08ADC12V1)

Chapter 11
Inter-Integrated Circuit (S08IICV2)

Chapter 12
Freescale Controller Area Network (S08MSCANV1)

Chapter 13
Serial Peripheral Interface (S08SPIV3)

Chapter 14
Serial Communications Interface (S08SCIV4)

Chapter 15
Real-Time Counter (S08RTCV1)

Chapter 16
Timer Pulse-Width Modulator (S08TPMV3)

Chapter 17
Development Support

Appendix A
Electrical Characteristics

Appendix B
Timer Pulse-Width Modulator (TPMV2)

Appendix C
Ordering Information and Mechanical Drawings

Chapter 1
Device Overview

MC9S08DZ60 Series devices provide significant value to customers looking to combine Controller Area Network (CAN) and embedded EEPROM in their applications. This combination will provide lower costs, enhanced performance, and higher quality.

1.1 Devices in the MC9S08DZ60 Series

This data sheet covers members of the MC9S08DZ60 Series of MCUs:

- MC9S08DZ60
- MC9S08DZ48
- MC9S08DZ32
- MC9S08DZ16

Table 1-1 summarizes the feature set available in the MC9S08DZ60 Series.

Table 1-1. MC9S08DZ60 Series Features by MCU and Pin Count

Feature	MC9S08DZ60			MC9S08DZ48			MC9S08DZ32			MC9S08DZ16	
Flash size (bytes)	60032			49152			33792			16896	
RAM size (bytes)	4096			3072			2048			1024	
EEPROM size (bytes)	2048			1536			1024			512	
Pin quantity	64	48	32	64	48	32	64	48	32	48	32
ACMP1	yes										
ACMP2	yes	yes[1]	no	yes	yes[1]	no	yes	yes[1]	no	yes[1]	no
ADC channels	24	16	10	24	16	10	24	16	10	16	10
DBG	yes										
IIC	yes										
IRQ	yes										
MCG	yes										
MSCAN	yes										
RTC	yes										
SCI1	yes										
SCI2	yes										
SPI	yes										
TPM1 channels	6	6	4	6	6	4	6	6	4	6	4
TPM2 channels	2										
XOSC	yes										
COP Watchdog	yes										

[1] ACMP2O is not available.

1.2 MCU Block Diagram

Figure 1-1 is the MC9S08DZ60 Series system-level block diagram.

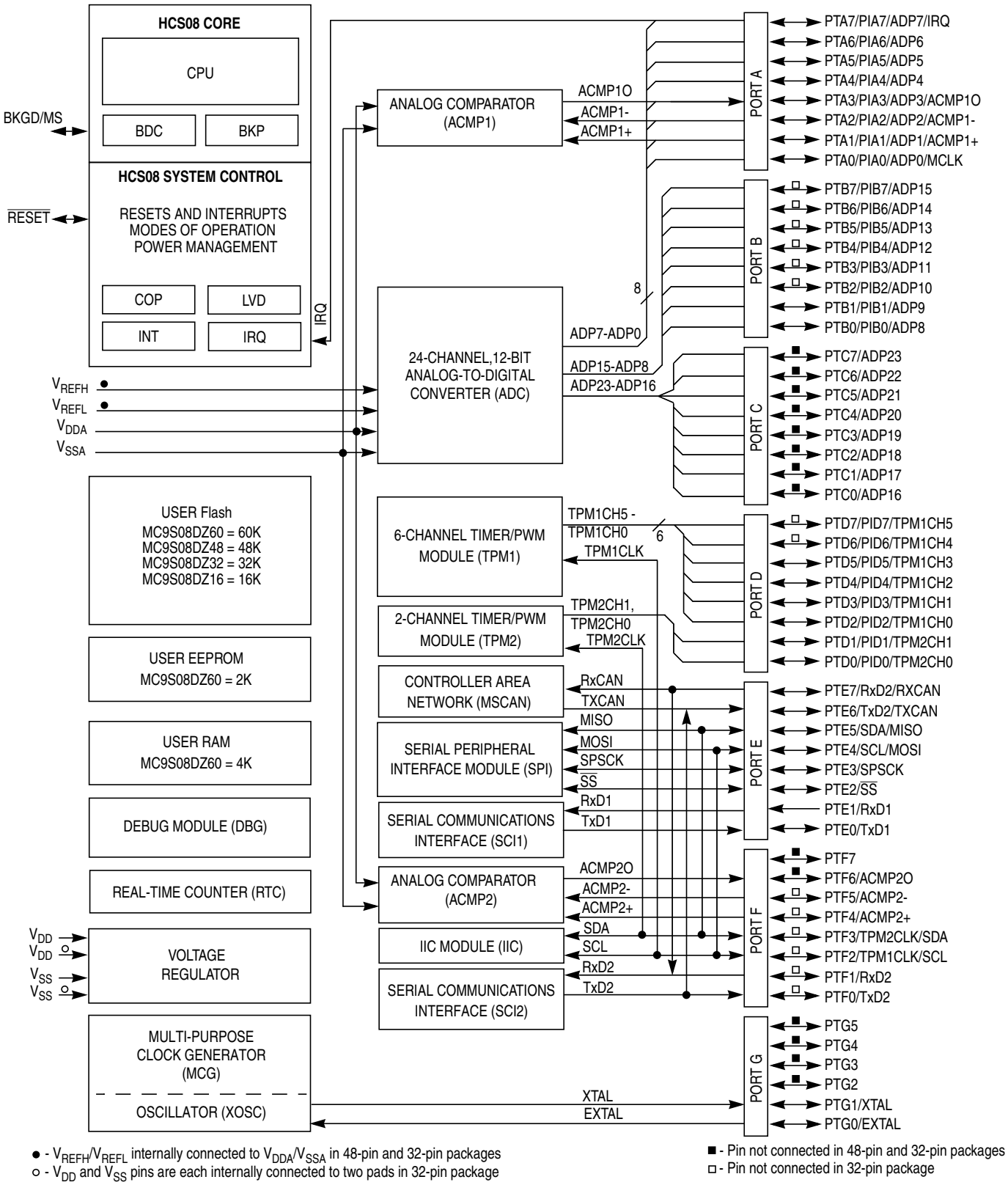

Figure 1-1. MC9S08DZ60 Block Diagram

Table 1-2 provides the functional version of the on-chip modules.

Table 1-2. Module Versions

Module		Version
Central Processor Unit	(CPU)	3
Multi-Purpose Clock Generator	(MCG)	1
Analog Comparator	(ACMP)	3
Analog-to-Digital Converter	(ADC)	1
Inter-Integrated Circuit	(IIC)	2
Freescale's CAN	(MSCAN)	1
Serial Peripheral Interface	(SPI)	3
Serial Communications Interface	(SCI)	4
Real-Time Counter	(RTC)	1
Timer Pulse Width Modulator	(TPM)	3[1]
Debug Module	(DBG)	2

[1] 3M05C and older masks have TPM version 2.

1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function.

The following are the clocks used in this MCU:

- BUSCLK — The frequency of the bus is always half of MCGOUT.
- LPO — Independent 1-kHz clock that can be selected as the source for the COP and RTC modules.
- MCGOUT — Primary output of the MCG and is twice the bus frequency.
- MCGLCLK — Development tools can select this clock source to speed up BDC communications in systems where BUSCLK is configured to run at a very slow frequency.
- MCGERCLK — External reference clock can be selected as the RTC clock source. It can also be used as the alternate clock for the ADC and MSCAN.
- MCGIRCLK — Internal reference clock can be selected as the RTC clock source.
- MCGFFCLK — Fixed frequency clock can be selected as clock source for the TPM1 and TPM2.
- TPM1CLK — External input clock source for TPM1.
- TPM2CLK — External input clock source for TPM2.

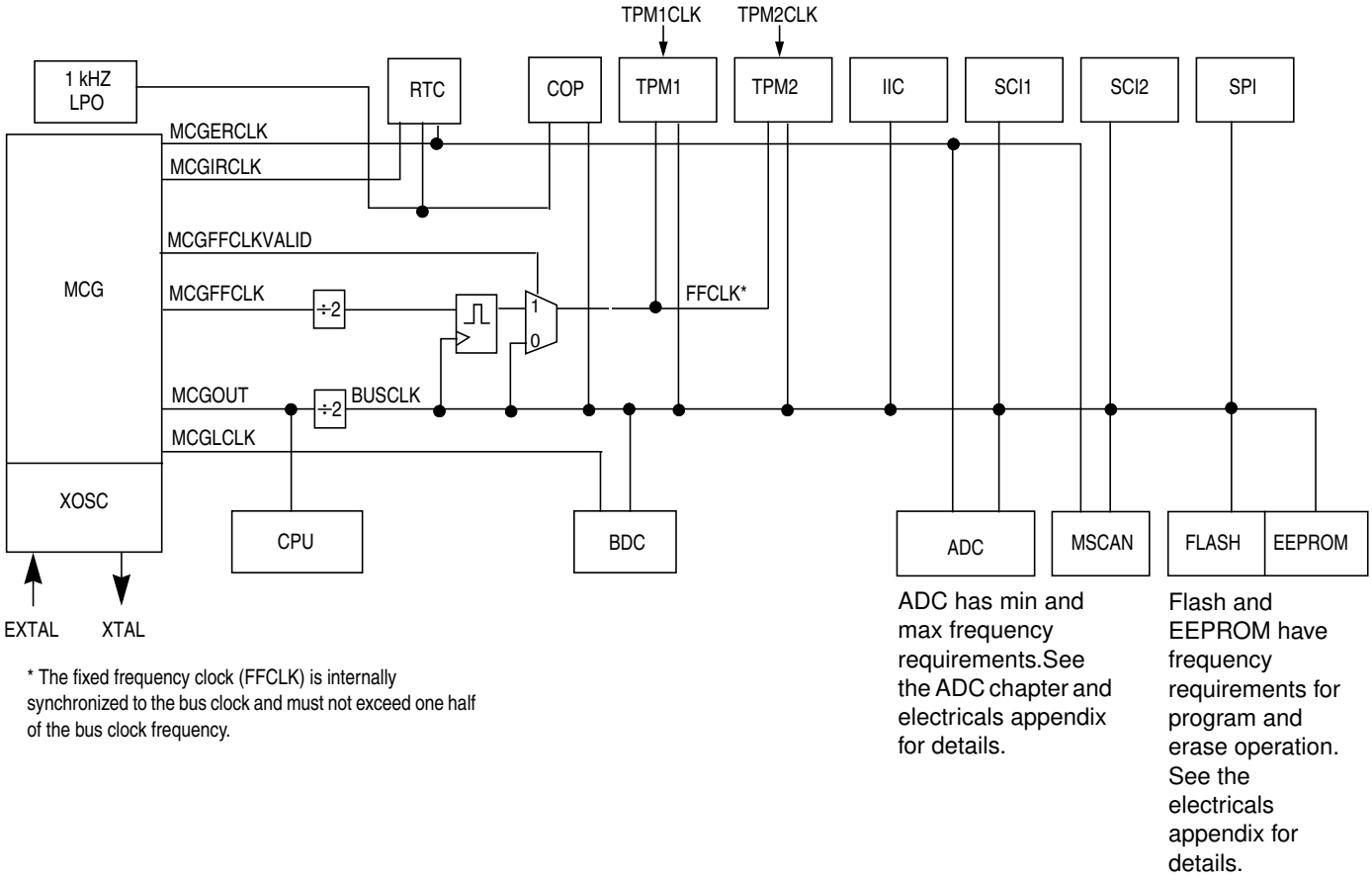

Figure 1-2. MC9S08DZ60 System Clock Distribution Diagram