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# MC9S08QD4
# MC9S08QD2
# S9S08QD4
# S9S08QD2

Data Sheet

***HCS08***
***Microcontrollers***

MC9S08QD4
Rev. 6
10/2010

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# MC9S08QD4 Series Features

### 8-Bit HCS08 Central Processor Unit (CPU)

- 16 MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Background debugging system
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- Support for up to 32 interrupt/reset sources

### Memory

- Flash read/program/erase over full operating voltage and temperature
- Flash size:
  - MC9S08QD4/S9S08QD4: 4096 bytes
  - MC9S08QD2/S9S08QD2: 2048 bytes
- RAM size
  - MC9S08QD4/S9S08QD4: 256 bytes
  - MC9S08QD2/S9S08QD2: 128 bytes

### Power-Saving Modes

- Wait plus three stops

### Clock Source Options

- **ICS** — Internal clock source module (ICS) containing a frequency-locked-loop (FLL) controlled by internal. Precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage.

### System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 32 kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt
- Illegal opcode detection with reset
- Illegal address detection with reset
- Flash block protect

### Peripherals

- **ADC** — 4-channel, 10-bit analog-to-digital converter with automatic compare function, asynchronous clock source, temperature sensor and internal bandgap reference channel. ADC is hardware triggerable using the RTI counter.
- **TIM1** — 2-channel timer/pulse-width modulator; each channel can be used for input capture, output compare, buffered edge-aligned PWM, or buffered center-aligned PWM
- **TIM2** — 1-channel timer/pulse-width modulator; each channel can be used for input capture, output compare, buffered edge-aligned PWM, or buffered center-aligned PWM
- **KBI** — 4-pin keyboard interrupt module with software selectable polarity on edge or edge/level modes

### Input/Output

- Four General-purpose input/output (I/O) pins, one input-only pin and one output-only pin. Outputs 10 mA each, 60 mA maximum for package.
- Software selectable pullups on ports when used as input
- Software selectable slew rate control and drive strength on ports when used as output
- Internal pullup on $\overline{\text{RESET}}$ and $\overline{\text{IRQ}}$ pin to reduce customer system cost

### Development Support

- Single-wire background debug interface

### Package Options

- 8-pin SOIC package
- 8-pin PDIP (Only for MC9S08QD4 and MC9S08QD2)
- All package options are RoHS compliant

# MC9S08QD4 Data Sheet

Covers: MC9S08QD4
MC9S08QD2
S9S08QD4
S9S08QD2

MC9S08QD4
Rev. 6
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# Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

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The following revision history table summarizes changes contained in this document.

| Revision Number | Revision Date | Description of Changes |
|---|---|---|
| 1 | 15 Sep 06 | Initial public release |
| 2 | 09 Jan 07 | Added MC9S08QD2 information; added “M” temperature range (–40 °C to 125 °C); updated temperature sensor equation in the ADC chapter. |
| 3 | 19 Nov. 07 | Added S9S08QD4 and S9S08QD2 information for automotive applications. Revised "Accessing (read or write) any flash control register..." to “ Writing any flash control register...” in Section 4.5.5, “Access Errors.” |
| 4 | 9 Sep 08 | Changed the SPMSC3 in Section 5.6, “Low-Voltage Detect (LVD) System,” and Section 5.6.4, “Low-Voltage Warning (LVW),” to SPMSC2.<br>Added $V_{POR}$ to Table A-5.<br>Updated “How to Reach Us” information. |
| 5 | 24 Nov 08 | Revised dc injection current in Table A-5. |
| 6 | 14 Oct 10 | Added $T_{JMax}$ in the Table A-2. |

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# Chapter 1
# Device Overview

## 1.1 Introduction

MC9S08QD4 series MCUs are members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

## 1.2 Devices in the MC9S08QD4 Series

This data sheet covers:

- MC9S08QD4
- MC9S08QD2
- S9S08QD4
- S9S08QD2

**NOTE**

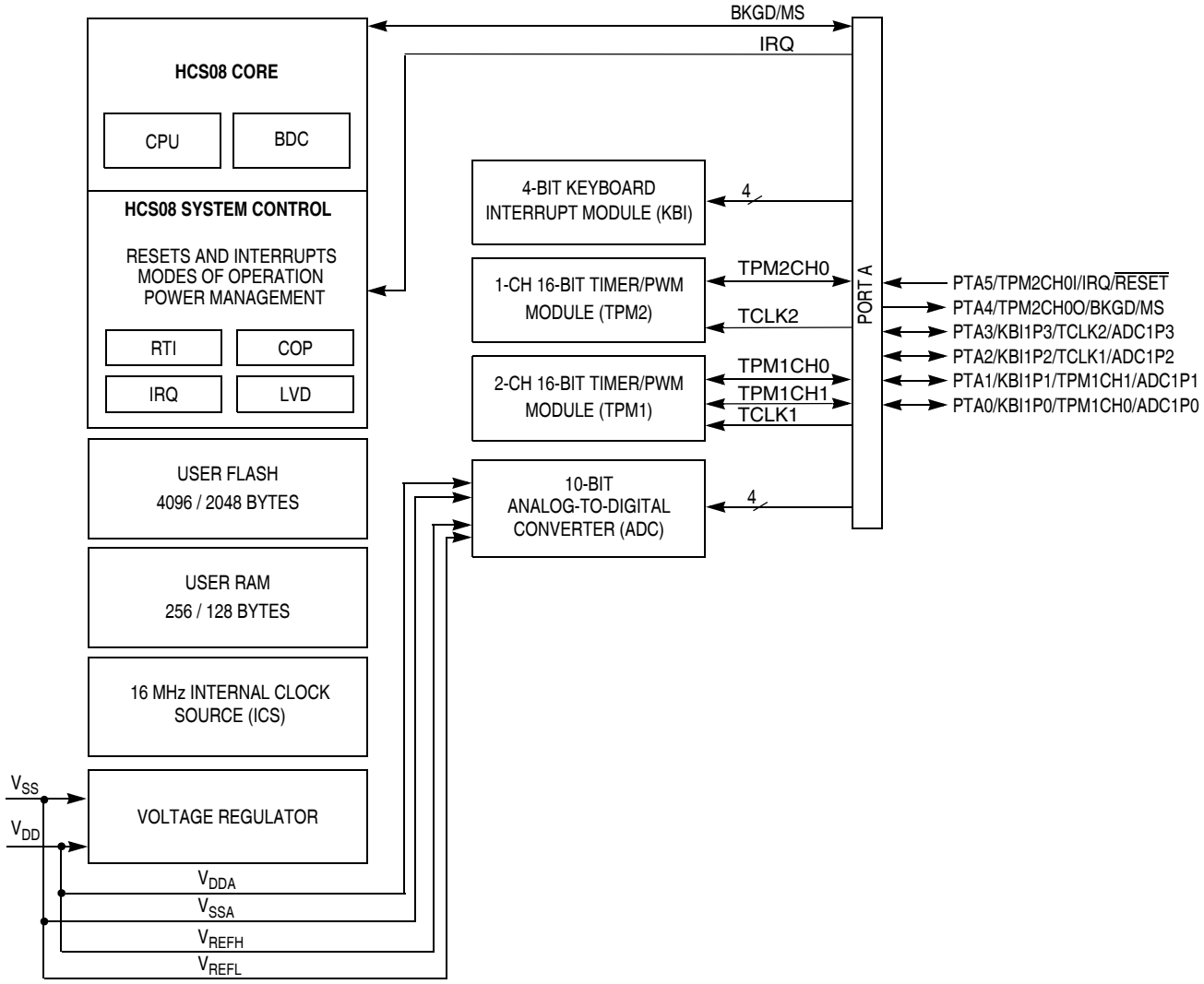
- The MC9S08QD4 and MC9S08QD2 devices are qualified for, and are intended to be used in, *consumer and industrial* applications.
- The S9S08QD4 and S9S08QD2 devices are qualified for, and are intended to be used in, *automotive* applications.

Table 1-1 summarizes the features available in the MCUs.

**Table 1-1. Features by MCU and Package**

| Consumer and Industrial Devices | | |
|---|---|---|
| **Feature** | **MC9S08QD4** | **MC9S08QD2** |
| Flash | 4 KB | 2 KB |
| RAM | 256 B | 128 B |
| ADC | 4-ch, 10-bit | |
| Bus speed | 8 MHz at 5 V | |
| Operating voltage | 2.7 to 5.5 V | |
| 16-bit Timer | One 1-ch; one 2-ch | |
| GPIO | Four I/O; one input-only; one output-only | |
| LVI | Yes | |
| Package options | 8-pin PDIP; 8-pin NB SOIC | |
| Consumer & Industrial Qualified | yes | yes |
| Automotive Qualified | no | no |
| | | |
| **Automotive Devices** | | |
| **Feature** | **S9S08QD4** | **S9S08QD2** |
| Flash | 4 KB | 2 KB |
| RAM | 256 B | 128 B |
| ADC | 4-ch, 10-bit | |
| Bus speed | 8 MHz at 5 V | |
| Operating voltage | 2.7 to 5.5 V | |
| 16-bit Timer | One 1-ch; one 2-ch | |
| GPIO | Four I/O; one input-only; one output-only | |
| LVI | Yes | |
| Package options | 8-pin NB SOIC | |
| Consumer & Industrial Qualified | no | no |
| Automotive Qualified | yes | yes |

## 1.2.1 MCU Block Diagram




NOTES:
1. Port pins are software configurable with pullup device if input port.
2. Port pins are software configurable for output drive strength.
3. Port pins are software configurable for output slew rate control.
4. IRQ contains a software configurable (IRQPDD) pullup/pulldown device if PTA5 enabled as IRQ pin function (IRQPE = 1).
5. $\overline{\text{RESET}}$ contains integrated pullup device if PTA5 enabled as reset pin function (RSTPE = 1).
6. PTA5 does not contain a clamp diode to $V_{DD}$ and must not be driven above $V_{DD}$. The voltage measured on this pin when internal pullup is enabled may be as low as $V_{DD}$ – 0.7 V. The internal gates connected to this pin are pulled to $V_{DD}$.
7. PTA4 contains integrated pullup device if BKGD enabled (BKGDPE = 1).
8. When pin functions as KBI (KBIPEn = 1) and associated pin is configured to enable the pullup device, KBEDGn can be used to reconfigure the pullup as a pulldown device.

**Figure 1-1. MC9S08QD4 Series Block Diagram**

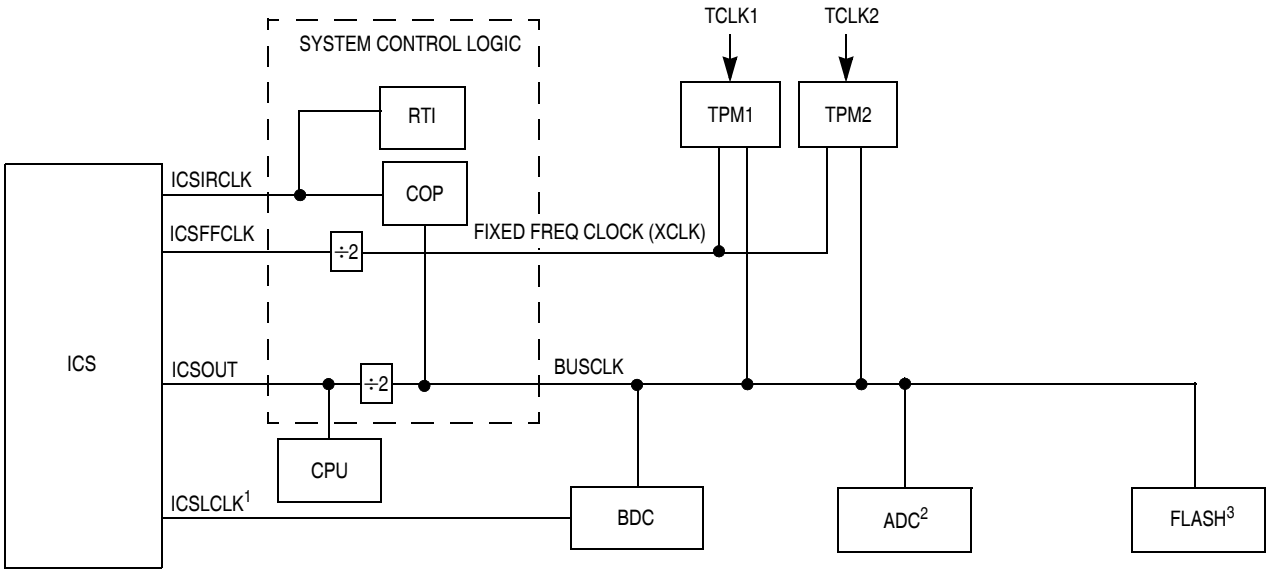
Table 1-2 provides the functional versions of the on-chip modules.

**Table 1-2. Versions of On-Chip Modules**

| Module | | Version |
|---|---|---|
| Analog-to-Digital Converter | (ADC) | 1 |
| Central Processing Unit | (CPU) | 2 |
| Internal Clock Source | (ICS) | 1 |
| Keyboard Interrupt | (KBI) | 2 |
| Timer Pulse-Width Modulator | (TPM) | 2 |

## 1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function. All memory mapped registers associated with the modules are clocked with BUSCLK.




1 ICSLCLK is the alternate BDC clock source for the MC9S08QD4 series.

2 ADC has min. and max frequency requirements. See ADC chapter and Appendix A, “Electrical Characteristics.”

3 Flash has frequency requirements for program and erase operation.See Appendix A, “Electrical Characteristics.”

**Figure 1-2. System Clock Distribution Diagram**

# Chapter 2
# External Signal Description

This chapter describes signals that connect to package pins. It includes pinout diagrams, table of signal properties, and detailed discussions of signals.

## 2.1 Device Pin Assignment

Figure 2-1 shows the pin assignments for the 8-pin packages.

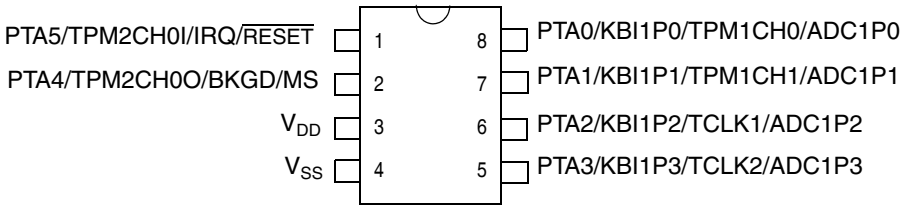
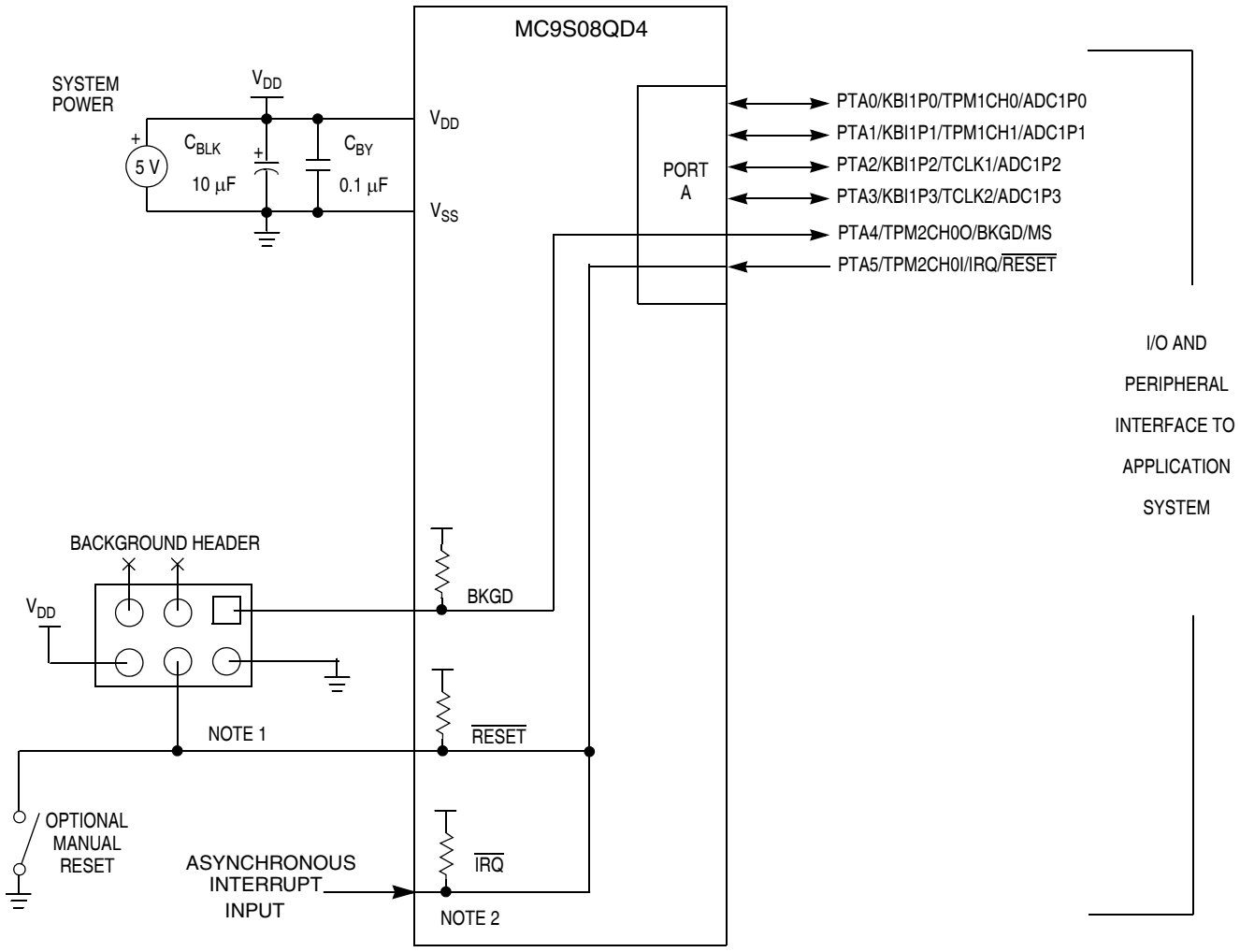



**Figure 2-1. 8-Pin Packages**

## 2.2 Recommended System Connections

Figure 2-2 shows pin connections that are common to almost all MC9S08QD4 series application systems.




NOTES:
1. RESET pin can only be used to reset into user mode, you can not enter BDM using RESET pin. BDM can be entered by holding MS low during POR or writing a 1 to BDFR in SBDFR with MS low after issuing BDM command.
2. IRQ has optional internal pullup/pulldown device

**Figure 2-2. Basic System Connections**

## 2.2.1 Power

$V_{DD}$ and $V_{SS}$ are the primary power supply pins for the MCU. This voltage source supplies power to all I/O buffer circuitry, the ADC module, and to an internal voltage regulator. The internal voltage regulator provides regulated lower-voltage source to the CPU and other internal circuitry of the MCU.

Typically, application systems have two separate capacitors across the power pins: a bulk electrolytic capacitor, such as a 10µF tantalum capacitor, to provide bulk charge storage for the overall system, and a bypass capacitor, such as a 0.1µF ceramic capacitor, located as near to the MCU power pins as practical to suppress high-frequency noise.

### 2.2.2 Oscillator

Out of reset the MCU uses an internally generated clock provided by the internal clock source (ICS) module. The internal frequency is nominally 16 MHz and the default ICS settings will provide for a 4 MHz bus out of reset. For more information on the ICS, see the Internal Clock Source chapter.

### 2.2.3 Reset (Input Only)

After a power-on reset (POR) into user mode, the PTA5/TPM2CH0I/IRQ/$\overline{\text{RESET}}$ pin defaults to a general-purpose input port pin, PTA5. Setting RSTPE in SOPT1 configures the pin to be the $\overline{\text{RESET}}$ input pin. Once configured as $\overline{\text{RESET}}$, the pin will remain $\overline{\text{RESET}}$ until the next POR. The $\overline{\text{RESET}}$ pin can be used to reset the MCU from an external source when the pin is driven low. When enabled as the $\overline{\text{RESET}}$ pin (RSTPE = 1), an internal pullup device is automatically enabled.

After a POR into active background mode, the PTA5/TPM2CH0I/IRQ/$\overline{\text{RESET}}$ pin defaults to the $\overline{\text{RESET}}$ pin.

When TPM2 is configured for input capture, the pin will be the input capture pin TPM2CH0I.

**NOTE**

This pin does not contain a clamp diode to $V_{DD}$ and must not be driven above $V_{DD}$.

The voltage measured on the internally pulled up $\overline{\text{RESET}}$ pin may be as low as $V_{DD} - 0.7$ V. The internal gates connected to this pin are pulled to $V_{DD}$.

### 2.2.4 Background / Mode Select (BKGD/MS)

During a power-on-reset (POR) or background debug force reset (see Section 5.8.3, “System Background Debug Force Reset Register (SBDFR)” for more information), the PTA4/TPM2CH0O/BKGD/MS pin functions as a mode select pin. Immediately after any reset, the pin functions as the background pin and can be used for background debug communication. When enabled as the BKGD/MS pin (BKGDPE = 1), an internal pullup device is automatically enabled.

The background debug communication function is enabled when BKGDPE in SOPT1 is set. BKGDPE is set following any reset of the MCU and must be cleared to use the PTA4/TPM2CH0O/BKGD/MS pins alternative pin functions.

If nothing is connected to this pin, the MCU will enter normal operating mode at the rising edge of the internal reset after a POR or force BDC reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during a POR or immediately after issuing a background debug force reset, which will force the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU’s BDC clock per bit time. The target MCU’s BDC clock could be as fast as the maximum bus clock rate, so there must never be any significant capacitance connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high speedup pulses to ensure fast rise times. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

### 2.2.5 General-Purpose I/O and Peripheral Ports

The MC9S08QD4 series of MCUs support up to 4 general-purpose I/O pins, 1 input-only pin and 1 output-only pin, which are shared with on-chip peripheral functions (timers, serial I/O, ADC, keyboard interrupts, etc.). On each of the MC9S08QD4 series devices there is one input-only and one output-only port pin.

When a port pin is configured as a general-purpose output or a peripheral uses the port pin as an output, software can select one of two drive strengths and enable or disable slew rate control. When a port pin is configured as a general-purpose input or a peripheral uses the port pin as an input, software can enable a pullup device.

For information about controlling these pins as general-purpose I/O pins, see the Chapter 6, “Parallel Input/Output Control.” For information about how and when on-chip peripheral systems use these pins, see the appropriate chapter referenced in Table 2-1.

Immediately after reset, all pins that are not output-only are configured as high-impedance, general-purpose inputs with internal pullup devices disabled. After reset, the output-only port function is not enabled but is configured for low output drive strength with slew rate control enabled. The PTA4 pin defaults to BKGD/MS on any reset.

**NOTE**

To avoid extra current drain from floating input pins, the reset initialization routine in the application program must either enable on-chip pullup devices or change the direction of unused pins to outputs so the pins do not float.

#### 2.2.5.1 Pin Control Registers

To select drive strength or enable slew rate control or pullup devices, the user writes to the appropriate pin control register located in the high-page register block of the memory map. The pin control registers operate independently of the parallel I/O registers and allow control of a port on an individual pin basis.

##### 2.2.5.1.1 Internal Pullup Enable

An internal pullup device can be enabled for each port pin by setting the corresponding bit in one of the pullup enable registers (PTxPEn). The pullup device is disabled if the pin is configured as an output by the parallel I/O control logic or any shared peripheral function, regardless of the state of the corresponding pullup enable register bit. The pullup device is also disabled if the pin is controlled by an analog function.

The KBI module and IRQ function when enabled for rising edge detection causes an enabled internal pull device to be configured as a pulldown.

### 2.2.5.2 Output Slew Rate Control

Slew rate control can be enabled for each port pin by setting the corresponding bit in one of the slew rate control registers (PTxSEn). When enabled, slew control limits the rate at which an output can transition in order to reduce EMC emissions. Slew rate control has no effect on pins that are configured as inputs.

### 2.2.5.3 Output Drive Strength Select

An output pin can be selected to have high output drive strength by setting the corresponding bit in one of the drive strength select registers (PTxDSn). When high drive is selected, a pin is capable of sourcing and sinking greater current. Even though every I/O pin can be selected as high drive, the user must ensure that the total current source and sink limits for the chip are not exceeded. Drive strength selection is intended to affect the DC behavior of I/O pins. However, the AC behavior is also affected. High drive allows a pin to drive a greater load with the same switching speed as a low drive enabled pin into a smaller load. Because of this, the EMC emissions may be affected by enabling pins as high drive.

**Table 2-1. Pin Sharing Priority**

| Lowest <- Pin Function Priority -> Highest | | | | Reference[1] |
|---|---|---|---|---|
| **Port Pins** | **Alternative Function** | **Alternative Function** | **Alternative Function** | |
| PTA0 | KBI1P0 | TPM1CH0 | ADC1P0[3] | KBI1, ADC1, and TPM1 Chapters |
| PTA1 | KBI1P1 | TPM1CH1 | ADC1P1[3] | KBI1, ADC1, and TPM1 Chapters |
| PTA2 | KBI1P2 | TCLK1 | ADC1P2[3] | KBI1, ADC1, and TPM1 Chapters |
| PTA3 | KBI1P3 | TCLK2 | ADC1P3[3] | KBI1, ADC1, and TPM2 Chapters |
| PTA4 | TPM2CH0O | BKGD/MS | | TPM2 Chapters |
| PTA5[2] | TPM2CH0I | IRQ | RESET | IRQ[4], and TPM2 Chapters |

1 See the module section listed for information on modules that share these pins.

2 Pin does not contain a clamp diode to $V_{DD}$ and must not be driven above $V_{DD}$. The voltage measured on this pin when internal pullup is enabled may be as low as $V_{DD}$ – 0.7 V. The internal gates connected to this pin are pulled to $V_{DD}$.

3 If both of these analog modules are enabled both will have access to the pin.

4 See Section 5.8, “Reset, Interrupt, and System Control Registers and Control Bits,” for information on configuring the IRQ module.

# Chapter 3
# Modes of Operation

## 3.1 Introduction

The operating modes of the MC9S08QD4 series are described in this chapter. Entry into each mode, exit from each mode, and functionality while in each of the modes are described.

## 3.2 Features

- Active background mode for code development
- Wait mode:
  - CPU shuts down to conserve power
  - System clocks running
  - Full voltage regulation maintained
- Stop modes:
  - CPU and bus clocks stopped
  - Stop2 — Partial power down of internal circuits, RAM contents retained
  - Stop3 — All internal circuits powered for fast recovery

## 3.3 Run Mode

This is the normal operating mode for the MC9S08QD4 series. This mode is selected when the BKGD/MS pin is high at the rising edge of reset. In this mode, the CPU executes code from internal memory with execution beginning at the address fetched from memory at 0xFFFE:0xFFFF after reset.

## 3.4 Active Background Mode

The active background mode functions are managed through the background debug controller (BDC) in the HCS08 core. The BDC provides the means for analyzing MCU operation during software development.

Active background mode is entered in any of five ways:

- When the BKGD/MS pin is low at the rising edge of reset
- When a BACKGROUND command is received through the BKGD pin
- When a BGND instruction is executed
- When encountering a BDC breakpoint