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S9S08RN60

S9S08RN60 Series Data Sheet

Supports: S9S08RN60, S9S08RN48 and S9S08RN32

Features

- 8-Bit S08 central processor unit (CPU)
 - Up to 20 MHz bus at 2.7 V to 5.5 V across temperature range of -40 °C to 125 °C
 - Supporting up to 40 interrupt/reset sources
 - Supporting up to four-level nested interrupt
 - On-chip memory
 - Up to 60 KB flash read/program/erase over full operating voltage and temperature
 - Up to 256 byte EEPROM with ECC; 2-byte erase sector; EEPROM program and erase while executing code from flash
 - Up to 4096 byte random-access memory (RAM)
 - Flash and RAM access protection
- Power-saving modes
 - One low-power stop mode; reduced power wait mode
 - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- Clocks
 - Oscillator (XOSC) - loop-controlled Pierce oscillator; crystal or ceramic resonator
 - Internal clock source (ICS) - containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allowing 1% deviation across temperature range of 0 °C to 70 °C and -40 °C to 85 °C, 1.5% deviation across temperature range of -40 °C to 105 °C, and 2% deviation across temperature range of -40 °C to 125 °C; up to 20 MHz
- System protection
 - Watchdog with independent clock source
 - Low-voltage detection with reset or interrupt; selectable trip points
 - Illegal opcode detection with reset
 - Illegal address detection with reset
- Development support
 - Single-wire background debug interface
 - Breakpoint capability to allow three breakpoints setting during in-circuit debugging
 - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes
- Peripherals
 - ACMP - one analog comparator with both positive and negative inputs; separately selectable interrupt on rising and falling comparator output; filtering
 - ADC - 16-channel, 12-bit resolution; 2.5 μs conversion time; data buffers with optional watermark; automatic compare function; internal bandgap reference channel; operation in stop mode; optional hardware trigger
 - CRC - programmable cyclic redundancy check module
 - FTM - three flex timer modulators modules including one 6-channel and two 2-channel ones; 16-bit counter; each channel can be configured for input capture, output compare, edge- or center-aligned PWM mode
 - IIC - One inter-integrated circuit module; up to 400 kbps; multi-master operation; programmable slave address; supporting broadcast mode and 10-bit addressing
 - MTIM - Two modulo timers with 8-bit prescaler and overflow interrupt
 - RTC - 16-bit real timer counter (RTC)
 - SCI - three serial communication interface (SCI/UART) modules optional 13-bit break; full duplex non-return to zero (NRZ); LIN extension support
 - SPI - one 8-bit and one 16-bit serial peripheral interface (SPI) modules; full-duplex or single-wire bidirectional; master or slave mode
 - TSI - supporting up to 16 external electrodes; configurable software or hardware scan trigger; fully support freescale touch sensing software library; capability to wake MCU from stop3 mode

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

- Input/Output
 - Up to 55 GPIOs including one output-only pin
 - Two 8-bit keyboard interrupt modules (KBI)
 - Two true open-drain output pins
 - Eight, ultra-high current sink pins supporting 20 mA source/sink current
- Package options
 - 64-pin LQFP
 - 48-pin LQFP
 - 32-pin LQFP

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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: RN60, RN48 and RN32.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

S 9 S08 RN AA F1 B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
S	Qualification status	<ul style="list-style-type: none"> S = fully qualified, general market flow
9	Memory	<ul style="list-style-type: none"> 9 = flash based
S08	Core	<ul style="list-style-type: none"> S08 = 8-bit CPU
RN	Device family	<ul style="list-style-type: none"> RN
AA	Approximate flash size in KB	<ul style="list-style-type: none"> 60 = 60 KB 48 = 48 KB 32 = 32 KB
F1	Fab and mask set identifier	<ul style="list-style-type: none"> W1
B	Temperature range (°C)	<ul style="list-style-type: none"> M = -40 to 125

Table continues on the next page...

Field	Description	Values
CC	Package designator	<ul style="list-style-type: none"> • LH = 64-pin LQFP • LF = 48-pin LQFP • LC = 32-pin LQFP

2.4 Example

This is an example part number:

S9S08RN60W1MLH

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

- Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

- Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 125°C	-100	+100	mA	

- Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
- Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V _{DD}	Supply voltage	-0.3	5.8	V
I _{DD}	Maximum current into V _{DD}	—	120	mA

Table continues on the next page...

Symbol	Description	Min.	Max.	Unit
V _{DIO}	Digital input voltage (except RESET, EXTAL, XTAL, or true open drain pin PTA2 and PTA3)	-0.3	V _{DD} + 0.3	V
	Digital input voltage (true open drain pin PTA2 and PTA3)	-0.3	6	V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} - 0.3	V _{DD} + 0.3	V

1. All digital I/O pins, except open-drain pin PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 is only clamped to V_{SS}.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	C	Descriptions		Min	Typical ¹	Max	Unit	
—	—	Operating voltage		2.7	—	5.5	V	
V _{OH}	C	Output high voltage	All I/O pins, standard-drive strength	5 V, I _{load} = -5 mA	V _{DD} - 0.8	—	—	V
	C			3 V, I _{load} = -2.5 mA	V _{DD} - 0.8	—	—	V
	C	High current drive pins, high-drive strength ^{2, 2}		5 V, I _{load} = -20 mA	V _{DD} - 0.8	—	—	V
	C			3 V, I _{load} = -10 mA	V _{DD} - 0.8	—	—	V
I _{OHT}	D	Output high current	Max total I _{OH} for all ports	5 V	—	—	-100	mA
				3 V	—	—	-50	
V _{OL}	C	Output low voltage	All I/O pins, standard-drive strength	5 V, I _{load} = 5 mA	—	—	0.8	V
	C			3 V, I _{load} = 2.5 mA	—	—	0.8	V
	C	High current drive pins, high-drive strength ²		5 V, I _{load} = 20 mA	—	—	0.8	V
	C			3 V, I _{load} = 10 mA	—	—	0.8	V

Table continues on the next page...

Table 2. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical ¹	Max	Unit
I _{OLT}	D	Output low current	Max total I _{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	50	
V _{IH}	P	Input high voltage	All digital inputs	V _{DD} >4.5V	0.70 × V _{DD}	—	—	V
	C			V _{DD} >2.7V	0.75 × V _{DD}	—	—	
V _{IL}	P	Input low voltage	All digital inputs	V _{DD} >4.5V	—	—	0.30 × V _{DD}	V
	C			V _{DD} >2.7V	—	—	0.35 × V _{DD}	
V _{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V _{DD}	—	—	mV
I _{IinI}	P	Input leakage current	All input only pins (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{IOZl}	P	Hi-Z (off-state) leakage current	All input/output (per pin)	V _{IN} = V _{DD} or V _{SS}	—	0.1	1	μA
I _{IOZTOTl}	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V _{IN} = V _{DD} or V _{SS}	—	—	2	μA
R _{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R _{PU} ³	P	Pullup resistors	PTA2 and PTA3 pin	—	30.0	—	60.0	kΩ
I _{IC}	D	DC injection current ^{4, 5, 6}	Single pin limit	V _{IN} < V _{SS} , V _{IN} > V _{DD}	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C _{In}	C	Input capacitance, all pins			—	—	7	pF
V _{RAM}	C	RAM retention voltage			—	2.0	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5 support ultra high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}.
5. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current (V_{in} > V_{DD}) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR Specification

Symbol	C	Description	Min	Typ	Max	Unit
V _{POR}	D	POR re-arm voltage ^{1, 2}	1.5	1.75	2.0	V

Table continues on the next page...

Table 3. LVD and POR Specification (continued)

Symbol	C	Description	Min	Typ	Max	Unit		
V _{LVDH}	C	Falling low-voltage detect threshold - high range (LVDV = 1) ³	4.2	4.3	4.4	V		
V _{LWV1H}	C	Falling low-voltage warning threshold - high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V	
V _{LWV2H}	C			Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V _{LWV3H}	C				Level 3 falling (LVWV = 10)	4.6	4.6	4.7
V _{LWV4H}	C			Level 4 falling (LVWV = 11)		4.7	4.7	4.8
V _{HYSH}	C	High range low-voltage detect/warning hysteresis	—	100	—	mV		
V _{LVDL}	C	Falling low-voltage detect threshold - low range (LVDV = 0)	2.56	2.61	2.66	V		
V _{LVDW1L}	C	Falling low-voltage warning threshold - low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V	
V _{LVDW2L}	C			Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V _{LVDW3L}	C				Level 3 falling (LVWV = 10)	2.82	2.9	2.98
V _{LVDW4L}	C			Level 4 falling (LVWV = 11)		2.92	3.0	3.08
V _{HYSDL}	C	Low range low-voltage detect hysteresis	—	40	—	mV		
V _{HYSWL}	C	Low range low-voltage warning hysteresis	—	80	—	mV		
V _{BG}	P	Buffered bandgap output ⁴	1.14	1.16	1.18	V		

1. Maximum is highest voltage that POR is guaranteed.
2. POR ramp time must be longer than 20us/V to get a stable startup.
3. Rising thresholds are falling threshold + hysteresis.
4. Voltage factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 5\text{ V}$)

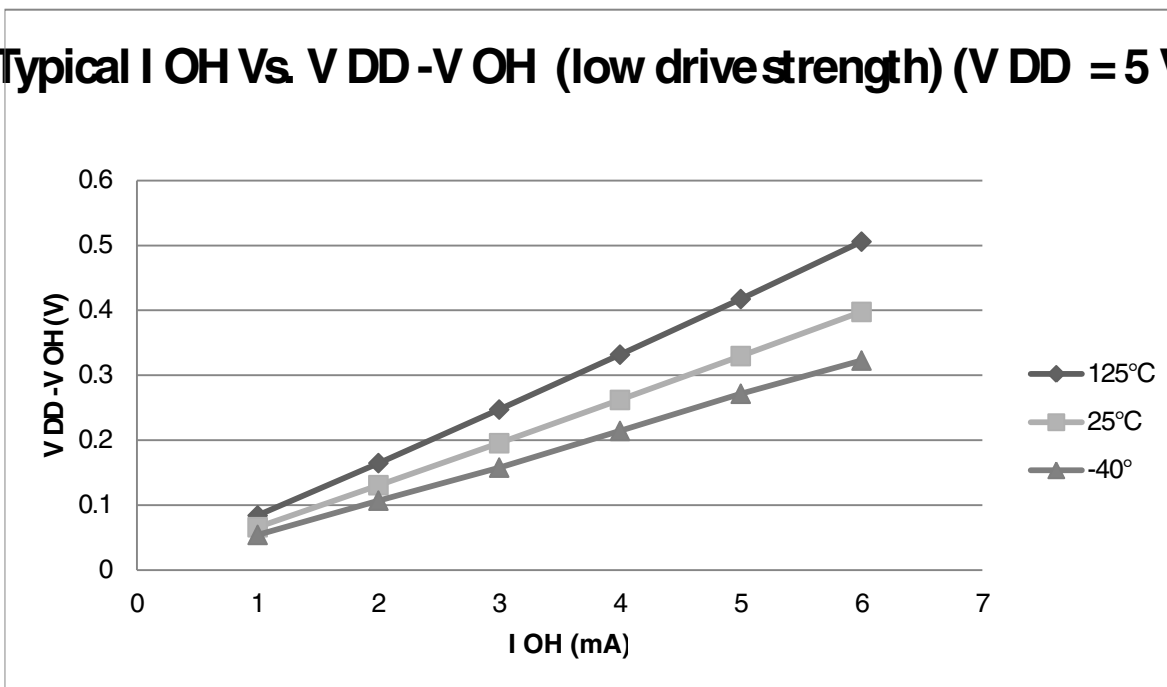


Figure 1. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (low drive strength) ($V_{DD} = 3\text{ V}$)

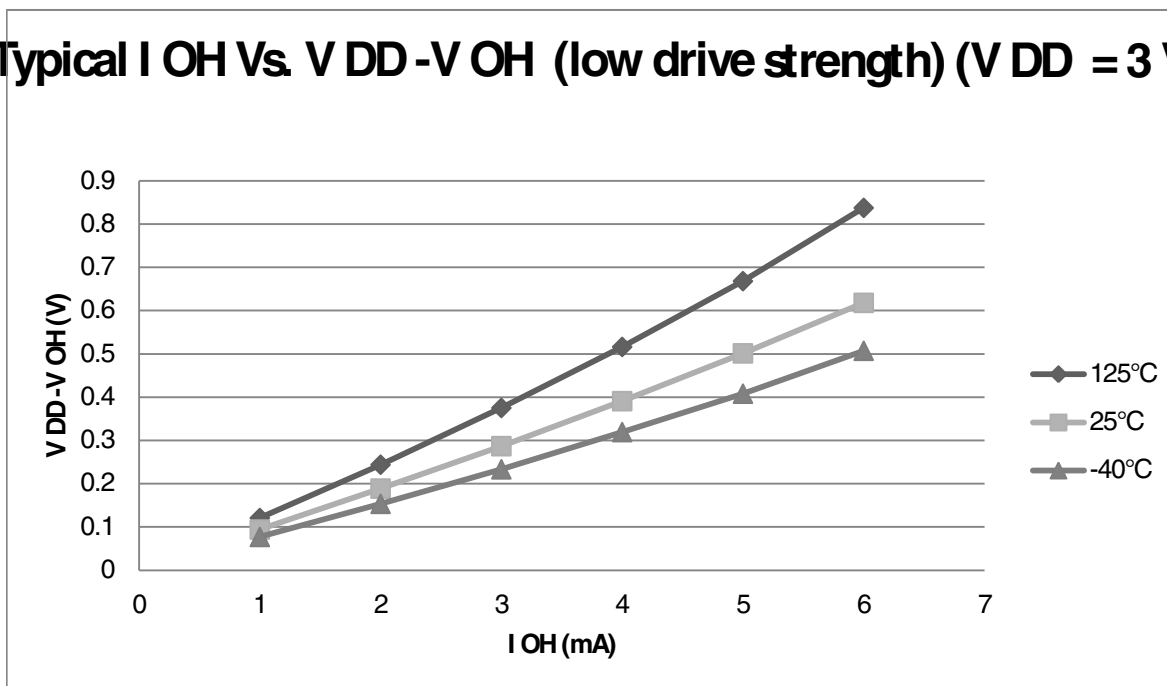


Figure 2. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (standard drive strength) ($V_{DD} = 3\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 5\text{ V}$)

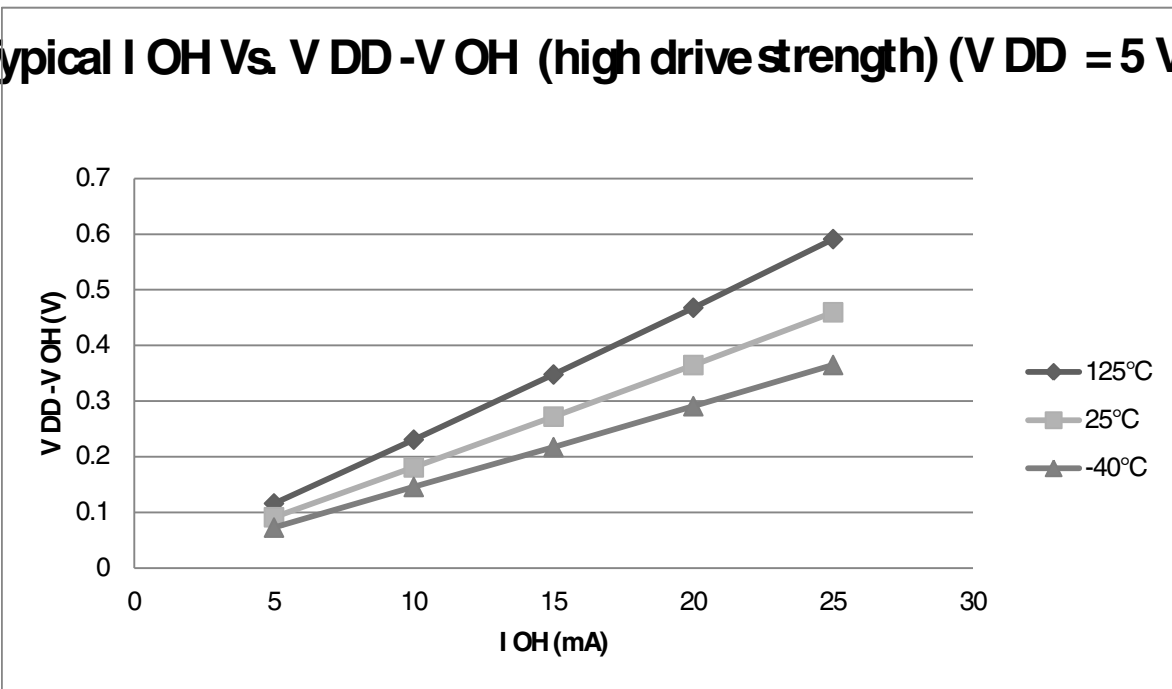


Figure 3. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 5\text{ V}$)

Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 3\text{ V}$)

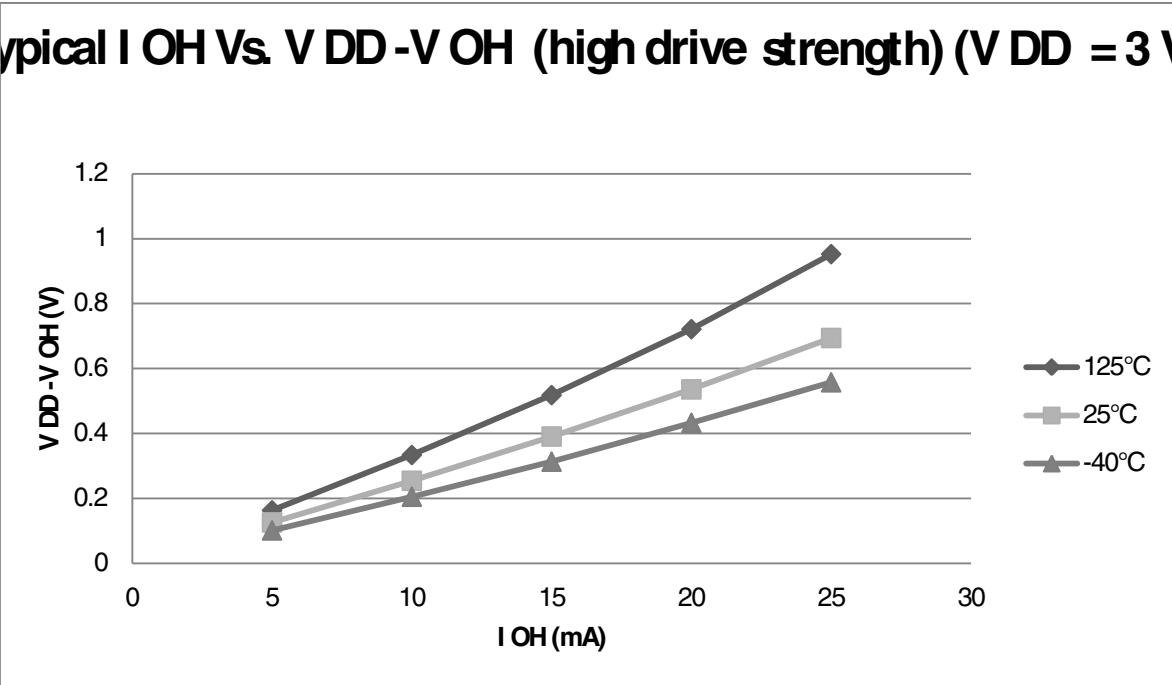


Figure 4. Typical I_{OH} Vs. $V_{DD}-V_{OH}$ (high drive strength) ($V_{DD} = 3\text{ V}$)

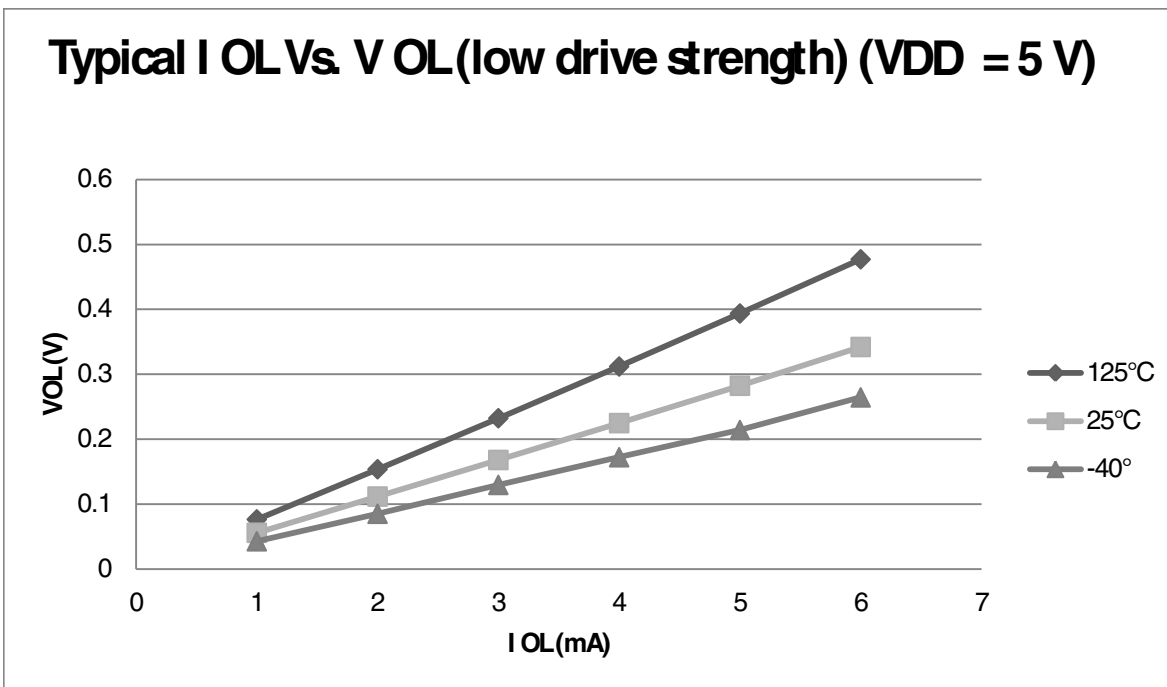


Figure 5. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 5\text{ V}$)

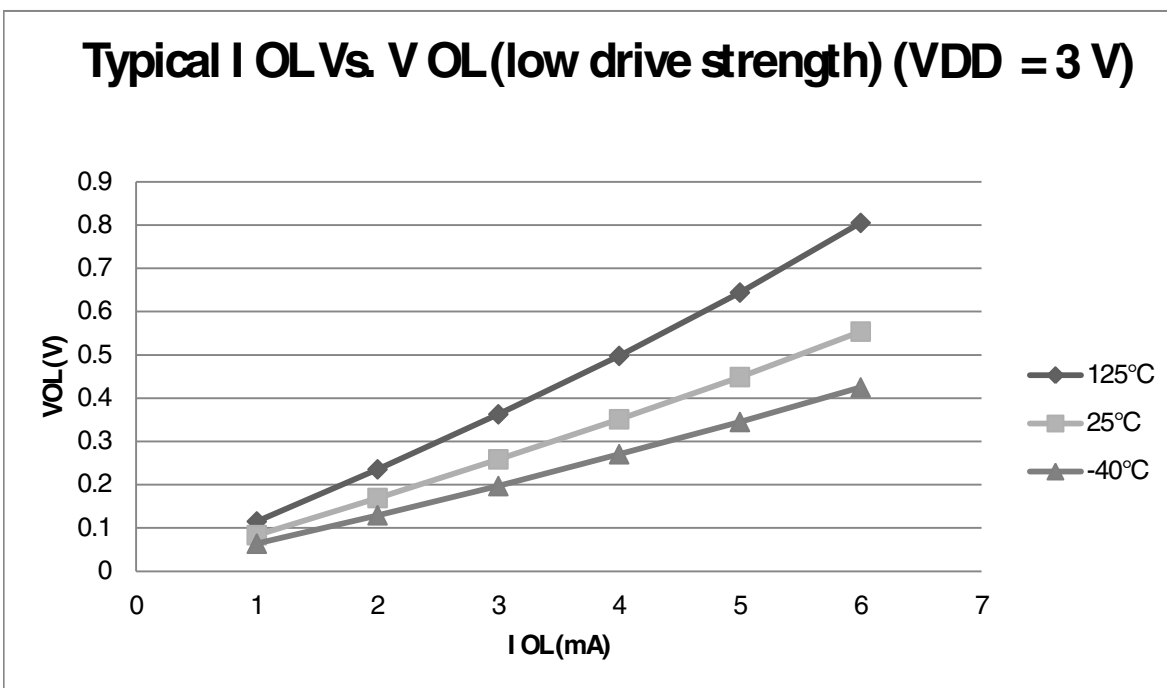


Figure 6. Typical I_{OL} Vs. V_{OL} (standard drive strength) ($V_{DD} = 3\text{ V}$)

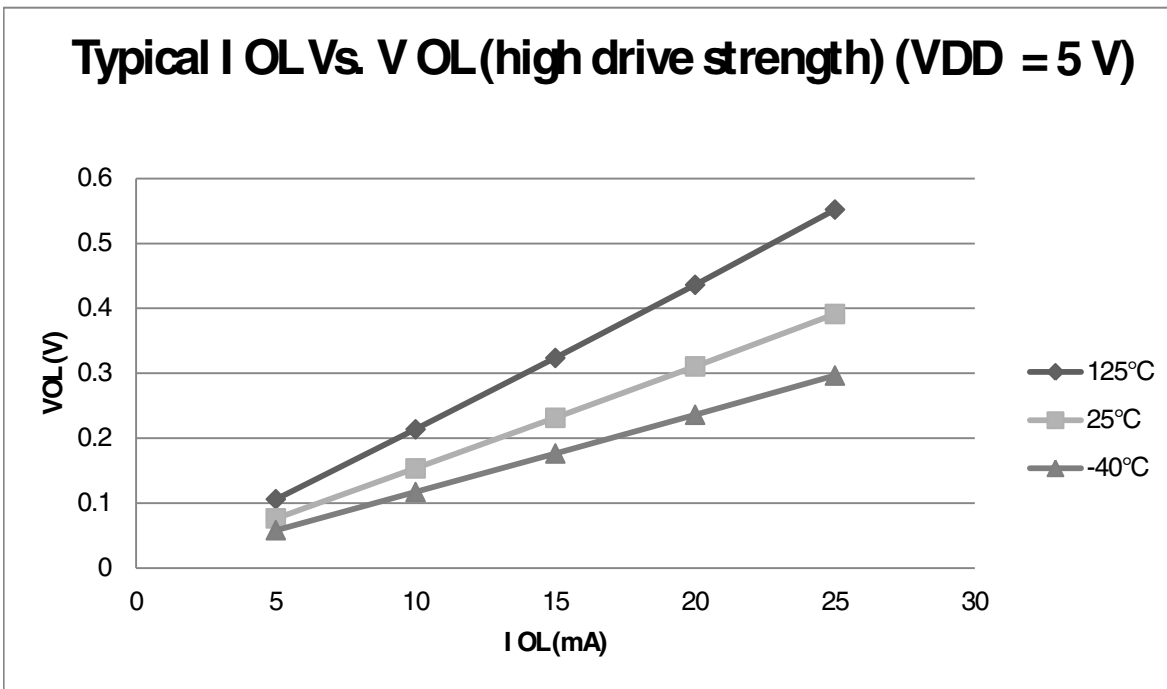


Figure 7. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 5\text{ V}$)

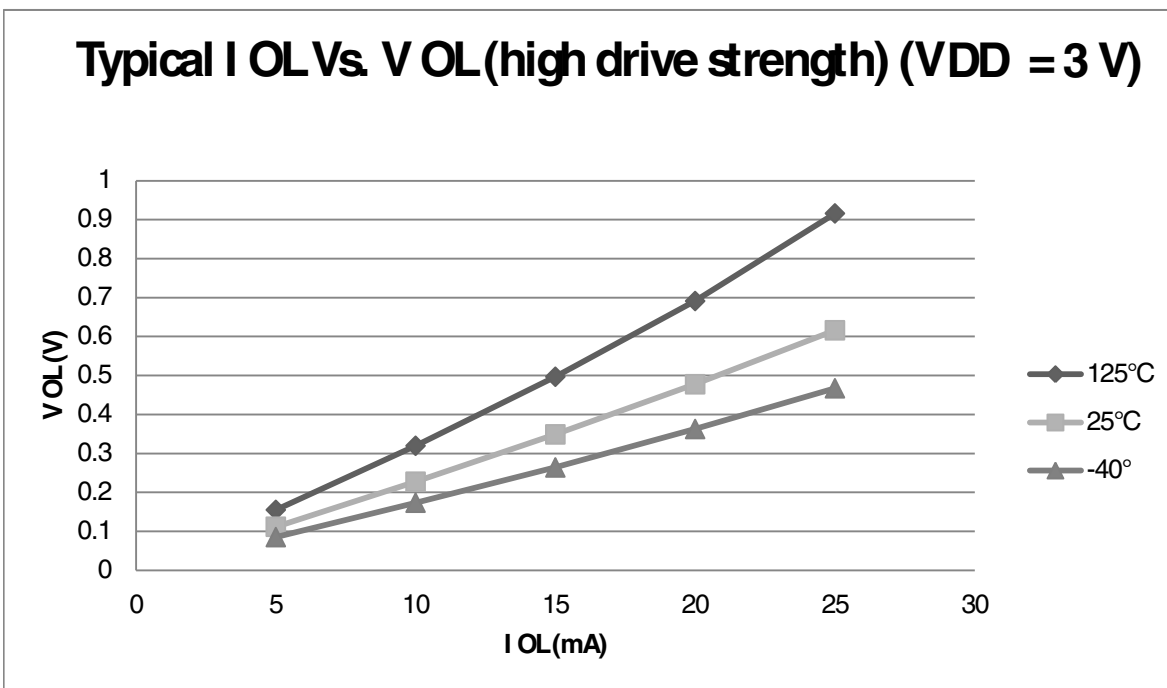


Figure 8. Typical I_{OL} Vs. V_{OL} (high drive strength) ($V_{DD} = 3\text{ V}$)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	12.6	—	mA	-40 to 125 °C
	C			10 MHz		7.2	—		
	C			1 MHz		2.4	—		
	C			20 MHz	3	9.6	—		
	C			10 MHz		6.1	—		
	C			1 MHz		2.1	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	10.5	—	mA	-40 to 125 °C
	C			10 MHz		6.2	—		
	C			1 MHz		2.3	—		
	C			20 MHz	3	7.4	—		
	C			10 MHz		5.0	—		
	C			1 MHz		2.0	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	12.1	14.8	mA	-40 to 125 °C
	C			10 MHz		6.5	—		
	C			1 MHz		1.8	—		
	P			20 MHz	3	9.1	11.8		
	C			10 MHz		5.5	—		
	C			1 MHz		1.5	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	9.8	12.3	mA	-40 to 125 °C
	C			10 MHz		5.4	—		
	C			1 MHz		1.6	—		
	P			20 MHz	3	6.9	9.2		
	C			10 MHz		4.4	—		
	C			1 MHz		1.4	—		
5	C	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	7.8	—	mA	-40 to 125 °C
	C			10 MHz		4.5	—		
	C			1 MHz		1.3	—		
	C			20 MHz	3	5.1	—		
	C			10 MHz		3.5	—		
	C			1 MHz		1.2	—		
6	C	Stop3 mode supply current no clocks active (except 1 kHz LPO clock) ^{2,3}	S3I _{DD}	—	5	3.8	—	μA	-40 to 125 °C
	C			—	3	3	—		-40 to 125 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
7	C	ADC adder to stop3	—	—	5	44	—	μA	-40 to 125 °C
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	40	—		
8	C	TSI adder to stop3 ⁴	—	—	5	111	—	μA	-40 to 125 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	110	—		
9	C	LVD adder to stop3 ⁵	—	—	5	130	—	μA	-40 to 125 °C
	C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
3. ACMP adder cause <1 μA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer to [TSI electrical specifications](#).
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

5.2 Switching specifications

5.2.1 Control timing

Table 5. Control timing

Num	C	Rating	Symbol	Min	Typical ¹	Max	Unit
1	P	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	DC	—	20	MHz
2	P	Internal low power oscillator frequency	f_{LPO}	0.67	1.0	1.25	KHz
3	D	External reset pulse width ^{2, 2}	t_{extrst}	$1.5 \times t_{Self_reset}$	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$34 \times t_{cyc}$	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³	t_{MSH}	100	—	—	ns
7	D	Keyboard interrupt pulse width	Asynchronous path ²	t_{LIH}	100	—	ns
	D		Synchronous path	t_{HIL}	$1.5 \times t_{cyc}$	—	ns
8	C	Port rise and fall time - Normal drive strength (HDRVE_PTXX = 0) (load = 50 pF) ^{4, 4}	—	t_{Rise}	—	10.2	ns
	C		—	t_{Fall}	—	9.5	ns
	C	Port rise and fall time - Extreme high drive strength (HDRVE_PTXX = 1) (load = 50 pF) ⁴	—	t_{Rise}	—	5.4	ns
	C		—	t_{Fall}	—	4.6	ns

1. Typical values are based on characterization data at $V_{DD} = 5.0\text{ V}$, $25\text{ }^\circ\text{C}$ unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$.

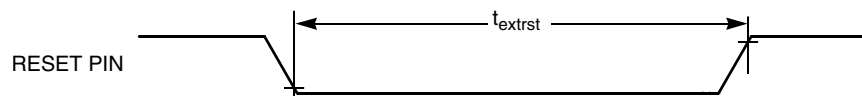


Figure 9. Reset timing

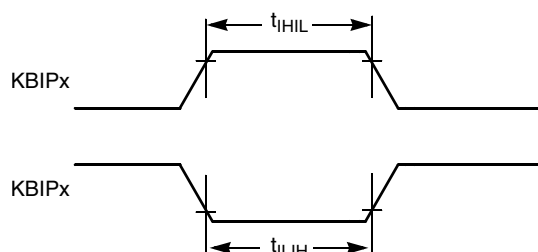


Figure 10. KBIPx timing

5.2.2 Debug trace timing specifications

Table 6. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

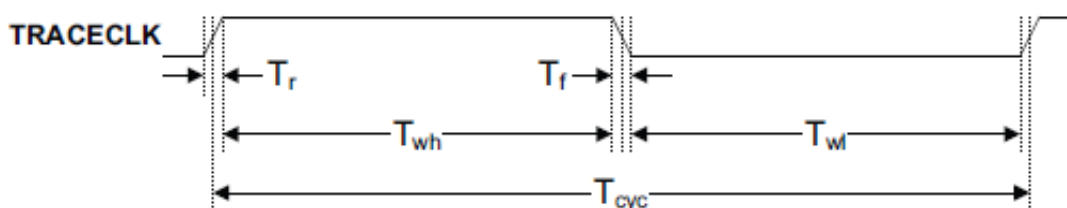


Figure 11. TRACE_CLKOUT specifications

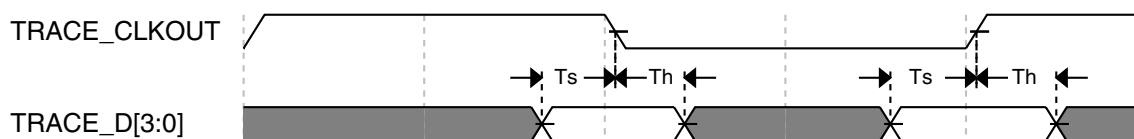


Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 7. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz

Table continues on the next page...

Table 7. FTM input timing (continued)

No.	C	Function	Symbol	Min	Max	Unit
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

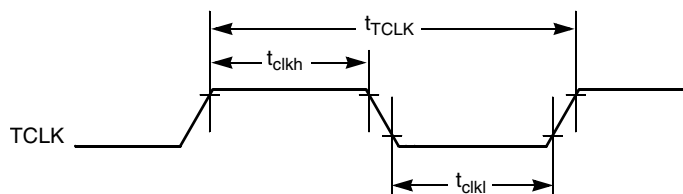


Figure 13. Timer external clock

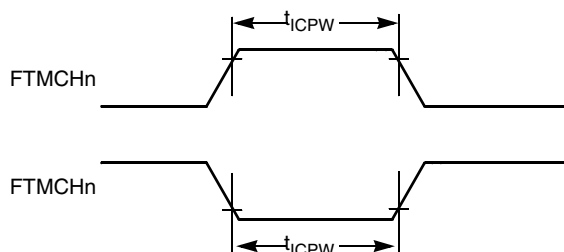


Figure 14. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 8. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	T_L to T_H -40 to 125	$^{\circ}\text{C}$
Junction temperature range	T_J	-40 to 135	$^{\circ}\text{C}$
Thermal resistance single-layer board			
64-pin LQFP	θ_{JA}	71	$^{\circ}\text{C}/\text{W}$
48-pin LQFP	θ_{JA}	81	$^{\circ}\text{C}/\text{W}$
32-pin LQFP	θ_{JA}	86	$^{\circ}\text{C}/\text{W}$
Thermal resistance four-layer board			
64-pin LQFP	θ_{JA}	53	$^{\circ}\text{C}/\text{W}$
48-pin LQFP	θ_{JA}	57	$^{\circ}\text{C}/\text{W}$
32-pin LQFP	θ_{JA}	57	$^{\circ}\text{C}/\text{W}$

The average chip-junction temperature (T_J) in $^{\circ}\text{C}$ can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, $^{\circ}\text{C}$

θ_{JA} = Package thermal resistance, junction-to-ambient, $^{\circ}\text{C}/\text{W}$

$$P_D = P_{\text{int}} + P_{\text{I/O}}$$

P_{int} = $I_{\text{DD}} \times V_{\text{DD}}$, Watts - chip internal power

$P_{\text{I/O}}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{\text{I/O}} \ll P_{\text{int}}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{\text{I/O}}$ is neglected) is:

$$P_D = K \div (T_J + 273 \text{ }^{\circ}\text{C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ }^{\circ}\text{C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A .

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)

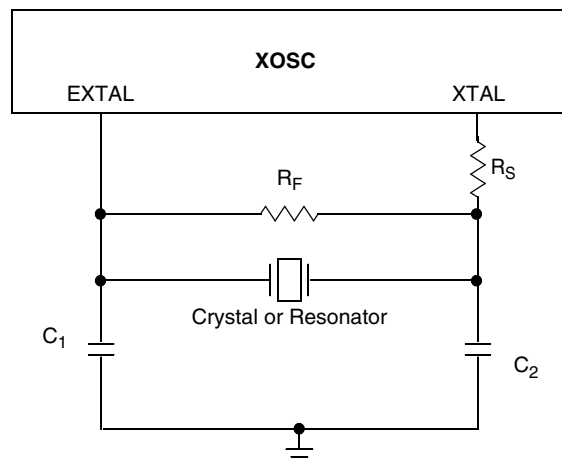
Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	32	—	40	kHz
	C		High range (RANGE = 1) FEE or FBE mode ^{2, 2}	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note ³			
3	D	Feedback resistor	Low Frequency, Low-Power Mode ^{4, 4}	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 39.0625 kHz crystal; High range = 20 MHz crystal ^{5, 5, 6}	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode ²	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	39.0625	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz

Table continues on the next page...

**Table 9. XOSC and ICS specifications (temperature range = -40 to 125 °C ambient)
(continued)**

Num	C	Characteristic	Symbol	Min	Typical ¹	Max	Unit		
11	P	Total deviation of DCO output from trimmed frequency ⁵	$\Delta f_{\text{dco_t}}$	—	—	±2.0			
	C					Over full voltage range and temperature range of -40 to 105 °C		±1.5	% f_{dco}
	C					Over fixed voltage and temperature range of 0 to 70 °C		±1.0	
12	C	FLL acquisition time ^{5, 7}	t_{Acquire}	—	—	2	ms		
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) ⁸	C_{Jitter}	—	0.02	0.2	% f_{dco}		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.


Figure 15. Typical crystal or resonator circuit

6.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min ¹	Typical ²	Max ³	Unit ⁴
D	Supply voltage for program/erase -40 °C to 125 °C	V _{prog/erase}	2.7	—	5.5	V
D	Supply voltage for read operation	V _{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f _{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f _{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t _{VFYALL}	—	—	17338	t _{cyc}
D	Erase Verify Flash Block	t _{RD1BLK}	—	—	16913	t _{cyc}
D	Erase Verify EEPROM Block	t _{RD1BLK}	—	—	810	t _{cyc}
D	Erase Verify Flash Section	t _{RD1SEC}	—	—	484	t _{cyc}
D	Erase Verify EEPROM Section	t _{DRD1SEC}	—	—	555	t _{cyc}
D	Read Once	t _{RDONCE}	—	—	450	t _{cyc}
D	Program Flash (2 word)	t _{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t _{PGM4}	0.20	0.21	0.46	ms
D	Program Once	t _{PGMONCE}	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t _{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t _{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t _{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t _{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t _{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t _{ERSBLK}	95.98	100.75	101.44	ms
D	Erase Flash Sector	t _{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t _{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t _{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t _{VFYKEY}	—	—	464	t _{cyc}
D	Set User Margin Level	t _{MLOADU}	—	—	407	t _{cyc}
C	FLASH Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance T _L to T _H = -40 °C to 125 °C	n _{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T _{Javg} = 85°C after up to 10,000 program/erase cycles	t _{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. t_{cyc} = 1 / f_{NVMBUS}

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

6.3 Analog

6.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD}-V_{DDAD}$)	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS}-V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	k Ω	—
Analog source resistance	12-bit mode	R_{AS}	—	—	2	k Ω	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
10-bit mode	—	—	5	k Ω	External to MCU		
• $f_{ADCK} > 4$ MHz	—	—	10				
• $f_{ADCK} < 4$ MHz	—	—	10				
8-bit mode (all valid f_{ADCK})	—	—	10				
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

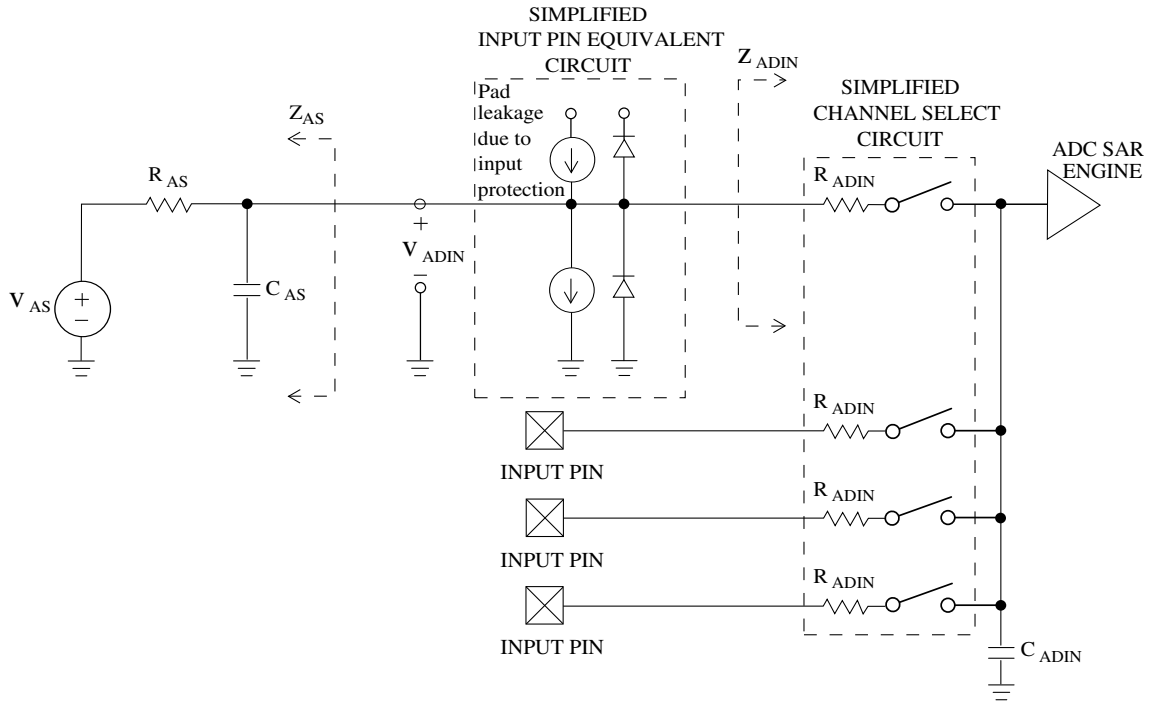


Figure 16. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	μA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	μA

Table continues on the next page...

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ^{2, 2}	12-bit mode	T	E_{TUE}	—	± 5.0	—	LSB ^{3, 3}
	10-bit mode	P		—	± 1.5	± 2.0	
	8-bit mode	P		—	± 0.7	± 1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	± 1.0	—	LSB ³
	10-bit mode ^{4, 4}	P		—	± 0.25	± 0.5	
	8-bit mode ⁴	P		—	± 0.15	± 0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	± 1.0	—	LSB ³
	10-bit mode	T		—	± 0.3	± 0.5	
	8-bit mode	T		—	± 0.15	± 0.25	
Zero-scale error ^{5, 5}	12-bit mode	C	E_{ZS}	—	± 2.0	—	LSB ³
	10-bit mode	P		—	± 0.25	± 1.0	
	8-bit mode	P		—	± 0.65	± 1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	± 2.5	—	LSB ³
	10-bit mode	T		—	± 0.5	± 1.0	
	8-bit mode	T		—	± 0.5	± 1.0	
Quantization error	≤ 12 bit modes	D	E_Q	—	—	± 0.5	LSB ³
Input leakage error ⁷	all modes	D	E_{IL}	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{in} = leakage current (refer to DC characteristics)