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Freescale Semiconductor, Inc.
Data Sheet

Document Number: MC9S08SG32
Rev. 9, 04/2015

MC9S08SG32 with Addenda Covers: MC9S08SG32 and MC9S08SG16

Rev. 9 of the MC9S08SG32 data sheet (covering MC9S08SG32 and MC9S08SG16) has three parts:

- The revision 2 addendum to revision 8.1 of the data sheet, immediately following this cover page.
- The revision 1 addendum to revision 8 of the data sheet.
- Revision 8 of the data sheet, following the addendums. The changes described in the addendums have not been implemented in the specified pages.

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08SG32AD
Rev. 2, 04/2015

Addendum to Rev. 8.1 of the MC9S08SG32 Covers: MC9S08SG32 and MC9S08SG16

This addendum identifies changes to Rev. 8.1 of the MC9S08SG32 data sheet (covering MC9S08SG32 and MC9S08SG16). The changes described in this addendum have not been implemented in the specified pages.

1 Update to the "Nonvolatile Register Summary" table for NVFTRIM and NVOPT

Location:	Table 4-4. Nonvolatile Register Summary, Page 47

For the NVFTRIM and NVOPT registers in Table 4-4, "Nonvolatile Register Summary," all reserved bits should be marked as "—" (not "0").

2 Update to the "Instruction Set Summary" table for BRA and BRN

Location:	Table 7-2. Instruction Set Summary (Sheet 3 of 9), Page 106

In Table 7-2, "Instruction Set Summary," remove "(if I = 1)" from the BRA instruction and remove "(if I = 0)" from the BRN instruction. The BRA and BRN instructions do not depend on the I bit.

MC9S08SG32 DataSheet Addendum

by: Microcontroller Solutions Group

This is the MC9S08SG32 DataSheet set consisting of the following files:

- MC9S08SG32 DataSheet Addendum, Rev 1
- MC9S08SG32 DataSheet, Rev 8

Freescale Semiconductor
Addendum

MC9S08SG32AD
Rev. 1, 02/2012

MC9S08SG32 Data Sheet Addendum

by: Microcontroller Solutions Group

This errata document describes updates to the *MC9S08SG32 Data Sheet*, order number MC9S08SG32. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com for the latest updates.

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1 Addendum for Revision 8.0

Table 1. MC9S08SG32 Rev. 1 Addendum

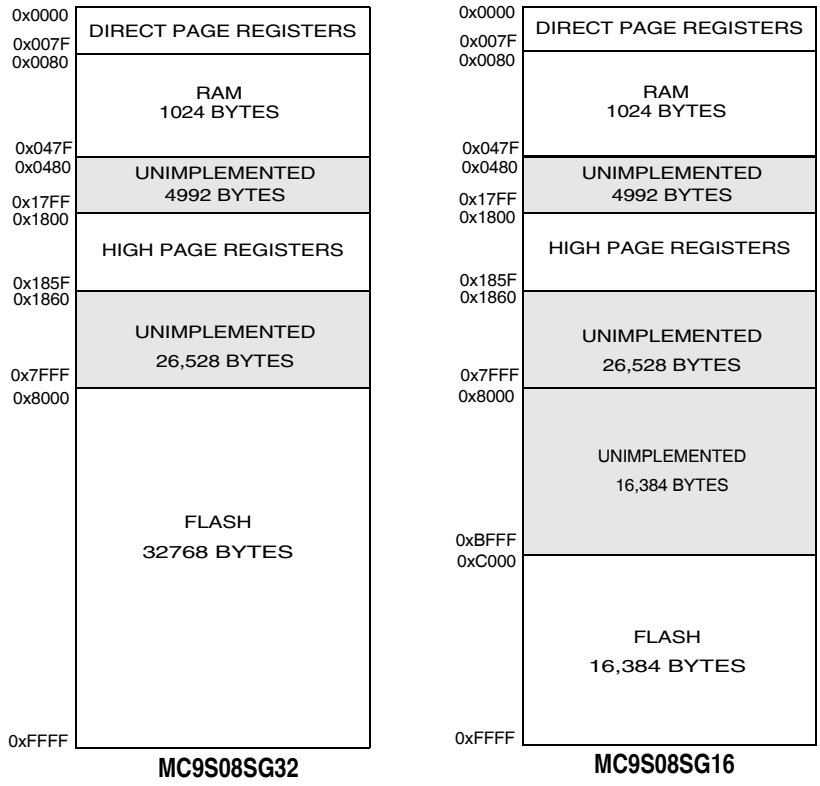
Location	Description
Chapter “Memory”/ Section “MC9S08SG32 Series Memory Map”/Figure 4-1. MC9S08SG32/MC9S08SG16 Memory Map/Page 39	In Figure 4-1. MC9S08SG32/MC9S08SG16 Memory Map for device MC9S08SG16 change the value of “Unimplemented Bytes” from “26,538” to “26,528”. 

Table 1. MC9S08SG32 Rev. 1 Addendum

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Chapter “Electrical Characteristics”/Section “Thermal Characteristics”/Table A-3. Thermal Characteristics/Page 293</td><td>Update Table A-3. Thermal Characteristics as follows:
• —Change the value for row “Thermal resistance,Single-layer board/28-pin TSSOP/Airflow @200ft/min.” from 71 to 72 C/W
—Change the value for 16-pin TSSOP/Thermalresistance
1.Single layer board / Airflow @ 200ft/min. from 108 to 113 C/W.
2.Four layer board / Airflow @ 200ft/min. from 78 to 84 C/W.
• Update parameter 4 of Table “A-3.Thermal Characteristics” .

<table>
<tr><th rowspan="2">#</th><th rowspan="2">C</th><th rowspan="2">Rating</th><th rowspan="2">Symbol</th><th rowspan="2">Value</th><th rowspan="2">Unit</th><th colspan="2">Temp Rated</th></tr>
<tr><th>Standard</th><th>AEC Grade 0</th></tr>
<tr><td>1</td><td>—</td><td colspan="6">Operating temperature range (packaged)</td></tr>
<tr><td></td><td></td><td>Temperature Code W</td><td rowspan="5">T_A</td><td>–40 to 150</td><td rowspan="5">°C</td><td>—</td><td>♦</td></tr>
<tr><td></td><td></td><td>Temperature Code J</td><td>–40 to 140</td><td>—</td><td>♦</td></tr>
<tr><td></td><td></td><td>Temperature Code M</td><td>–40 to 125</td><td>♦</td><td>—</td></tr>
<tr><td></td><td></td><td>Temperature Code V</td><td>–40 to 105</td><td>♦</td><td>—</td></tr>
<tr><td></td><td></td><td>Temperature Code C</td><td>–40 to 85</td><td>♦</td><td>—</td></tr>
<tr><td>2</td><td>D</td><td colspan="6">Thermal resistance, Single-layer board</td></tr>
<tr><td></td><td></td><td></td><td></td><td>Airflow @200 ft/min</td><td>Natural Convection</td><td></td><td></td></tr>
<tr><td></td><td></td><td>28-pin TSSOP</td><td rowspan="3">θ_{JA}</td><td>72</td><td>91</td><td rowspan="3">°C/W</td><td>♦</td><td>♦</td></tr>
<tr><td></td><td></td><td>20-pin TSSOP</td><td>94</td><td>114</td><td>♦</td><td>—</td></tr>
<tr><td></td><td></td><td>16-pin TSSOP</td><td>113</td><td>133</td><td>♦</td><td>♦</td></tr>
<tr><td>3</td><td>D</td><td colspan="6">Thermal resistance, Four-layer board</td></tr>
<tr><td></td><td></td><td></td><td></td><td>Airflow @200 ft/min</td><td>Natural Convection</td><td></td><td></td></tr>
<tr><td></td><td></td><td>28-pin TSSOP</td><td rowspan="3">θ_{JA}</td><td>51</td><td>58</td><td rowspan="3">°C/W</td><td>♦</td><td>♦</td></tr>
<tr><td></td><td></td><td>20-pin TSSOP</td><td>68</td><td>75</td><td>♦</td><td>—</td></tr>
<tr><td></td><td></td><td>16-pin TSSOP</td><td>84</td><td>92</td><td>♦</td><td>♦</td></tr>
<tr><td>4</td><td>D</td><td colspan="6">Maximum junction temperature</td></tr>
<tr><td></td><td></td><td>Temperature Code W</td><td rowspan="5">T_J</td><td>155</td><td rowspan="5">°C</td><td>—</td><td>♦</td></tr>
<tr><td></td><td></td><td>Temperature Code J</td><td>150</td><td>—</td><td>♦</td></tr>
<tr><td></td><td></td><td>Temperature Code M</td><td>135</td><td>♦</td><td>—</td></tr>
<tr><td></td><td></td><td>Temperature Code V</td><td>115</td><td>♦</td><td>—</td></tr>
<tr><td></td><td></td><td>Temperature Code C</td><td>95</td><td>♦</td><td>—</td></tr>
</table>
</td></tr>
<tr><td>Chapter “Electrical Characteristics”/Section “DC Characteristics”/Table A-6. DC Characteristics/Page 298</td><td>In the Table “DC Characteristics” add note 11 and 12 for parameter #18.
Note 11: Device functionality is guaranteed between the LVD threshold VLVD0 and VDD Min. When VDD is below the minimum operating voltage (VDD Min), the analog parameters for the IO pins, ACMP and ADC, are not guaranteed to meet data sheet performance parameters.
Note 12: In addition to LVD, it is recommended to also use the LVW feature. LVW can trigger an interrupt and be used as an indicator to warn that the VDD is dropping,so that the software can take actions accordingly before the VDD drops below VDD Min.</td></tr>
</table>

Table 1. MC9S08SG32 Rev. 1 Addendum

Location	Description
Chapter “Electrical Characteristics”/Section “Flash Specifications”/Table “A-16. Flash Characteristics”/Page 323	In Table A-16 Flash Characteristics/row 9/column "Characteristic", change the temperature parameter names as follows: Standard: -40°C to +125°C HT: -40°C to +150°C T = 25°C

2 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History Table

Rev. Number	Substantive Changes	Date of Release
1.0	• Initial release. Changes done in Chapter “Electrical Characteristics”.	02/2012

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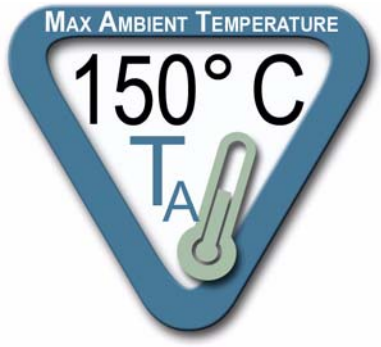
MC9S08SG32AD
Rev. 1
02/2012

MC9S08SG32
MC9S08SG16
Data Sheet

Now Includes High-Temperature (up to 150 °C) Devices!



HCS08
Microcontrollers

MC9S08SG32
Rev. 8
5/2010

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MC9S08SG32 Series Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- 36-MHz HCS08 CPU for temperatures greater than 125 °C
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- FLASH read/program/erase over full operating voltage and temperature from –40 up to 150 °C
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and FLASH contents

Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time counter for use in run, wait, and stop

Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and:
  - 1.5% deviation over temperature –40 to 125 °C
  - 3% deviation for temperature > 125 °C
- ICS supports bus frequencies from 2 MHz to 20 MHz

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect

Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip, in-circuit emulation (ICE) debug module containing two comparators and 9 trigger modes. Eight-deep FIFO for storing change-of-flow address and event-only data. Debug module supports both tag and force breakpoints

Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 µs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel; runs in stop3
- **ACMP** — Analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be optionally routed to TPM module; runs in stop3
- **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
- **MTIM** — 8-bit modulo counter with 8-bit prescaler and overflow interrupt
- **TPMx** — Two 2-channel timer pwm modules (TPM1, TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components, runs in all MCU modes

Input/Output

- 22 general purpose I/O pins (GPIOs)
- 8 interrupt pins with selectable polarity
- Ganged output option for PTB[5:2] and PTC[3:0]; allows single write to change state of multiple pins
- Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins

Package Options

- 28-TSSOP, 20-TSSOP, 16-TSSOP (20-pin package options not available on high-temperature rated devices).

MC9S08SG32 Data Sheet

Covers MC9S08SG32
MC9S08SG16

MC9S08SG32
Rev. 8
5/2010

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Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
1	6/2007	Updated the TPM module, incorporated minor revisions for the T_j, PTxSE slew rate, FPROT and Appendix B packaging information. -SAMPLES DRAFT-
2	10/2007	Qualify Draft includes updates to TPM module and the Electricals appendix. Also, revised the order numbering information.
3	5/2008	Updated some electricals and made some minor grammatical/formatting revisions. Corrected the SPI block module version. Removed incorrect ADC temperature sensor value from the Features section. Updated the package information with a special mask set identifier.
4	5/2008	Added the EMC Radiated Emissions data. Removed the Susceptibility Data. Updated the Corporate addresses on the back cover.
5	03/2009	Added the High Temperature Device Specifications and updated the charts.
6	04/2009	Updated ADC characteristics for Temp Sensor Slope to be a range of 25 C–150 Çadded Control Timing table row 2 to separate standard characteristics from the AEC Grade 0 characteristics, and included the text, “AEC Grade 0” to the text of footnote 3 for Table B-1 Device Numbering System. Added notes to the ADC chapter specifying that, for this device, there are only 16 analog input pins and consequently no APCTL3 register. Updated the Literature Request information on the back cover.
7	10/2009	Revised Table A-6 DC Characteristics, Row 24 Bandgap Voltage Reference for AEC Grade 0 from 1.21V to 1.22 V. Removed AEC Grade 0 (red diamond) from the Table A-9 ICS Frequency Specifications, Row 9 Total deviation of trimmed DCO output frequency over voltage and temperature so that it is not listed for AEC Grade 0.

Revision Number	Revision Date	Description of Changes
8	5/2010	• In the A.9 ICS Characteristic table, changed row 9 parameter classification from a D to a P to indicate that these parameters are guaranteed during production testing on each individual device. • In the A.16 Flash Charateristic table, added the AEC temperature range to row 9. • Revised Figure 2-1 so that the RESET pin shows the overbar.

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