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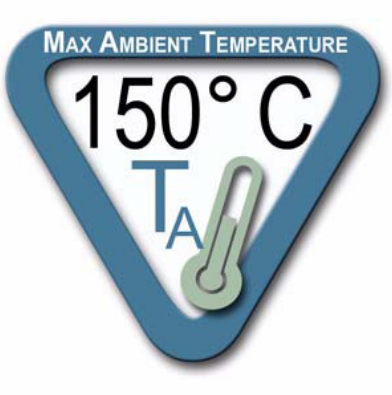
MC9S08SG8
MC9S08SG4

Data Sheet

Now Includes High-Temperature (up to 150 °C) Devices!



HCS08
Microcontrollers

MC9S08SG8
Rev. 8
1/2014

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semiconductor

MC9S08SG8 Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40 MHz HCS08 CPU (central processor unit)
- 36 MHz HCS08 CPU for temperatures greater than 125 °C
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- Flash read/program/erase over full operating voltage and temperature
- Random-access memory (RAM)

Power-Saving Modes

- Two very low power stop modes
- Reduced power wait mode
- Very low power real time interrupt for use in run, wait, and stop

Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16MHz
- Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 1.5% deviation over temperature –40 to 125 °C or 3% deviation for temperature > 125 °C and voltage; supports bus frequencies from 2 MHz to 20MHz.

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH block protect

Development Support

- Single-wire background debug interface
- Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
- On-chip, in-circuit emulation (ICE) debug module containing two comparators and nine trigger modes. Eight deep FIFO for storing change-of-flow address and event-only data. Debug module supports both tag and force breakpoints.

Peripherals

- **ADC** — 12-channel, 10-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel; runs in stop3
- **ACMP** — Analog comparator with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can be optionally routed to TPM module; runs in stop3
- **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- **SPI** — Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; Master or Slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10-bit addressing
- **MTIM** — 8-bit modulo counter with 8-bit prescaler and overflow interrupt
- **TPMx** — Two 2-channel timer pwm modules (TPM1, TPM2); Selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components, runs in all MCU modes

Input/Output

- 16 general purpose I/O pins (GPIOs)
- 8 interrupt pins with selectable polarity
- Ganged output option for PTB[5:2] and PTC[3:0]; allows single write to change state of multiple pins
- Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.

Package Options

- 20-TSSOP (not available on high-temperature rated devices)
- 16-TSSOP
- 8-SOIC (not available on high-temperature rated devices)

MC9S08SG8 Data Sheet

Covers MC9S08SG8
MC9S08SG4

MC9S08SG8
Rev. 8
1/2014

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
0	15 Dec 2006	Initial alpha customer release version; Preliminary
1	June 2007	Samples Draft. Updated book with the latest TPM v3 module. Includes some minor edits to the IIC module to update the Module Quick Start. Fixed the SOPT1 bits 1 and 0 to be RESERVED for both READ and WRITE. Changed all the Reset states of the Slew Rate Enable Registers (PTASE, PTBSE, and PTCSE) bits from 1 to 0 due to silicon functional change.
2	11/2007	Market Launch. Updated the Electricals and Device Numbering scheme information.
3	12/2007	• Fixed typos: Chapter 7 heading corrected version to v2, and Figure 16-1. title corrected to read ...”TPM Modules Highlighted.” • Table A-3. Thermal Characteristics row 1, V and M entries were transposed. V now refers to value -40 to 105°C and M now refers to value -40 to 125°C. Added row 2, parameter classification of “D” and row 4 symbol of ”θ_{JA}.” • Table A-6. DC Characteristics, row 8 Input Hysteresis, corrected units from mV to V.
4	3/2008	• SPI block corrected to be version 3 of the module. • Temperature Sensor values corrected to reflect the ADC 5V in Section 9.1.4 Temperature Sensor and Table A-12. ADC Characteristics. • Provided Maximum juncture temperature for C, V, and M Temperature ranges. • Corrected Table A-6, row 10 separated to two pins: PTB6/SDA/XTAL, $\overline{\text{RESET}}$. • Corrected block diagrams User Flash and User RAM listing typos to be SG8 and SG4 instead of SH8 and SH4. • Updated the Revision History for Revision Number 1 to include the information on the Slew Rate Enable Register changes that occurred for that revision.
5	6/2008	• Added ICS over Temperature graph to Electricals appendix.

Revision Number	Revision Date	Description of Changes
6	7/2009	• Revised NV Register 0xFFAE address to have dashes instead of 0s. • Revised NVOPT register in Table 4-4 and Figure 4-6 so that Reserved is indicated with em dashes (—). • Changed ICS FLL deviation to 1.5% from 2%. • Table A-9, Row 1and Table A-6 footnote 10: Removed temperature reference. • Table A-9, Row 9: Changed Column C to “D” and Max to “1.5%” • Removed section A.14.2. • Updated Mechanical drawings to point to the Freescale web. • Rebuilt book to ensure proper footers and pagination. • Revised all "Reserved" vector space memory locations in Table 4-1 to read, "Unused Vector Space (available for user program)."
7	7/2011	• Revised to include high-temperature (up to 150 °C) devices for 16-pin TSSOP package. • In Table 2-1, added TCLK to row 20 and Alt 3 column. • Updated “How to Reach Us” information.
8	1/2014	Changes done in Chapter 3, “Modes of Operation”. Updated Table 3-1 Updated PPDC column to “x” from “0” for the specification STOPE=1,ENBDM=0,LVDE and LVDSE =both bits must be 1. Changes done in Appendix A, “Electrical Characteristics” • In Table A-6. DC Characteristics for column “Characteristic” moved “Reset” from parameter “P” to “C”. • In the Table A-6 added note 11 and 12 for parameter #18. Note 11: Device functionality is guaranteed between the LVD threshold VLVD0 and VDD Min.When VDD is below the minimum operating voltage (VDD Min), the analog parameters for the IO pins, ACMP and ADC, are not guaranteed to meet data sheet performance parameters. Note 12: In addition to LVD, it is recommended to also use the LVW feature. LVW can trigger an interrupt and be used as an indicator to warn that the VDD is dropping,so that the software can take actions accordingly before the VDD drops below VDD Min. • Table A-13. Control Timing. For the parameter “Internal low power oscillator period” changed the “Min” value from “800” to “700”.

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Chapter 1
Device Overview

The MC9S08SG8 members of the low-cost, high-performance HCS08 family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types. The high-temperature devices have been qualified to meet or exceed AEC Grade 0 requirements to allow them to operate up to 150 °C TA.

1.1 Devices in the MC9S08SG8 Series

Table 1-1 summarizes the feature set available in the MC9S08SG8 series of MCUs.

Table 1-1. MC9S08SG8 Features by MCU and Package

Feature	9S08SG8			9S08SG4		
FLASH size (bytes)	8192			4096		
RAM size (bytes)	512			256		
Pin quantity	20	16	8	20	16	8
ACMP	yes					
ADC channels	12	8	4	12	8	4
DBG	yes					
ICS	yes	yes	yes[1]	yes	yes	yes [1]
IIC	yes					
MTIM	yes					
Pin Interrupts	8	8	4	8	8	4
Pin I/O	16	12	4	16	12	4
RTC	yes					
SCI	yes	yes	no	yes	yes	no
SPI	yes	yes	no	yes	yes	no
TPM1 channels	2	2	1	2	2	1
TPM2 channels	2	2	1	2	2	1
XOSC	yes	yes	no	yes	yes	no

[1] FBE and FEE modes are not available in 8-pin packages.

1.2 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08SG8 MCU.

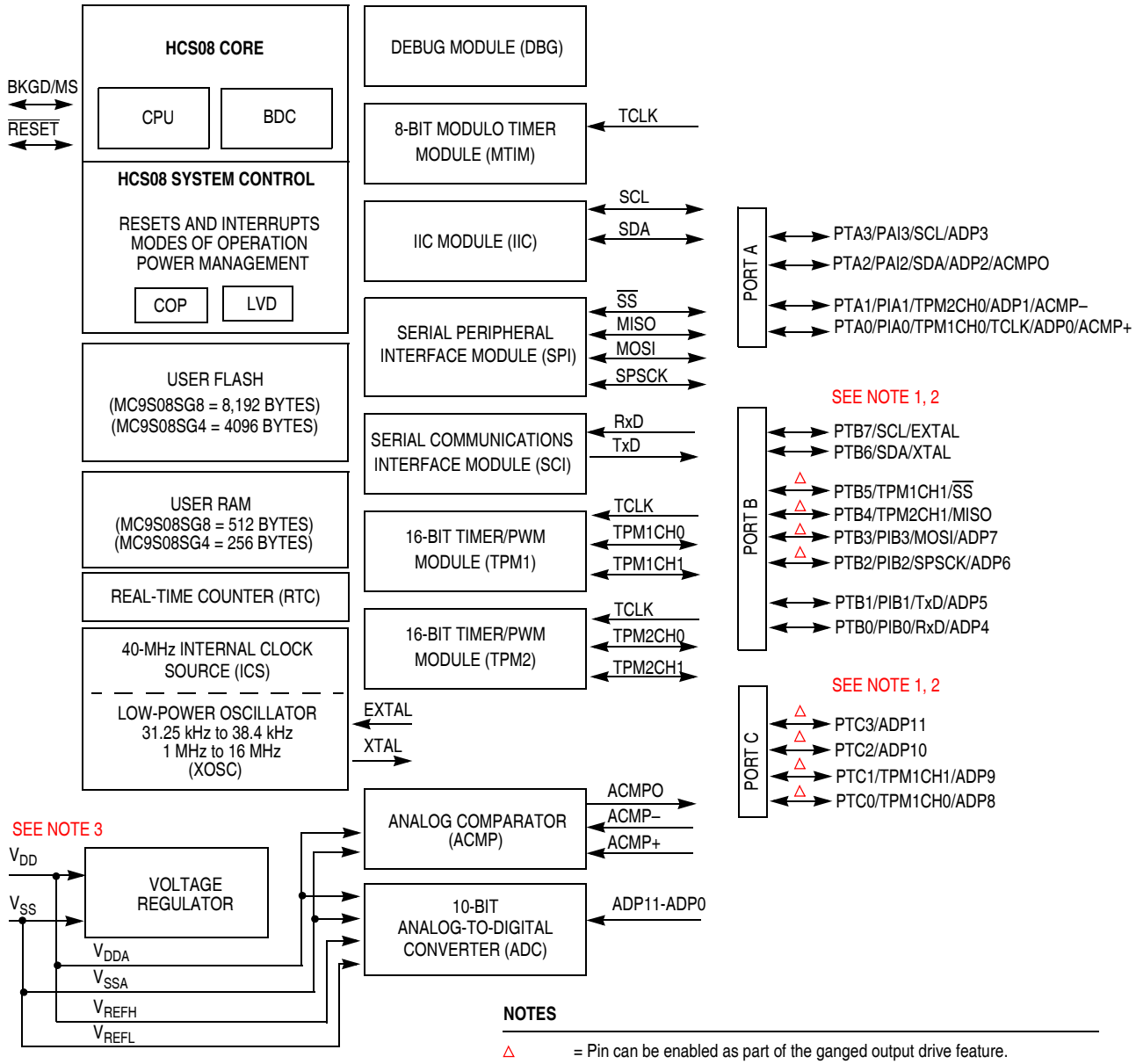

Figure 1-1. MC9S08SG8 Block Diagram

Table 1-2 provides the functional version of the on-chip modules.

Table 1-2. Module Versions

Module		Version
Analog Comparator (5V)	(ACMP)	2
Analog-to-Digital Converter	(ADC)	1
Central Processor Unit	(CPU)	2
Inter-Integrated Circuit	(IIC)	2
Internal Clock Source	(ICS)	2
Serial Peripheral Interface	(SPI)	3
Serial Communications Interface	(SCI)	4
Modulo Timer	(MTIM)	1
Real-Time Counter	(RTC)	1
Timer Pulse Width Modulator	(TPM)	3

1.3 System Clock Distribution

Figure 1-2 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function.

The following defines the clocks used in this MCU:

- BUSCLK — The frequency of the bus is always half of ICSOUT.
- ICSOUT — Primary output of the ICS and is twice the bus frequency.
- ICSLCLK — Development tools can select this clock source to speed up BDC communications in systems where the bus clock is configured to run at a very slow frequency.
- ICSERCLK — External reference clock can be selected as the RTC clock source and as the alternate clock for the ADC module.
- ICSIRCLK — Internal reference clock can be selected as the RTC clock source.
- ICSFFCLK — Fixed frequency clock can be selected as clock source for the TPM1, TPM2 and MTIM modules.
- LPOCLK — Independent 1-kHz clock source that can be selected as the clock source for the COP and RTC modules.
- TCLK — External input clock source for TPM1, TPM2 and MTIM and is referenced as TPMCLK in TPM chapters.

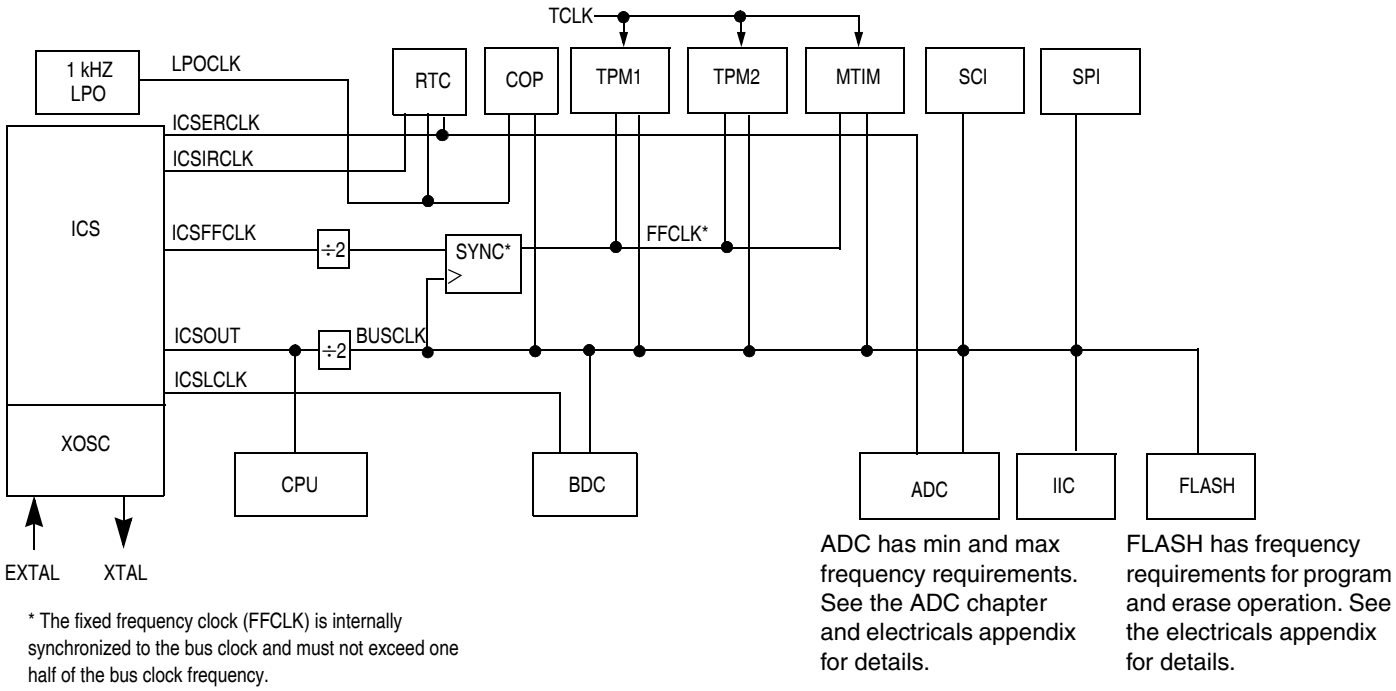

Figure 1-2. System Clock Distribution Diagram

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

Figure 2-1 - Figure 2-3 shows the pin assignments for the MC9S08SG8 devices.

NOTE

20-pin TSSOP package and 8-pin SOIC package are not available for the AEC Grade 0 high-temperature rated devices.

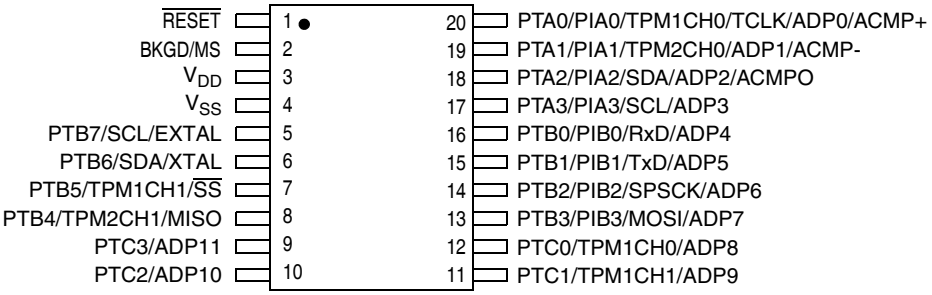

Figure 2-1. 20-Pin TSSOP

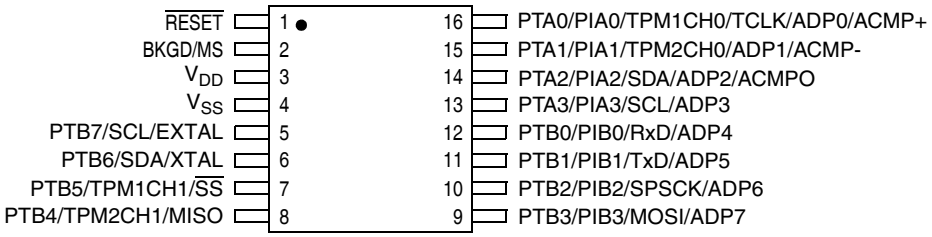

Figure 2-2. 16-Pin TSSOP