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MC9S08EL32
MC9S08EL16
MC9S08SL16
MC9S08SL8

Data Sheet

HCS08
Microcontrollers

MC9S08EL32
Rev. 3
7/2008

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MC9S08EL32 Features

8-Bit HCS08 Central Processor Unit (CPU)

- 40-MHz HCS08 CPU (central processor unit)
- HC08 instruction set with added BGND instruction
- Support for up to 32 interrupt/reset sources

On-Chip Memory

- FLASH read/program/erase over full operating voltage and temperature
- EEPROM in-circuit programmable memory; program and erase while executing FLASH; erase abort
- Random-access memory (RAM)
- Security circuitry to prevent unauthorized access to RAM and NVM contents

Power-Saving Modes

- Two very low-power stop modes
- Reduced power wait mode
- Very low-power real-time interrupt for use in run, wait, and stop

Clock Source Options

- Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
- Internal clock source (ICS) — Contains a frequency-locked loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supports bus frequencies from 2–20 MHz

System Protection

- Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- Illegal opcode detection with reset
- Illegal address detection with reset
- FLASH and EEPROM block protect

Development Support

- Single-wire background debug interface
- Breakpoint capability allows single breakpoint setting during in-circuit debugging (plus two more breakpoints in the on-chip debug module)
- In-circuit emulation (ICE) debug module — contains two comparators and nine trigger modes; eight-deep FIFO for storing change-of-flow address and event-only data; supports both tag and force breakpoints

Peripherals

- **ADC** — 16-channel, 10-bit resolution, 2.5 μs conversion time, automatic compare function, temperature sensor, internal bandgap reference channel; runs in stop3
- **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; output can optionally be routed to TPM module; runs in stop3
- **SCI** — Full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake-up on active edge
- **SLIC** — Supports LIN 2.0 and SAE J2602 protocols; up to 120 kbps, full LIN message buffering, automatic bit rate and frame synchronization, checksum generation and verification, UART-like byte transfer mode
- **SPI** — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
- **IIC** — Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer
- **TPMx** — One 4-channel (TPM1) and one 2-channel (TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
- **RTC** — 8-bit modulus real-time counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar, or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components

Input/Output

- 22 general purpose I/O pins
- 16 interrupt pins with selectable polarity
- Hysteresis and configurable pull up device on all input pins; Configurable slew rate and drive strength on all output pins.

Package Options

- 28-TSSOP
- 20-TSSOP

MC9S08EL32 Data Sheet

Covers MC9S08EL32
MC9S08EL16
MC9S08SL16
MC9S08SL8

MC9S08EL32
Rev. 3
7/2008

Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

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The following revision history table summarizes changes contained in this document.

Revision Number	Revision Date	Description of Changes
3	07/2008	Initial public revision

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Chapter 1
Device Overview

The MC9S08EL32 Series and MC9S08SL16 Series are members of the low-cost, high-performance HCS08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced HCS08 core and are available with a variety of modules, memory sizes, memory types, and package types.

1.1 Devices in the MC9S08EL32 Series and MC9S08SL16 Series

Table 1-1 summarizes the feature set available in the MC9S08EL32 Series and MC9S08SL16 Series of MCUs.

Table 1-1. MC9S08EL32 Series and MC9S08SL16 Series Features by MCU and Package

Feature	9S08EL32		9S08EL16		9S08SL16		9S08SL8	
FLASH size (bytes)	32768		16384		16384		8192	
RAM size (bytes)	1024				512			
EEPROM size (bytes)	512				256			
Pin quantity	28	20	28	20	28	20	28	20
Package type	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP	TSSOP
Port Interrupts	16	12	16	12	16	12	16	12
ACMP1	yes				yes			
ACMP2	yes	no	yes	no	no			
ADC channels	16	12	16	12	16	12	16	12
DBG	yes				yes			
ICS	yes				yes			
IIC	yes				yes			
RTC	yes				yes			
SCI	yes				yes			
SLIC	yes				yes			
SPI	yes				yes			
TPM1 channels	4				2			
TPM2 channels	2				2			
XOSC	yes				yes			

1.2 MCU Block Diagram

The block diagram in Figure 1-1 shows the structure of the MC9S08EL32 Series. Not all features are available on all devices in all packages. See Table 1-1 for details.

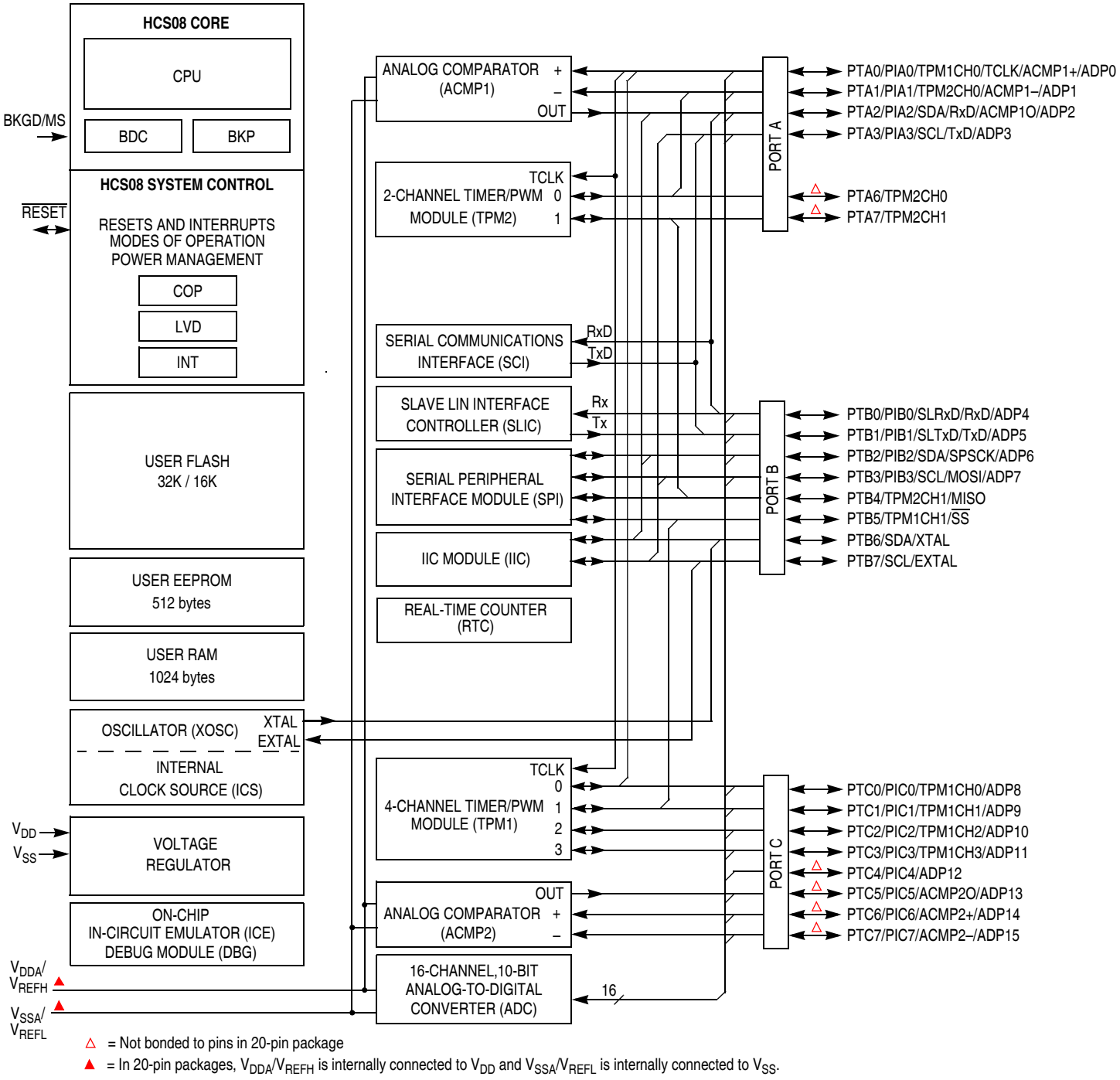

Figure 1-1. MC9S08EL32 and MC9S08EL16 Block Diagram

The block diagram in Figure 1-2 shows the structure of the MC9S08SL16 Series.

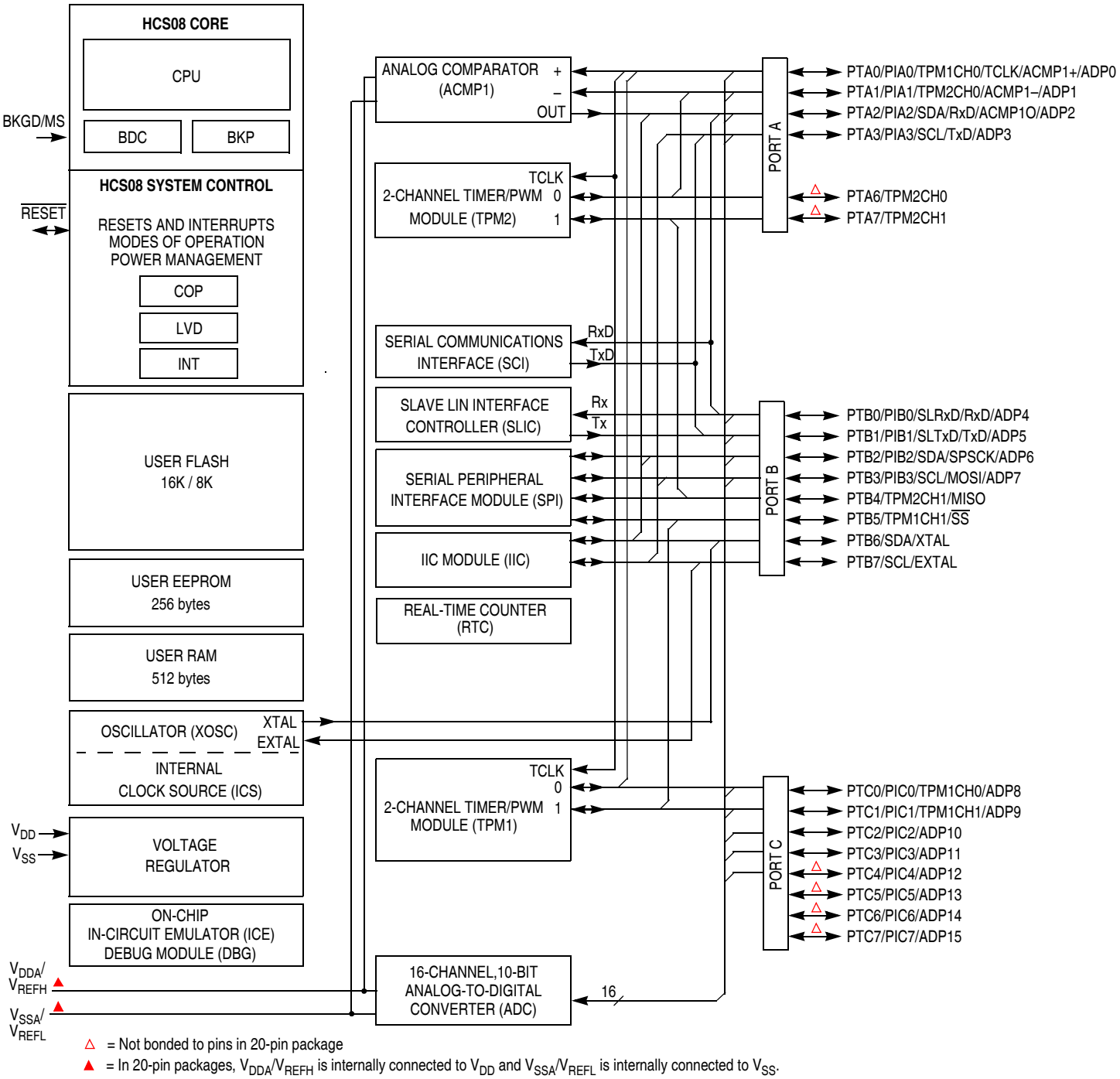

Figure 1-2. MC9S08SL16 and MC9S08SL8 Block Diagram

Table 1-2 provides the functional version of the on-chip modules

Table 1-2. Module Versions

Module		Version
Central Processor Unit	(CPU)	3
Internal Clock Source	(ICS)	2
5-V Analog Comparator	(ACMP_5V)	2
Analog-to-Digital Converter	(ADC)	1
Inter-Integrated Circuit	(IIC)	2
Slave LIN Interface Controller	(SLIC)	1
Serial Peripheral Interface	(SPI)	3
Serial Communications Interface	(SCI)	4
Real-Time Counter	(RTC)	1
Timer Pulse Width Modulator	(TPM)	2
On-Chip ICE Debug	(DBG)	2

1.3 System Clock Distribution

Figure 1-3 shows a simplified clock connection diagram. Some modules in the MCU have selectable clock inputs as shown. The clock inputs to the modules indicate the clock(s) that are used to drive the module function.

The following defines the clocks used in this MCU:

- BUSCLK — The frequency of the bus is always half of ICSOUT.
- ICSOUT — Primary output of the ICS and is twice the bus frequency.
- ICSLCLK — Development tools can select this clock source to speed up BDC communications in systems where the bus clock is configured to run at a very slow frequency.
- ICSERCLK — External reference clock can be selected as the RTC clock source and as the alternate clock for the ADC module.
- ICSIRCLK — Internal reference clock can be selected as the RTC clock source.
- ICSFFCLK — Fixed frequency clock can be selected as clock source for the TPM1 and TPM2 modules.
- LPO — Independent 1-kHz clock that can be selected as the source for the COP and RTC modules.
- TCLK — External input clock source for TPM1 and TPM2 and is referenced as TPMCLK in TPM chapters.

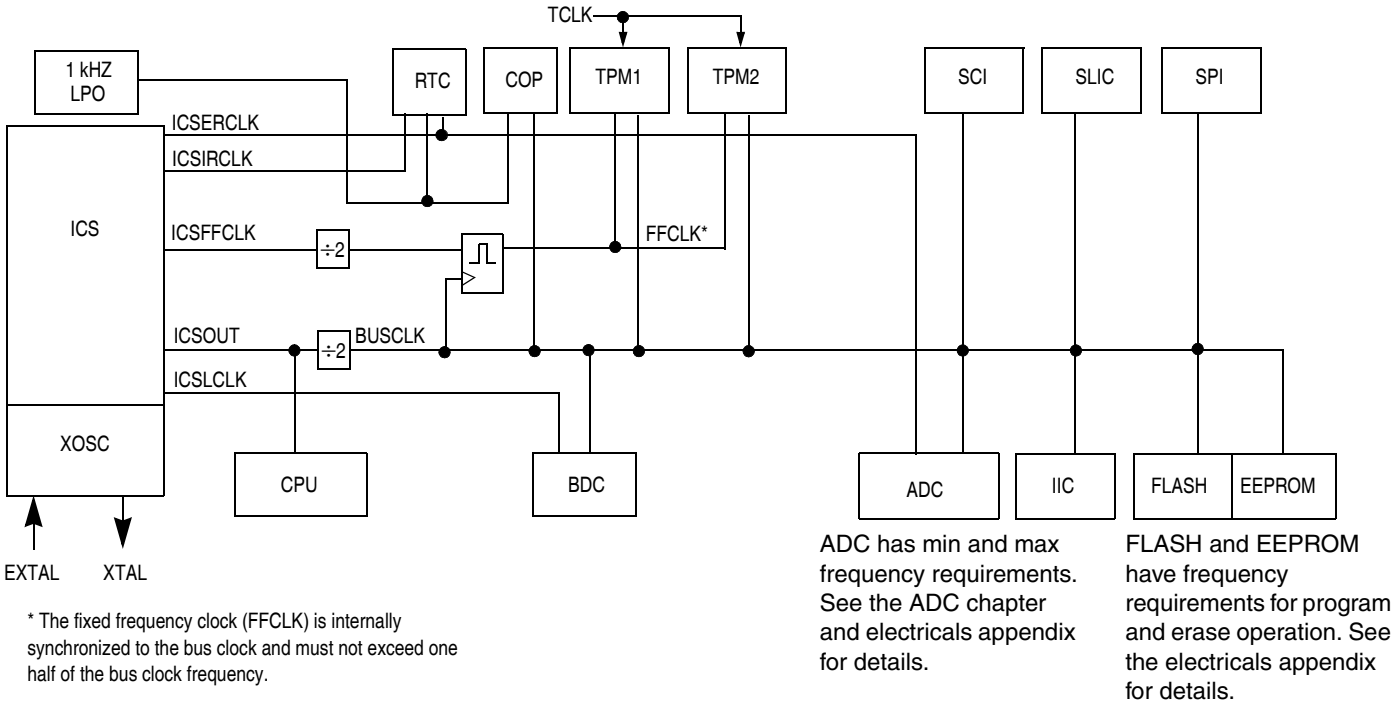

Figure 1-3. System Clock Distribution Diagram

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

This section describes pin assignments for the MC9S08EL32 Series and MC9S08SL16 Series devices. Not all features are available in all devices. See Table 1-1 for details.

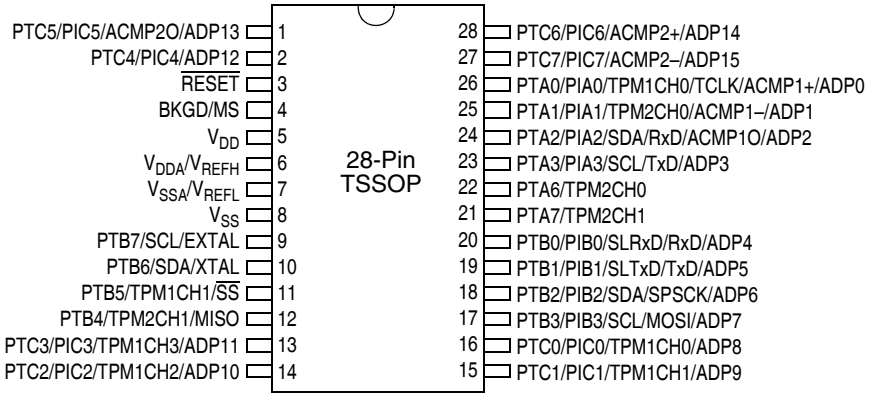

Figure 2-1. 28-Pin TSSOP

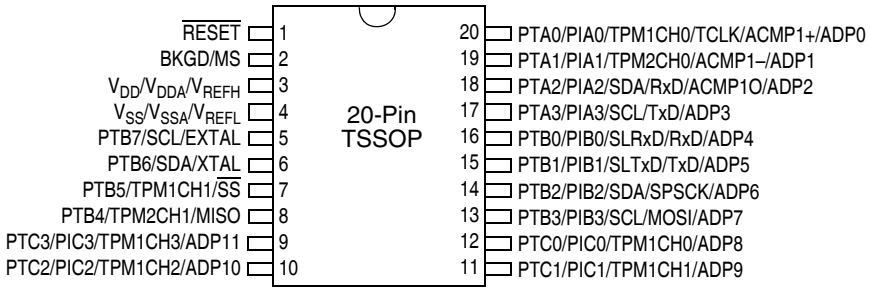

Figure 2-2. 20-Pin TSSOP