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MC9S12VR-Family
Reference Manual

S12 MagniV
Microcontrollers

MC9S12VRRM

Rev. 4.2

8-February-2016

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A full list of family members and options is included in the device overview section.

The following revision history table summarizes changes contained in this document.

This document contains information for all constituent modules, with the exception of the CPU. For CPU information please refer to **CPU12-1** in the **CPU12 & CPU12X Reference Manual**.

Revision History

Date	Revision Level	Description
06-July-2015	Rev 4.0 Draft C	• Removed electrical parameter classification • Changed BATS low voltage warning levels in Table I-2 NUM 1,5 and 6 • Removed 32QFN package • Added thermal specs for S12VR32
27-August-2015	Rev 4.0	• Updated S12HSDRVV3
21-December-2015	Rev 4.1	• Changed VDDX low voltage reset assert level from min 2.97V to 2.95V. see Table B-1 item 7b
8-February-2016	Rev 4.2	• Replaced Freescale logo by NXP logo

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Chapter 1
Device Overview MC9S12VR-Family

Revision History

Version Number	Revision Date	Description of Changes
Rev 3.4	30-January-2014	• Corrected Figure 1-4 32LQFP pinout pin 5
Rev 4.0 Initial Draft	3-February-2014	• Added MC9S12VR16 & MC9S12VR32 to Table 1-1 • Added MC9S12VR16 & MC9S12VR32 maskset N11N to Table 1-3 • Added CPMU differences between masksets N11N & N59H
Draft A	2-April-2014	• Added 32QFN package
Draft B	24-February-2015	• Included feedback from shared review

1.1 Introduction

The MC9S12VR-Family is an optimized automotive 16-bit microcontroller product line focused on low-cost, high-performance, and low pin-count. This family integrates an S12 microcontroller with a LIN Physical interface, a 5V regulator system to supply the microcontroller, and analog blocks to control other elements of the system which operate at vehicle battery level (e.g. relay drivers, high-side driver outputs, wake up inputs). The MC9S12VR-Family is targeted at generic automotive applications requiring single node LIN communications. Typical examples of these applications include window lift modules, seat modules and sun-roof modules to name a few.

The MC9S12VR-Family uses many of the same features found on the MC9S12G family, including error correction code (ECC) on flash memory, EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12VR-Family delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12VR-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of NXP's existing 8-bit and 16-bit MCU families. Like the MC9S12XS family, the MC9S12VR-Family runs 16-bit wide accesses without wait states for all peripherals and memories. Misaligned single cycle 16-bit RAM access is not supported. The MC9S12VR-Family is available in 32-pin and 48-pin LQFP. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12VR-Family is a general-purpose family of devices created with relay based motor control in mind and is suitable for a range of applications, including:

- Window lift modules
- Door modules
- Seat controllers

- Smart actuators
- Sun roof modules

1.2 Features

This section describes the key features of the MC9S12VR-Family.

1.2.1 MC9S12VR-Family Member Comparison

Table 1-1 provides a summary of different members of the MC9S12VR-Family and their features. This information is intended to provide an understanding of the range of functionality offered by this microcontroller family.

Table 1-1. MC9S12VR - Family

Feature	MC9S12VR16	MC9S12VR32	MC9S12VR48	MC9S12VR64	MC9S12VR48	MC9S12VR64
Package	32 LQFP				48 LQFP	
CPU	HCS12					
Flash memory (ECC)	16 Kbytes	32 Kbytes	48 Kbytes	64 Kbytes	48 Kbytes	64 Kbytes
EEPROM (ECC)	128 Bytes		512 Bytes			
RAM	2 Kbytes					
LIN physical layer	1					
SPI	—		1			
SCI	1		2			
Timer	4ch x 16-bit					
PWM	8ch x 8-bit or 4ch x 16-bit					
10-bit ADC channels	2				6	
Frequency modulated PLL	Yes					
Internal 1 MHz RC oscillator	Yes					
Autonomous window watchdog	1					
Low-side drivers (protected for inductive loads)	2					
High-side drivers	1				2	
High voltage Inputs	4					
General purpose I/Os (5V)	16				28	
Direct battery sense pin	1					
Supply voltage sense	1					

Feature	MC9S12VR16	MC9S12VR32	MC9S12VR48	MC9S12VR64	MC9S12VR48	MC9S12VR64
Chip temperature sensor	1					
Supply voltage	V_{SUP} = 6V – 18 V (normal operation) up to 40V (protected operation)					
EVDD output current	20mA @ 5V					
Maximum execution speed	25 MHz					

1.3 Chip-Level Features

On-chip modules available within the family include the following features:

- HCS12 CPU core
- 64, 48, 32 or 16 Kbyte on-chip flash with ECC
- 512 or 128 byte EEPROM with ECC
- 2 Kbyte on-chip SRAM
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range
- 4-20 MHz amplitude controlled pierce oscillator
- Internal COP (watchdog) module (with separate clock source)
- Timer module (TIM) supporting input/output channels that provide a range of 16-bit input capture, output compare and counter (up to 4 channels)
- Pulse width modulation (PWM) module (up to 8 x 8-bit channels)
- 10-bit resolution successive approximation analog-to-digital converter (ADC) with up to 6 channels available on external pins
- One serial peripheral interface (SPI) module
- One serial communication interface (SCI) module supporting LIN communications (with RX connected to a timer channel for internal oscillator calibration purposes, if desired)
- Up to one additional SCI (not connected to LIN physical layer)
- One on-chip LIN physical layer transceiver fully compliant with the LIN 2.2 standard & SAE J2602-2 LIN standard
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API) (combination with cyclic, watchdog)
- Two protected low-side outputs to drive inductive loads
- Up to two protected high-side outputs
- 4 high-voltage inputs with wake-up capability and readable internally on ADC
- Up to two 10mA high-current outputs
- 20mA high-current output for use as Hall sensor supply
- Battery voltage sense with low battery warning, internally reverse battery protected
- Chip temperature sensor

1.4 Module Features

The following sections provide more details of the modules implemented on the MC9S12VR-Family.

1.4.1 HCS12 16-Bit Central Processor Unit (CPU)

The HCS12 CPU is a high-speed, 16-bit processing unit that has a programming model identical to that of the industry standard M68HC11 central processor unit (CPU).

- Full 16-bit data paths supports efficient arithmetic operation and high-speed math execution
- Supports instructions with odd byte counts, including many single-byte instructions. This allows much more efficient use of ROM space.
- Extensive set of indexed addressing capabilities, including:
  - Using the stack pointer as an indexing register in all indexed operations
  - Using the program counter as an indexing register in all but auto increment/decrement mode
  - Accumulator offsets using A, B, or D accumulators
  - Automatic index predecrement, preincrement, postdecrement, and postincrement (by –8 to +8)

1.4.2 On-Chip Flash with ECC

On-chip flash memory on the MC9S12VR features the following:

- 64, 48, 32 or 16 Kbyte of program flash memory
  - Automated program and erase algorithm
  - Protection scheme to prevent accidental program or erase
- 512 or 128 Byte EEPROM
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 4 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

1.4.3 On-Chip SRAM

- 2 Kbytes of general-purpose RAM

1.4.4 Main External Oscillator (XOSCLCP)

- Loop control Pierce oscillator using 4 MHz to 20 MHz crystal
  - Current gain control on amplitude output
  - Signal with low harmonic distortion
  - Low power
  - Good noise immunity
  - Eliminates need for external current limiting resistor
  - Transconductance sized for optimum start-up margin for typical crystals
  - Oscillator pins shared with GPIO functionality

1.4.5 Internal RC Oscillator (IRC)

- Factory trimmed internal reference clock
  - 1 MHz internal RC oscillator with ±1.3% accuracy over rated temperature range

1.4.6 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier
  - No external components required
  - Reference divider and multiplier allow large variety of clock rates
  - Automatic bandwidth control mode for low-jitter operation
  - Automatic frequency lock detector
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
  - Reference clock sources:
    - Internal 1 MHz RC oscillator (IRC)

1.4.7 Clock and Power Management Unit (CPMU)

- Real time interrupt (RTI)
- Clock monitor (CM)
- System reset generation

1.4.8 System Integrity Support

- Power-on reset (POR)
- Illegal address detection with reset
- Low-voltage detection with interrupt or reset
- Computer operating properly (COP) watchdog with option to run on internal RC oscillator
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory