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MC9S12XS256
Reference Manual

Covers MC9S12XS Family
MC9S12XS256
MC9S12XS128
MC9S12XS64

HCS12
Microcontrollers

MC9S12XS256RMV1

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This document contains information for the complete S12XS Family and thus includes a set of separate flash (FTMR) module sections to cover the whole family. A full list of family members and options is included in the appendices.

This document contains information for all constituent modules, with the exception of the CPU. For CPU information please refer to CPU12XV1 in the CPU12/CPU12X Reference Manual.

Revision History

Date	Revision Level	Description
November, 2010	1.11	Updated Chapter 3 Memory Mapping Control (S12XMMCV4) Updated Chapter 11 Freescale's Scalable Controller Area Network (S12MSCANV3) Updated Chapter 14 Serial Communication Interface (S12SCIV5) Updated footnotes on table 1-2 Updated note in Appendix F Ordering Information
Jul, 2011	1.12	Corrected API accuracy in feature list Corrected name of pin #27 in 80QFP pinout (PE5->PE4) Updated Chapter 2 Port Integration Module (S12XSPIMV1) Updated Chapter 11 Freescale's Scalable Controller Area Network (S12MSCANV3)
Aug, 2012	1.13	Updated Chapter 4 Interrupt (S12XINTV2) Updated Chapter 8 S12XE Clocks and Reset Generator (S12XECRGV1) Updated V_{DDF} max. voltage in Appendix A Electrical Characteristics Minor editorial corrections in: Chapter 2 Port Integration Module (S12XSPIMV1) Chapter 5 Background Debug Module (S12XBDMV2) Chapter 6 S12X Debug (S12XDBGV3) Module

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Chapter 1
Device Overview S12XS Family

1.1 Introduction

The new S12XS family of 16-bit micro controllers is a compatible, reduced version of the S12XE family. These families provide an easy approach to develop common platforms from low-end to high-end applications, minimizing the redesign of software and hardware.

Targeted at generic automotive applications and CAN nodes, some typical examples of these applications are: Body Controllers, Occupant Detection, Door Modules, RKE Receivers, Smart Actuators, Lighting Modules and Smart Junction Boxes amongst many others.

The S12XS family retains many of the features of the S12XE family including Error Correction Code (ECC) on Flash memory, a separate Data-Flash Module for code or data storage, a Frequency Modulated Locked Loop (IPLL) that improves the EMC performance and a fast ATD converter.

S12XS family delivers 32-bit performance with all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC and code-size efficiency advantages currently enjoyed by users of Freescale's existing 16-bit S12 and S12X MCU families. Like members of other S12X families, the S12XS family runs 16-bit wide accesses without wait states for all peripherals and memories.

The S12XS family is available in 112-pin LQFP, 80-pin QFP, 64-pin LQFP package options and maintains a high level of pin compatibility with the S12XE family. In addition to the I/O ports available in each module, up to 18 further I/O ports are available with interrupt capability allowing Wake-Up from stop or wait modes.

The peripheral set includes MSCAN, SPI, two SCIs, an 8-channel 24-bit periodic interrupt timer, 8-channel 16-bit Timer, 8-channel PWM and up to 16- channel 12-bit ATD converter.

Software controlled peripheral-to-port routing enables access to a flexible mix of the peripheral modules in the lower pin count package options.

1.1.1 Features

Features of the S12XS Family are listed here. Please see Table D-1 for memory options and Table D-2 for the peripheral features that are available on the different family members.

- 16-bit CPU12X
  - Upward compatible with S12 instruction set with the exception of five Fuzzy instructions (MEM, WAV, WAVR, REV, REVW) which have been removed
  - Enhanced indexed addressing
  - Access to large data segments independent of PPAGE

- INT (interrupt module)
  - Seven levels of nested interrupts
  - Flexible assignment of interrupt sources to each interrupt level.
  - External non-maskable high priority interrupt (XIRQ)
  - The following inputs can act as Wake-up Interrupts
    - IRQ and non-maskable XIRQ
    - CAN receive pins
    - SCI receive pins
    - Depending on the package option up to 20 pins on ports J, H and P configurable as rising or falling edge sensitive
- MMC (module mapping control)
- DBG (debug module)
  - Monitoring of CPU bus with tag-type or force-type breakpoint requests
  - 64 x 64-bit circular trace buffer captures change-of-flow or memory access information
- BDM (background debug mode)
- OSC_LCP (oscillator)
  - Low power loop control Pierce oscillator utilizing a 4MHz to 16MHz crystal
  - Good noise immunity
  - Full-swing Pierce option utilizing a 2MHz to 40MHz crystal
  - Transconductance sized for optimum start-up margin for typical crystals
- IPLL (Internally filtered, frequency modulated phase-locked-loop clock generation)
  - No external components required
  - Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
- CRG (clock and reset generation)
  - COP watchdog
  - Real time interrupt
  - Clock monitor
  - Fast wake up from STOP in self clock mode
- Memory Options
  - 64, 128 and 256 Kbyte Flash
  - Flash General Features
    - 64 data bits plus 8 syndrome ECC (Error Correction Code) bits allow single bit failure correction and double fault detection
    - Erase sector size 1024 bytes
    - Automated program and erase algorithm
    - Protection scheme to prevent accidental program or erase
    - Security option to prevent unauthorized access
    - Sense-amp margin level setting for reads
  - 4 and 8 Kbyte Data Flash space

- 16 data bits plus 6 syndrome ECC (Error Correction Code) bits allow single bit failure correction and double fault detection
- Erase sector size 256 bytes
- Automated program and erase algorithm

— 4, 8 and 12 Kbyte RAM

- 16-channel, 12-bit Analog-to-Digital converter
  - 8/10/12 Bit resolution
  - 3µs, 10-bit single conversion time
  - Left or right justified result data
  - External and internal conversion trigger capability
  - Internal oscillator for conversion in Stop modes
  - Wake from low power modes on analog comparison > or <= match
  - Continuous conversion mode
  - Multiplexer for 16 analog input channels
  - Multiple channel scans
  - Pins can also be used as digital I/O
- MSCAN (1 M bit per second, CAN 2.0 A, B software compatible module)
  - 1 Mbit per second, CAN 2.0 A, B software compatible module
    - Standard and extended data frames
    - 0 - 8 bytes data length
    - Programmable bit rate up to 1 Mbps
  - Five receive buffers with FIFO storage scheme
  - Three transmit buffers with internal prioritization
  - Flexible identifier acceptance filter programmable as:
    - 2 x 32-bit
    - 4 x 16-bit
    - 8 x 8-bit
  - Wake-up with integrated low pass filter option
  - Loop back for self test
  - Listen-only mode to monitor CAN bus
  - Bus-off recovery by software intervention or automatically
  - 16-bit time stamp of transmitted/received messages
- TIM (standard timer module)
  - 8 x 16-bit channels for input capture or output compare
  - 16-bit free-running counter with 8-bit precision prescaler
  - 1 x 16-bit pulse accumulator
- PIT (periodic interrupt timer)
  - Up to four timers with independent time-out periods
  - Time-out periods selectable between 1 and 2^{24} bus clock cycles

  - Time-out interrupt and peripheral triggers
  - Start of timers can be aligned
- Up to 8 channel x 8-bit or 4 channel x 16-bit Pulse Width Modulator
  - Programmable period and duty cycle per channel
  - Center- or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
- Serial Peripheral Interface Module (SPI)
  - Configurable for 8 or 16-bit data size
  - Full-duplex or single-wire bidirectional
  - Double-buffered transmit and receive
  - Master or Slave mode
  - MSB-first or LSB-first shifting
  - Serial clock phase and polarity options
- Two Serial Communication Interfaces (SCI)
  - Full-duplex or single wire operation
  - Standard mark/space non-return-to-zero (NRZ) format
  - Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
  - 13-bit baud rate selection
  - Programmable character length
  - Programmable polarity for transmitter and receiver
  - Receive wakeup on active edge
  - Break detect and transmit collision detect supporting LIN
- On-Chip Voltage Regulator
  - Two parallel, linear voltage regulators with bandgap reference
  - Low-voltage detect (LVD) with low-voltage interrupt (LVI)
  - Power-on reset (POR) circuit
  - Low-voltage reset (LVR)
- Low-power wake-up timer (API)
  - Internal oscillator driving a down counter
  - Trimmable to +/-5% accuracy
  - Time-out periods range from 0.2ms to ~13s with a 0.2ms resolution
- Input/Output
  - Up to 91 general-purpose input/output (I/O) pins depending on the package option and 2 input-only pins
  - Hysteresis and configurable pull up/pull down device on all input pins
  - Configurable drive strength on all output pins
- Package Options
  - 112-pin low-profile quad flat-pack (LQFP)
  - 80-pin quad flat-pack (QFP)

  - 64-pin low-profile quad flat-pack (LQFP)
- Operating Conditions
  - Wide single Supply Voltage range 3.135 V to 5.5 V at full performance
    - Separate supply for internal voltage regulator and I/O allow optimized EMC filtering
  - 40MHz maximum CPU bus frequency
  - Ambient temperature range –40°C to 125°C
  - Temperature Options:
    - –40°C to 85°C
    - –40°C to 105°C
    - –40°C to 125°C

1.1.2 Modes of Operation

Operating modes:

- Normal single-chip mode
- Special single-chip mode with active background debug mode

NOTE

This chip family does not support external bus modes.

Low-power modes:

- System stop modes
  - Pseudo stop mode
  - Full stop mode with fast wake-up option
- System wait mode

1.1.3 Block Diagram

Figure 1-1 shows a block diagram of the S12XS Family devices

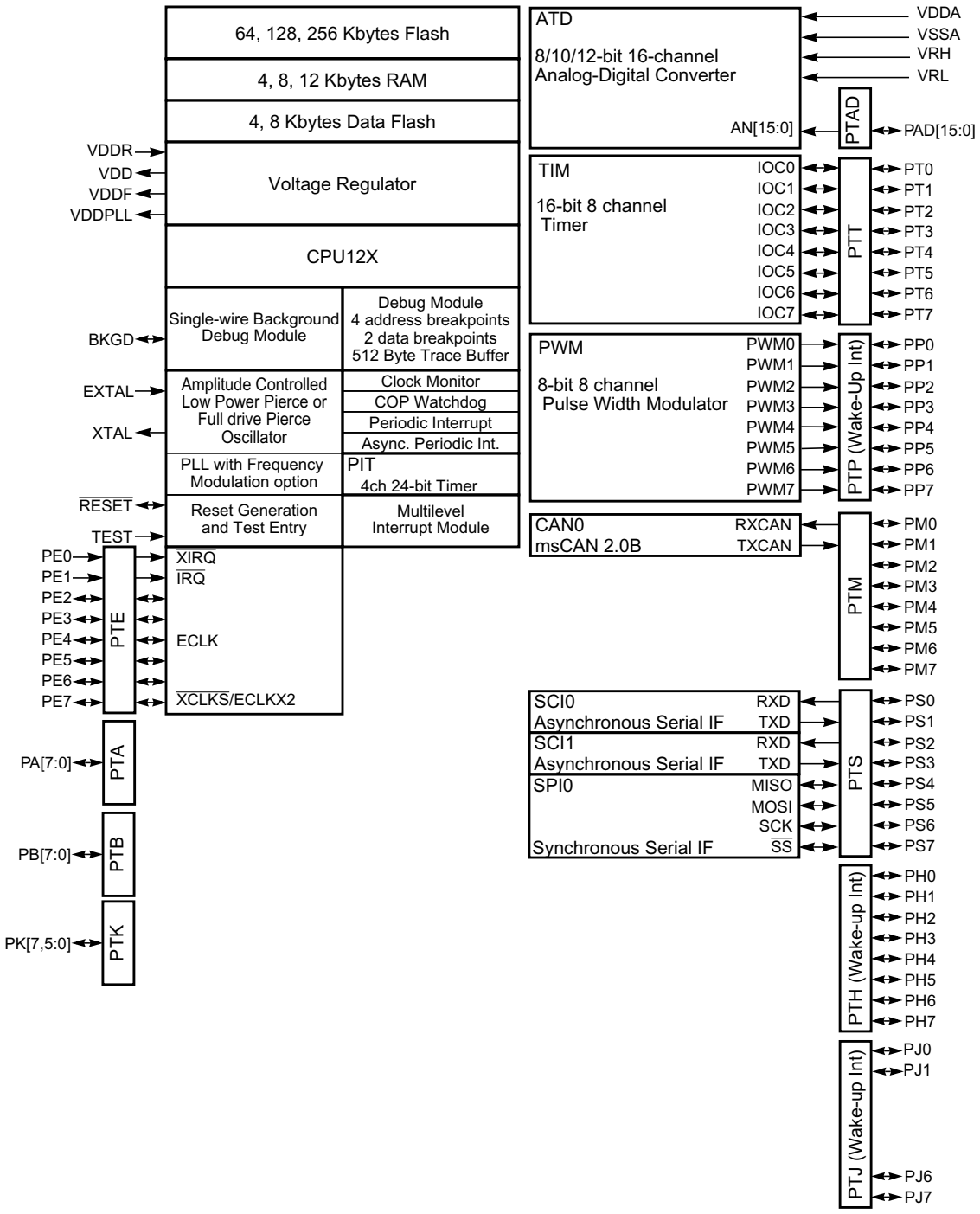

Figure 1-1. S12XS Family Block Diagram

1.1.4 Device Memory Map

Table 1-1 shows the device register memory map.

Table 1-1. Device Register Memory Map

Address	Module	Size (Bytes)
0x0000–0x0009	PIM (port integration module)	10
0x000A–0x000B	MMC (memory map control)	2
0x000C–0x000D	PIM (port integration module)	2
0x000E–0x000F	Reserved	2
0x0010–0x0017	MMC (memory map control)	8
0x0018–0x0019	Reserved	2
0x001A–0x001B	Device ID register	2
0x001C–0x001F	PIM (port integration module)	4
0x0020–0x002F	DBG (debug module)	16
0x0030–0x0031	Reserved	2
0x0032–0x0033	PIM (port integration module)	2
0x0034–0x003F	ECRG (clock and reset generator)	12
0x0040–0x006F	TIM (timer module)	48
0x0070–0x00C7	Reserved	88
0x00C8–0x00CF	SCI0 (serial communications interface)	8
0x00D0–0x00D7	SCI1 (serial communications interface)	8
0x00D8–0x00DF	SPI0 (serial peripheral interface)	8
0x00E0–0x00FF	Reserved	32
0x0100–0x0113	FTMR control registers	20
0x0114–0x011F	Reserved	12
0x0120–0x012F	INT (interrupt module)	16
0x0130–0x013F	Reserved	16
0x0140–0x017F	CAN0	64
0x0180–0x023F	Reserved	192
0x0240–0x027F	PIM (port integration module)	64
0x0280–0x02BF	Reserved	64
0x02C0–0x02EF	ATD0 (analog-to-digital converter 12 bit 16-channel)	48
0x02F0–0x02F7	Voltage regulator	8
0x02F8–0x02FF	Reserved	8
0x0300–0x0327	PWM (pulse-width modulator 8 channels)	40
0x0328–0x033F	Reserved	24
0x0340–0x0367	PIT (periodic interrupt timer)	40