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MC9S12ZVL Family Reference Manual and Datasheet

S12 MagniV Microcontrollers

Rev. 2.41
October 24, 2017
MC9S12ZVLRM

nxp.com

The MC9S12ZVL family of microcontrollers is targeted at use in safety relevant systems and has been developed using an ISO26262 compliant development system under the NXP Safe Assure program.

For more details of how to use the device in safety relevant systems refer to the MC9S12ZVL Safety Manual at :

http://nxp.com/S12ZVL

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://nxp.com

A full list of family members and options is included in the device overview section.

This document contains information for all constituent modules, with the exception of the S12Z CPU. For S12ZCPU information please refer to the CPU S12Z Reference Manual.

NOTE

This reference manual documents the entire S12ZVL-Family. It contains a superset of features within the family. Some module versions differ from one part to another within the family. Section 1.2.1 MC9S12ZVL-Family Member Comparison provides support to access the correct information for a particular part within the family.

Revision History

Date	Revision Level	Description
28 September 2013	0.14	• Updated Chapter 1, “Device Overview MC9S12ZVL-Family” • Updated Chapter 10, “Analog-to-Digital Converter (ADC12B_LBA)” • Updated Chapter 18, “Serial Communication Interface (S12SCIV6)” • Updated Chapter 19, “Serial Peripheral Interface (S12SPIV5)” • Updated Chapter 21, “LIN Physical Layer (S12LINPHYV2)”” • Updated Appendix A, “MCU Electrical Specifications” • Updated Appendix O, “Detailed Register Address Map” • Updated Appendix N, “Ordering Information”
28 November 2013	0.15	• Updated Chapter 1, “Device Overview MC9S12ZVL-Family” • Updated Chapter 8, “ECC Generation Module (SRAM_ECCV2)” • Updated Chapter 10, “Analog-to-Digital Converter (ADC12B_LBA)” • Updated MC9S12ZVL” • Updated Chapter 19, “Serial Peripheral Interface (S12SPIV5)” • Updated Chapter 21, “LIN Physical Layer (S12LINPHYV2)”” • Updated Appendix A, “MCU Electrical Specifications”
17 September 2014	1.00	• Updated Chapter 1, “Device Overview MC9S12ZVL-Family” • Updated Chapter 5, “Background Debug Controller (S12ZBDCV2)” • Updated Chapter 7, “S12Z DebugLite (S12ZDBGV3)” • Updated Chapter 22, “Flash Module (S12ZFTMRZ)” • Updated Chapter 21, “LIN Physical Layer (S12LINPHYV2)”” • Updated Appendix A, “MCU Electrical Specifications” • Updated Appendix O, “Detailed Register Address Map • Updated Appendix M, “Package Information
16 October 2014	1.01	• Updated Appendix A, “MCU Electrical Specifications”
11 December 2014	2.00	Initial version including ZVL128 • Updated Chapter 1, “Device Overview MC9S12ZVL-Family” • Updated Chapter 2, “Port Integration Module (S12ZVLPIMV2)” • Added Chapter 3, “5V Analog Comparator (ACMPV2)” • Updated Chapter 7, “S12Z DebugLite (S12ZDBGV3)” • Updated Chapter 10, “Analog-to-Digital Converter (ADC12B_LBA)” • Added Chapter 11, “Digital Analog Converter (DAC_8B5V_V2)” • Added Chapter 12, “Programmable Gain Amplifier (PGAV1)” • Added Chapter 13, “Scalable Controller Area Network (S12MSCANV2)” • Updated Chapter 22, “Flash Module (S12ZFTMRZ)” • Updated Appendix O, “Detailed Register Address Map”
05 May 2015	2.00 Draft D	• Updated Chapter 1, “Device Overview MC9S12ZVL-Family” • Added new version of Chapter 8, “ECC Generation Module (SRAM_ECCV2)” • Added new version of Chapter 9, “S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)” • Added new version of Chapter 12, “Programmable Gain Amplifier (PGAV1) • added VL128 specific parameter (3.3V VDDX mode, Supply Current Table) to Appendix A, “MCU Electrical Specifications

Revision History

Date	Revision Level	Description
13 May 2015	2.00 Draft E	• Added new version of Chapter 12, “Programmable Gain Amplifier (PGAV1) • Added new version of Chapter 11, “Digital Analog Converter (DAC_8B5V_V2) • added missing modules DAC, PGA, ACMP, PWM1 to Appendix O, “Detailed Register Address Map • update voltage range inside Appendix I, “ACMP Electrical Specifications and Appendix G, “DAC_8B5V Electrical Specifications
05 June 2015	2.00 Draft F	• Added new version of Chapter 1, “Device Overview MC9S12ZVL-Family” • Added new version of Appendix A, “MCU Electrical Specifications
27 October 2015	2.00 Draft G	• Added new version v0.4 of Appendix A, “MCU Electrical Specifications” • correct Order Information
25 February 2016	2.00Draft I	• change to NXP style • Added new version of Appendix A, “MCU Electrical Specifications
10 May 2016	2.00	• Added version 0.80 of Appendix A, “MCU Electrical Specifications • changed to Chapter 10, “Analog-to-Digital Converter (ADC12B_LBA) version V3
08 August 2017	2.10	• Added version 0.90 of Appendix A, “MCU Electrical Specifications • Added version 2.00 of Chapter 1, “Device Overview MC9S12ZVL-Family
12 September 2017	2.20	• Added version 1.0 of Appendix A, “MCU Electrical Specifications
10 October 2017	2.30	• Added version 1.1 of Appendix A, “MCU Electrical Specifications
19 October 2017	2.40	• Added version 1.2 of Appendix A, “MCU Electrical Specifications
24 October 2017	2.41	• Added version 1.21 of Appendix A, “MCU Electrical Specifications

Chapter 1
Device Overview MC9S12ZVL-Family

Chapter 2
Port Integration Module (S12ZVLPIMV2)

Chapter 3
5V Analog Comparator (ACMPV2)

Chapter 4
Memory Mapping Control (S12ZMMCV1)

Chapter 5
Background Debug Controller (S12ZBDCV2)

Chapter 6
Interrupt (S12ZINTV0)

Chapter 7
S12Z DebugLite (S12ZDBGV3)

Chapter 8
ECC Generation Module (SRAM_ECCV2)

Chapter 9
S12 Clock, Reset and Power Management Unit (S12CPMU_UHV)

Chapter 10
Analog-to-Digital Converter (ADC12B_LBA)

Chapter 11
Digital Analog Converter (DAC_8B5V_V2)

Chapter 12
Programmable Gain Amplifier (PGAV1)

Chapter 13
Scalable Controller Area Network (S12MSCANV2)

Chapter 14
Supply Voltage Sensor (BATSV3)

Chapter 15
Timer Module (TIM16B6CV3)

Chapter 16
Timer Module (TIM16B2CV3)

Chapter 17
Pulse-Width Modulator (S12PWM8B8CV2)

Chapter 18
Serial Communication Interface (S12SCIV6)

Chapter 19
Serial Peripheral Interface (S12SPIV5)

Chapter 20
Inter-Integrated Circuit (IICV3)

Chapter 21
LIN Physical Layer (S12LINPHYV2)

Chapter 22
Flash Module (S12ZFTMRZ)

Appendix A
MCU Electrical Specifications

Appendix B
CPMU Electrical Specifications (VREG, OSC, IRC, PLL)

Appendix C
ADC Specifications

Appendix D
LINPHY Electrical Specifications

Appendix E
NVM Electrical Parameters

Appendix F
BATS Electrical Specifications

Appendix G
DAC_8B5V Electrical Specifications

Appendix H
PGA Electrical Specifications

Appendix I
ACMP Electrical Specifications

Appendix J
PIM Electrical Specifications

Appendix K
SPI Electrical Specifications

Appendix L
MSCAN Electrical Specifications

Appendix M
Package Information

Appendix N
Ordering Information

Appendix O
Detailed Register Address Map

Chapter 1
Device Overview MC9S12ZVL-Family

Table 1-1. Revision History

Version Number	Revision Date	Description of Changes
1.0	28. May 2013	• added feedback from shared review • changed IFR mapping table conditional text to make the ADC reference conversion visible for the customer
1.1	26. Aug.2013	• added feedback from shared review
1.2	29. Aug.2013	• update table 1-12, replaced for SCI0/1 EX with RX
1.3	19.Sep. 2013	• added chapter 1.13.2, “BDC Command Restriction”
1.4	2 April 2014	• fix findings from the shared review
1.5	5 Aug. 2014	• fix typo PMW -> PWM
1.6	24 Sep. 2014	• added the VL128 device
1.7	21 Oct. 2014	• added PWM channel muxing • added PGA - DAC - ACMP - ADC analog connections
1.8	03 Jun. 2015	• correct alignment in table 1-15
1.9	27 Oct. 2015	• correct table 1-3
2.0	08 Aug. 2017	• correct CTRL register name for PAD6-PAD9, table 1-6 • correct 32-pin QFN-EP availability, table 1-2

1.1 Introduction

The MC9S12ZVL-Family is an automotive 16-bit microcontroller family using the 180nm NVM + UHV technology that offers the capability to integrate 40V analog components. This family reuses many features from the existing S12 portfolio. The particular differentiating features of this family are the enhanced S12Z core and the integration of “high-voltage” analog modules, including the voltage regulator (VREG) and a Local Interconnect Network (LIN) physical layer.

The MC9S12ZVL-Family includes error correction code (ECC) on RAM, FLASH and EEPROM for diagnostic or data storage, a fast analog-to-digital converter (ADC) and a frequency modulated phase locked loop (IPLL) that improves the EMC performance. The MC9S12ZVL-Family delivers an optimized solution with the integration of several key system components into a single device, optimizing system architecture and achieving significant space savings. The MC9S12ZVL-Family delivers all the advantages and efficiencies of a 16-bit MCU while retaining the low cost, power consumption, EMC, and code-size efficiency advantages currently enjoyed by users of existing S12 families. The MC9S12ZVL-Family is available in 48-pin, 32-pin LQFP and 32-pin QFN-EP. In addition to the I/O ports available in each module, further I/O ports are available with interrupt capability allowing wake-up from stop or wait modes.

The MC9S12ZVL-Family is a general-purpose family of devices suitable for a wide range of applications. The MC9S12ZVL-Family is targeted at generic automotive applications requiring LIN connectivity. Typical examples of these applications include switch panels and body endpoints for sensors.

1.2 Features

This section describes the key features of the MC9S12ZVL-Family.

1.2.1 MC9S12ZVL-Family Member Comparison

Table 1-2 provides a summary of main features within the MC9S12ZVL-Family.

Table 1-2. MC9S12ZVL-Family Comparison

Feature	MC9S12ZVL128 MC9S12ZVLA128	MC9S12ZVL96 MC9S12ZVLA96	MC9S12ZVL64 MC9S12ZVLA64	MC9S12ZVL32	MC9S12ZVL16	MC9S12ZVL8	MC9S12ZVLS32	MC9S12ZVLS16
Flash memory (ECC) [KB]	128	96	64	32	16	8	32	16
EEPROM (ECC) [Byte]	2048		1024	128			128	
RAM (ECC) [Byte]	8192		4096	1024	1024	512	1024	
max bus clock	32 MHz			32 MHz			32 MHz	
HVI	1			1			1	
LIN Physical layer	1			1			1	
Vreg current capability(1) - 70 mA (VDDX) - 170 mA ballast option (BCTL) - tolerance - 3.3V VDDX support, see also: 9.3.2.27, “Voltage Regulator Control Register (CPMUVREGCTL)	yes yes 3% / 2%(2) yes			yes yes 3% no			yes yes 3% no	
ASIL SEooC target	A			A			A	
Package	48-pin / 32-pin LQFP / 32-pin QFN-EP			48-pin / 32-pin LQFP			32-pin QFN-EP	
ADC channels -10-bit -12-bit	10(3) / 6 10(3)(2) / 6(2)			10(3) / 6 -			6 -	
PWM	8 16 bit Channels			8 Channel (up to 4 16 bit)			8 Channel (up to 4 16 bit)	
DAC	1(4)(2)			-			-	
PGA[5]	1(2)			-			-	
ACMP	1(2)			-			-	
Timer	6 + 2 channel			6 + 2 channel			6 + 2 channel	

Table 1-2. MC9S12ZVL-Family Comparison

Feature	MC9S12ZVL128 MC9S12ZVLA128	MC9S12ZVL96 MC9S12ZVLA96	MC9S12ZVL64 MC9S12ZVLA64	MC9S12ZVL32	MC9S12ZVL16	MC9S12ZVL8	MC9S12ZVLS32	MC9S12ZVLS16
SCI[6]	2			2			2	
SPI	1			1			1	
IIC	1			1			1	
MSCAN	1			-			-	
max SRAM_ECC access width	4 Byte			2 Byte			2 Byte	
Supported ADC option bits	yes			no			no	
General purpose I/O - pin to support 25 mA driver strength to VSSX - pin to support 20 mA driver strength from VDDX (EVDD)	34(3) / 19 3(3) / 1 1			34(3) / 19 3(3) / 1 1			18 3 1	
Interrupt capable pins[7] 5V / 12V	22(3) / 16 / 1			22(3) / 16 / 1			14 / 1	

1 total current capability for MCU and MCU - external loads (on same PCB - board)
2 MC9S12ZVLA device only
3 available in 48-pin packages only
4 to internally feed the ACMP or bonded out in 48-LQFP
5 only 5V operation mode supported
6 one SCI routed to the LINPHY
7 $\overline{\text{IRQ}}$ / $\overline{\text{XIRQ}}$ and KWx pins

NOTE

After power up, the MC9S12ZVL(A)128/96/64 devices starts in 3.3V VDDX mode. Then is possible to switch to the 5.0V VDDX behavior. For more details see the “Clock, Reset and Power Management Unit” section, 9.3.2.27, “Voltage Regulator Control Register (CPMUVREGCTL)

1.3 Chip-Level Features

On-chip modules available within the family include the following features:

- S12Z CPU core
- 128, 96, 64, 32, 16 or 8 KB on-chip flash with ECC
- 2048, 1024, 128 byte EEPROM with ECC
- 8192, 4096, 1024 or 512 byte on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range
- 4-20 MHz amplitude controlled pierce oscillator

- Internal COP (watchdog) module
- analog-to-digital converter (ADC) with 10 -bit or 12 -bit resolution and up to 10 channels available on external pins and V_{bg} (bandgap) result reference
- PGA module with two input channels
- One 8-bit 5V digital-to-analog converter (DAC)
- One analog comparators (ACMP) with rail-to-rail inputs
- MSCAN (1 Mbit/s, CAN 2.0 A, B software compatible) module
- One serial peripheral interface (SPI) module
- One serial communication interface (SCI) module with interface to internal LIN physical layer transceiver (with RX connected to a timer channel for frequency calibration purposes, if desired)
- Up to one additional SCI (not connected to LIN physical layer)
- One on-chip LIN physical layer transceiver fully compliant with the LIN 2.2 standard
- 6-channel timer module (TIM0) with input capture/output compare
- 2-channel timer module (TIM1) with input capture/output compare
- Inter-IC (IIC) module
- 8-channel Pulse Width Modulation module (PWM)
- On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
- Autonomous periodic interrupt (API), supports cyclic wakeup from Stop mode
- Pins to support 25 mA drive strength to VSSX
- Pin to support 20 mA drive strength from VDDX (EVDD)
- High Voltage Input (HVI)
- Supply voltage sense with low battery warning
- On-chip temperature sensor, temperature value can be measured with ADC or can generate a high temperature warning
- Up to 23 pins can be used as keyboard wake-up interrupt (KWI)

1.4 Module Features

The following sections provide more details of the integrated modules.

1.4.1 S12Z Central Processor Unit (CPU)

The S12Z CPU is a revolutionary high-speed core, with code size and execution efficiencies over the S12X CPU. The S12Z CPU also provides a linear memory map eliminating the inconvenience and performance impact of page swapping.

- Harvard Architecture - parallel data and code access
- 3 stage pipeline
- 32-Bit wide instruction and databus
- 32-Bit ALU
- 24-bit addressing (16 MByte linear address space)

- Instructions and Addressing modes optimized for C-Programming & Compiler
  - MAC unit 32bit += 32bit*32bit
  - Hardware divider
  - Single cycle multi-bit shifts (Barrel shifter)
  - Special instructions for fixed point math
- Unimplemented opcode traps
- Unprogrammed byte value (0xFF) defaults to SWI instruction

1.4.1.1 Background Debug Controller (BDC)

- Background debug controller (BDC) with single-wire interface
  - Non-intrusive memory access commands
  - Supports in-circuit programming of on-chip nonvolatile memory

1.4.1.2 Debugger (DBG)

- Three comparators (A, B and D)
  - Comparator A compares the full address bus and full 32-bit data bus
  - Comparators B and D compare the full address bus only
  - Each comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)

1.4.2 Embedded Memory

1.4.2.1 Memory Access Integrity

- Illegal address detection
- ECC support on embedded NVM and system RAM