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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# Switching Amplifier

## FEATURES

- ◆ Low Cost Intelligent Switching Amplifier
- ◆ Directly Connects to Most Embedded Micro-controllers and Digital Signal Controllers
- ◆ Integrated Gate Driver Logic with Dead-time Generation and Shoot-through Prevention
- ◆ Wide Power Supply Range (8.5 V To 60 V)
- ◆ Over 10A Peak Output Current per Phase
- ◆ Independent Current Sensing for each Output
- ◆ User Programmable Cycle-by-cycle Current Limit Protection
- ◆ Over-Current and Over-Temperature Warning Signals

## APPLICATIONS

- ◆ Bidirectional DC Brush Motors
- ◆ 2 Unidirectional DC Brush Motors
- ◆ 2 Independent Solenoid Actuators
- ◆ Stepper Motors

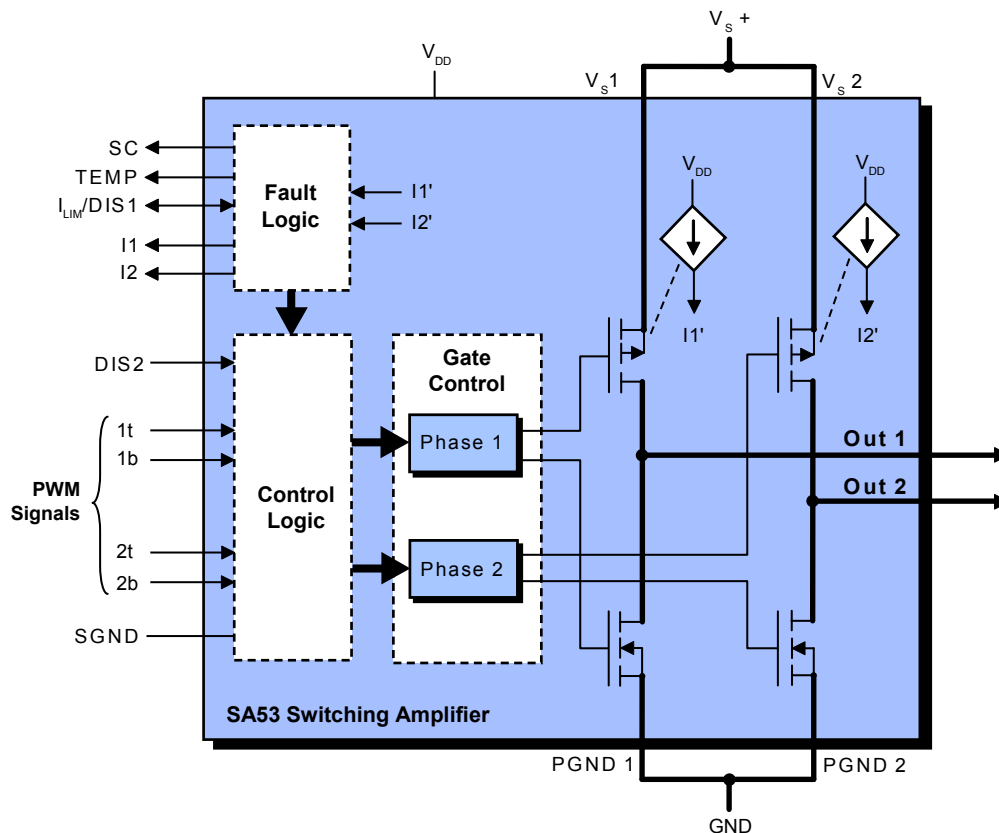
## DESCRIPTION

The SA53 is a fully integrated switching amplifier designed primarily to drive DC brush motors. Two independent half bridges provide over 10 amperes peak output current under microcontroller or DSC control. Thermal and short circuit monitoring is provided, which generates fault signals for the microcontroller to take appropriate action. A block diagram is provided in Figure 1.

Additionally, cycle-by-cycle current limit offers user programmable hardware protection independent of the microcontroller. Output current is measured using an innovative low loss technique. The SA53 is built using a multi-technology process allowing CMOS logic control and complementary DMOS output power devices on the same IC. Use of P-channel high side FETs enables 60V operation without bootstrap or charge pump circuitry.

The HSOP surface mount package balances excellent thermal performance with the advantages of a low profile surface mount package.

**FIGURE 1. BLOCK DIAGRAM**



## 1. CHARACTERISTICS AND SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| Parameter                             | Symbol    | Min    | Max              | Units |
|---------------------------------------|-----------|--------|------------------|-------|
| SUPPLY VOLTAGE                        | $V_S$     |        | 60               | V     |
| SUPPLY VOLTAGE                        | $V_{DD}$  |        | 5.5              | V     |
| LOGIC INPUT VOLTAGE                   |           | (-0.5) | ( $V_{DD}+0.5$ ) | V     |
| OUTPUT CURRENT, peak, 10ms (NOTE 2)   | $I_{OUT}$ |        | 10               | A     |
| POWER DISSIPATION, avg, 25°C (NOTE 2) | $P_D$     |        | 100              | W     |
| TEMPERATURE, solder, 10sec            | $T_S$     |        | 260              | °C    |
| TEMPERATURE, junction (NOTE 2)        | $T_J$     |        | 150              | °C    |
| TEMPERATURE RANGE, storage            | $T_{STG}$ | -55    | +125             | °C    |
| OPERATING TEMPERATURE, case           | $T_A$     | -25    | +85              | °C    |

### SPECIFICATIONS

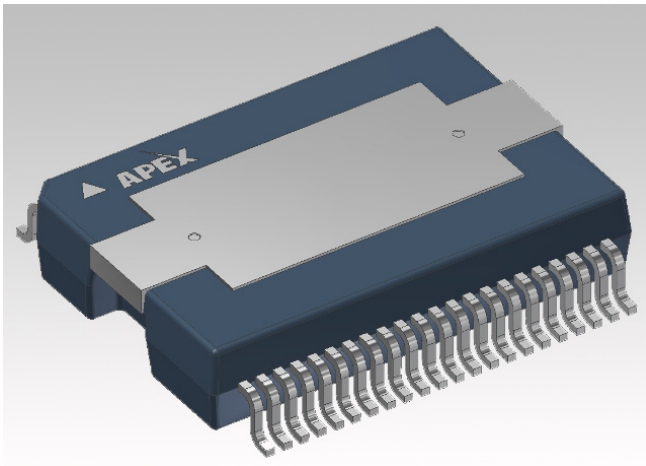
| PARAMETER                                  | TEST CONDITIONS (Note 1)   | MIN  | TYP  | MAX | UNITS |
|--|--|------|------|-----|-------|
| <b>LOGIC</b>                               |  |      |      |     |       |
| INPUT LOW                                  |  |      |      | 1   | V     |
| INPUT HIGH                                 |  | 1.8  |      |     | V     |
| OUTPUT LOW                                 |  |      |      | 0.3 | V     |
| OUTPUT HIGH                                |  | 3.7  |      |     | V     |
| OUTPUT CURRENT (SC, Temp, $I_{LIM}/DIS1$ ) |  |      | 50   |     | mA    |
| <b>POWER SUPPLY</b>                        |  |      |      |     |       |
| $V_S$                                      |  | UVLO | 50   | 60  | V     |
| $V_S$ UNDERVOLTAGE LOCKOUT, (UVLO)         |  |      | 8.3  |     | V     |
| $V_{DD}$                                   |  | 4.5  |      | 5.5 | V     |
| SUPPLY CURRENT, $V_S$                      | 20 kHz (One phase switching at 50% duty cycle) , $V_S=50V$ , $V_{DD}=5V$   |      | 25   | 30  | mA    |
| SUPPLY CURRENT, $V_{DD}$                   | 20 kHz (One phase switching at 50% duty cycle) , $V_S=50V$ , $V_{DD}=5.5V$ |      | 5    | 6.5 | mA    |
| <b>CURRENT LIMIT</b>                       |  |      |      |     |       |
| CURRENT LIMIT THRESHOLD (Vth)              |  |      | 3.75 |     | V     |
| Vth HYSTERESIS                             |  |      | 100  |     | mV    |
| <b>OUTPUT</b>                              |  |      |      |     |       |
| CURRENT, CONTINUOUS                        | 25°C Case Temperature  | 3    |      |     | A     |
| RIISING DELAY, TD (RIISE)                  | See Figure 10  |      | 270  |     | ns    |
| FALLING DELAY, TD (FALL)                   | See Figure 10  |      | 270  |     | ns    |
| DISABLE DELAY, TD (DIS)                    | See Figure 10  |      | 200  |     | ns    |
| ENABLE DELAY, TD ( $\overline{DIS}$ )      | See Figure 10  |      | 200  |     | ns    |
| RIISE TIME, T (RIISE)                      | See Figure 11  |      | 50   |     | ns    |
| FALL TIME, T (FALL)                        | See Figure 11  |      | 50   |     | ns    |
| ON RESISTANCE SOURCING (P-CHANNEL)         | 3A Load  |      | 400  |     | mΩ    |
| ON RESISTANCE SINKING (N-CHANNEL)          | 3A Load  |      | 400  |     | mΩ    |

**SPECIFICATIONS, continued**

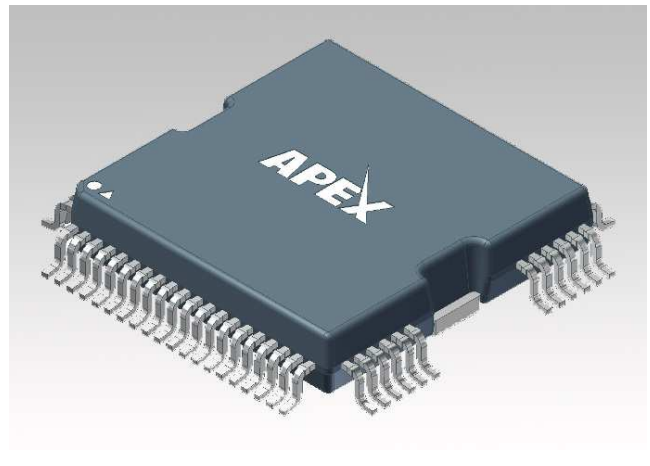
| PARAMETER                    | TEST CONDITIONS (Note 1) | MIN | TYP  | MAX | UNITS |
|------------------------------|--------------------------|-----|------|-----|-------|
| <b>THERMAL</b>               |                          |     |      |     |       |
| THERMAL WARNING              |                          |     | 135  |     | °C    |
| THERMAL WARNING HYSTERESIS   |                          |     | 40   |     | °C    |
| RESISTANCE, junction to case | Full temperature range   |     | 1.25 | 1.5 | °C/W  |
| TEMPERATURE RANGE, case      | Meets Specifications     | -25 |      | +85 | °C    |

NOTES:

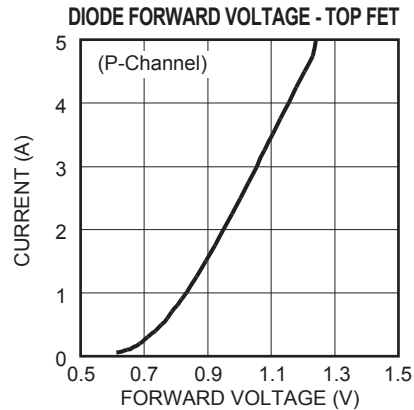
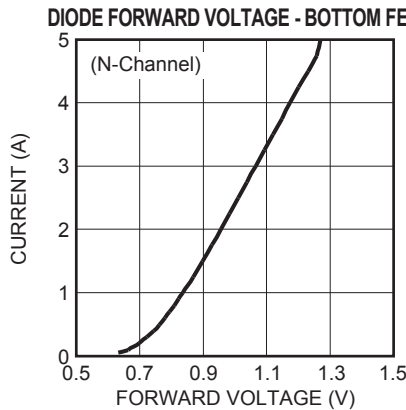
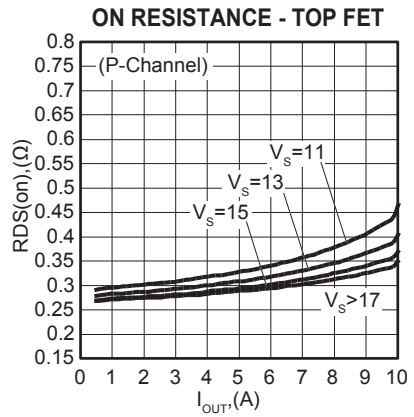
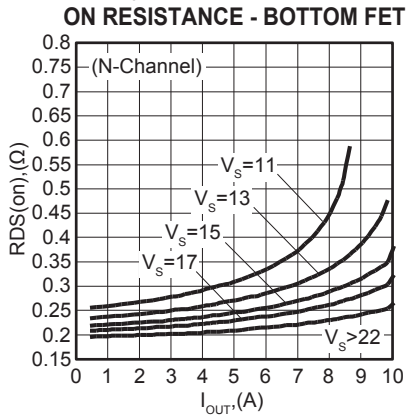
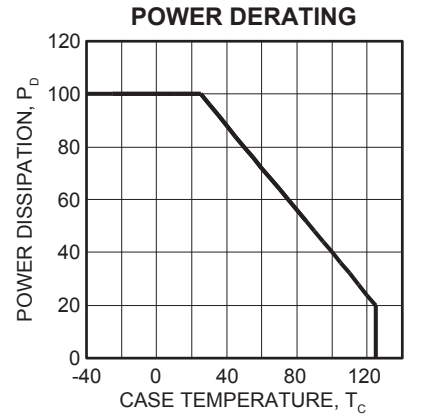
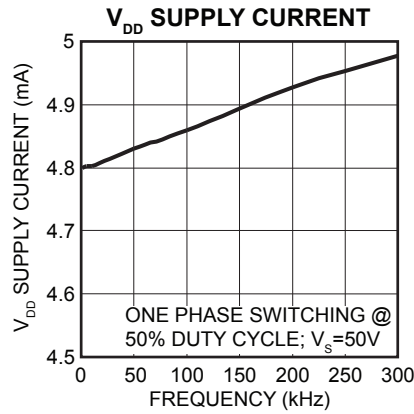
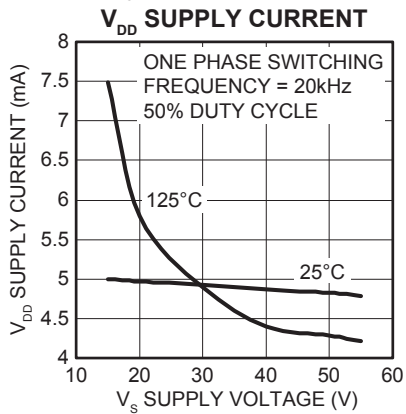
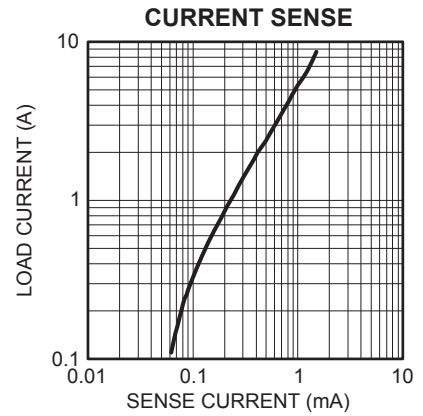
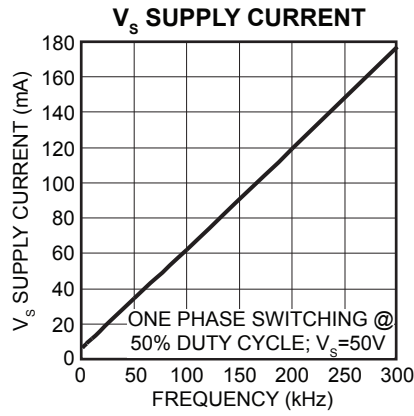
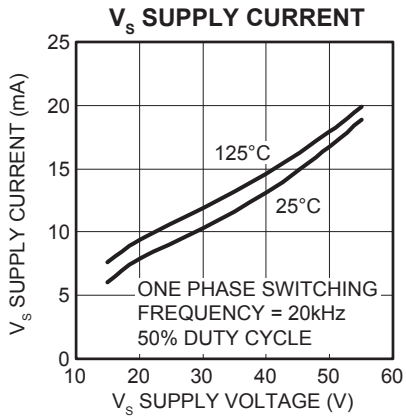
1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and  $T_c = 25^\circ\text{C}$ ).
2. Long term operation at elevated temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTBF.
3. Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of  $150^\circ\text{C}$ .



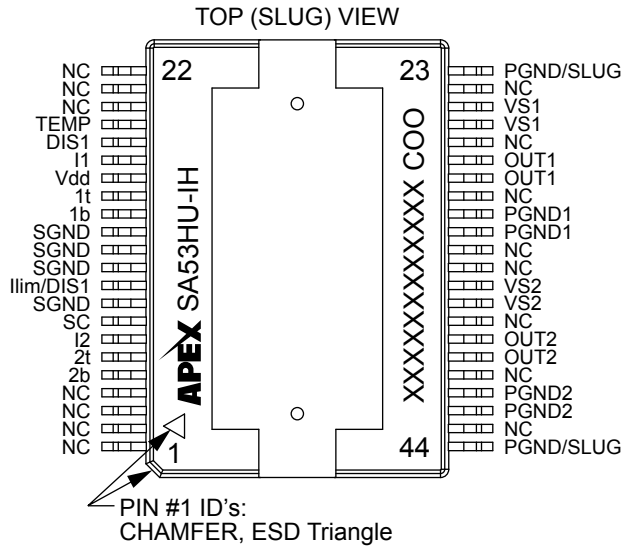
**FIGURE 2A.**  
44-pin HSOP Slug Up, Package Style HU



**FIGURE 2B.**  
64-pin QFP, Package Style HQ



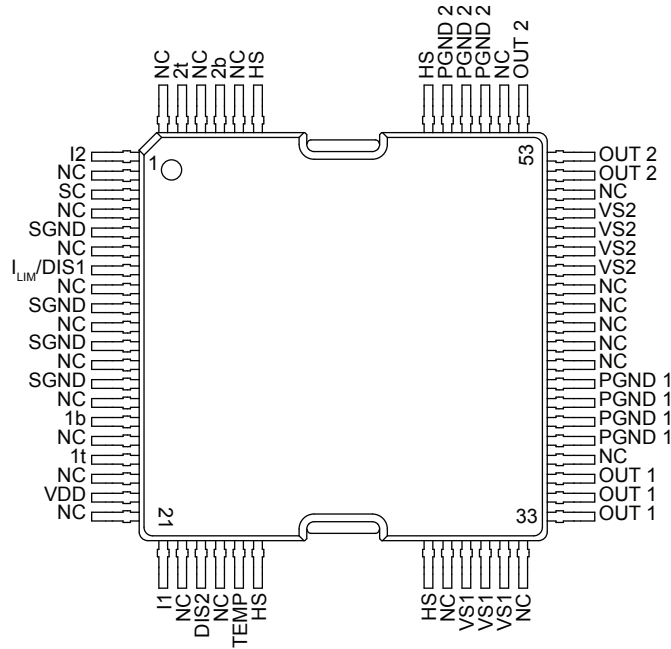
**FIGURE 3A. EXTERNAL CONNECTIONS - 44-pin HSOP**



**TABLE 1A. PIN DESCRIPTIONS - 44-pin HSOP**

| Pin #  | Pin Name        | Signal Type        | Simplified Pin Description  |
|--|-----------------|--------------------|---|
| 25,26  | $V_s$ (phase 1) | Power              | High Voltage Supply (8.5-60V) supplies phase 1 only   |
| 38,39  | OUT 2           | Power Output       | Half Bridge 2 Power Output  |
| 41,42  | PGND (phase 2)  | Power              | High Current GND Return Path for Power Output 2   |
| 8  | SC              | Logic Output       | Indication of a short of an output to supply, GND or another phase  |
| 5  | 2b              | Logic Input        | Logic high commands 2 phase lower FET to turn on  |
| 6  | 2t              | Logic Input        | Logic high commands 2 phase upper FET to turn on  |
| 7  | I2              | Analog Output      | Phase 2 current sense output  |
| 10   | $I_{LIM}/DIS1$  | Logic Input/Output | As an output, logic high indicates cycle-by-cycle current limit, and logic low indicates normal operation. As an input, logic high places all outputs in a high impedance state and logic low disables the cycle-by-cycle current limit function. |
| 9,11,12,13   | SGND            | Power              | Analog and digital GND – internally connected to PGND   |
| 14   | 1b              | Logic Input        | Logic high commands 1 phase lower FET to turn on  |
| 15   | 1t              | Logic Input        | Logic high commands 1 phase upper FET to turn on  |
| 16   | $V_{DD}$        | Power              | Logic Supply (5V)   |
| 17   | I1              | Analog Output      | Phase 1 current sense output  |
| 18   | DIS2            | Logic Input        | Logic high places all outputs in a high impedance state   |
| 19   | TEMP            | Logic Output       | Thermal indication of die temperature above 135°C   |
| 35,36  | $V_s$ (phase 2) | Power              | High Voltage Supply phase 2   |
| 28,29  | OUT 1           | Power Output       | Half Bridge 1 Power Output  |
| 31,32  | PGND (phase 1)  | Power              | High Current GND Return Path for Power Outputs 1 & 2  |
| 23,44  | HS              | Mechanical         | Pins connected to the package heat slug   |
| 1,2,3,4,20,<br>21,22,24,27,<br>30,33,34,37,<br>40,43 | NC              | ---                | Do Not Connect  |

**FIGURE 3B. EXTERNAL CONNECTIONS - 64-pin QFP**



**TABLE 1B. PIN DESCRIPTIONS - 64-pin QFP**

| Pin #  | Pin Name                 | Signal Type        | Simplified Pin Description  |
|--|--------------------------|--------------------|---|
| 29,30,31   | V <sub>s</sub> (phase 1) | Power              | High Voltage Supply (8.5-60V) supplies phase 1 only   |
| 51,52,53   | OUT 2                    | Power Output       | Half Bridge 2 Power Output  |
| 55,56,57   | PGND (phase 2)           | Power              | High Current GND Return Path for Power Output 2   |
| 3  | SC                       | Logic Output       | Indication of a short of an output to supply, GND or another phase  |
| 61   | 2b                       | Logic Input        | Logic high commands 2 phase lower FET to turn on  |
| 63   | 2t                       | Logic Input        | Logic high commands 2 phase upper FET to turn on  |
| 1  | I2                       | Analog Output      | Phase 2 current sense output  |
| 7  | I <sub>LIM</sub> /DIS1   | Logic Input/Output | As an output, logic high indicates cycle-by-cycle current limit, and logic low indicates normal operation. As an input, logic high places all outputs in a high impedance state and logic low disables the cycle-by-cycle current limit function. |
| 5,9,11,13  | SGND                     | Power              | Analog and digital GND – internally connected to PGND   |
| 15   | 1b                       | Logic Input        | Logic high commands 1 phase lower FET to turn on  |
| 17   | 1t                       | Logic Input        | Logic high commands 1 phase upper FET to turn on  |
| 19   | V <sub>DD</sub>          | Power              | Logic Supply (5V)   |
| 21   | I1                       | Analog Output      | Phase 1 current sense output  |
| 23   | DIS2                     | Logic Input        | Logic high places all outputs in a high impedance state   |
| 25   | TEMP                     | Logic Output       | Thermal indication of die temperature above 135°C   |
| 46,47,48,49  | V <sub>s</sub> (phase 2) | Power              | High Voltage Supply phase 2   |
| 33,34,35   | OUT 1                    | Power Output       | Half Bridge 1 Power Output  |
| 37,38,39,40  | PGND (phase 1)           | Power              | High Current GND Return Path for Power Outputs 1 & 2  |
| 26,27,58,59  | HS                       | Mechanical         | Pins connected to the package heat slug   |
| 2,4,6,8,10,<br>12,14,16,18,<br>20,22,24,28,<br>32,36,41,42,<br>43,44,45,50,<br>54,60,62,64 | NC                       | ---                | Do Not Connect  |

## 1.2 Pin Descriptions

**V<sub>S</sub>**: Supply voltage for the output transistors. These pins require decoupling (1μF capacitor with good high frequency characteristics is recommended) to the PGND pins. The decoupling capacitor should be located as close to the V<sub>S</sub> and PGND pins as possible. Additional capacitance will be required at the V<sub>S</sub> pins to handle load current peaks and potential motor regeneration. Refer to the applications section of this datasheet for additional discussion regarding bypass capacitor selection. Note that V<sub>S</sub> pins 29-31 carry only the phase 1 supply current. Pins 46-49 carry supply current for phase 2. Phase 1 may be operated at a different supply voltage from phase 2. Both V<sub>S</sub> voltages are monitored for undervoltage conditions.

**OUT 1, OUT 2**: These pins are the power output connections to the load. NOTE: When driving an inductive load, it is recommended that two Schottky diodes with good switching characteristics (fast t<sub>RR</sub> specs) be connected to each pin so that they are in parallel with the parasitic back-body diodes of the output FETs. (See Section 2.6)

**PGND**: Power Ground. This is the ground return connection for the output FETs. Return current from the load flows through these pins. PGND is internally connected to SGND through a resistance of a few ohms. See section 2.1 of this datasheet for more details.

**SC**: Short Circuit output. If a condition is detected on any output which is not in accordance with the input commands, this indicates a short circuit condition and the SC pin goes high. The SC signal is blanked for approximately 200ns during switching transitions but in high current applications, short glitches may appear on the SC pin. A high state on the SC output will not automatically disable the device. The SC pin includes an internal 12kΩ series resistor.

**1b, 2b**: These Schmitt triggered logic level inputs are responsible for turning the associated bottom, or lower N-channel output FETs on and off. Logic high turns the bottom N-channel FET on, and a logic low turns the low side N-channel FET off. If 2b or 2b is high at the same time that a corresponding 1t or 2t input is high, protection circuitry will turn off both FETs in order to prevent shoot-through on that output phase. Protection circuitry also includes a dead-time generator, which inserts dead time in the outputs in the case of simultaneous switching of the top and bottom input signals.

**1t, 2t**: These Schmitt triggered logic level inputs are responsible for turning the associated top side, or upper P-channel FET outputs on and off. Logic high turns the top P-channel FET on, and a logic low turns the top P-channel FET off.

**I1, I2**: Current sense pins. The SA53 supplies a positive current to these pins which is proportional to the current flowing through the top side P-channel FET for that phase. Commutating currents flowing through the backbody diode of the P-channel FET or through external Schottky diodes are not registered on the current sense pins. Nor do currents flowing through the low side N-channel FET, in either direction, register at the current sense pins. A resistor connected from a current sense pin to SGND creates a voltage signal representation of the phase current that can be monitored with ADC inputs of a processor or external circuitry.

The current sense pins are also internally compared with the current limit threshold voltage reference, V<sub>th</sub>. If the voltage on any current sense pin exceeds V<sub>th</sub>, the cycle by cycle current limit circuit engages. Details of this functionality are described in the applications section of this datasheet.

**I<sub>LIM</sub>/DIS1**: This pin is directly connected to the disable circuitry of the SA53. Pulling this pin to logic high places OUT 1 and OUT 2 in a high impedance state. This pin is also connected internally to the output of the current limit latch through a 12kΩ resistor and can be monitored to observe the function of the cycle-by-cycle current limit feature. Pulling this pin to a logic low effectively disables the cycle-by-cycle current limit feature.

**SGND**: This is the ground return connection for the V<sub>DD</sub> logic power supply pin. All internal analog and logic circuitry is referenced to this pin. PGND is internally connected to GND through a resistance of a few ohms,. However, it is highly recommended to connect the GND pin to the PGND pins externally as close to the device as possible. Failure do to this may result in oscillations on the output pins during rising or falling edges.

**V<sub>DD</sub>**: This is the connection for the 5V power supply, and provides power for the logic and analog circuitry in the SA53. This pin requires decoupling (at least 0.1μF capacitor with good high frequency characteristics is recommended) to the SGND pin.

**DIS2**: The DIS2 pin is a Schmitt triggered logic level input that places OUT 1 and OUT 2 in a high impedance state when pulled high. DIS2 has an internal 12kΩ pull-down resistor and may therefore be left unconnected.



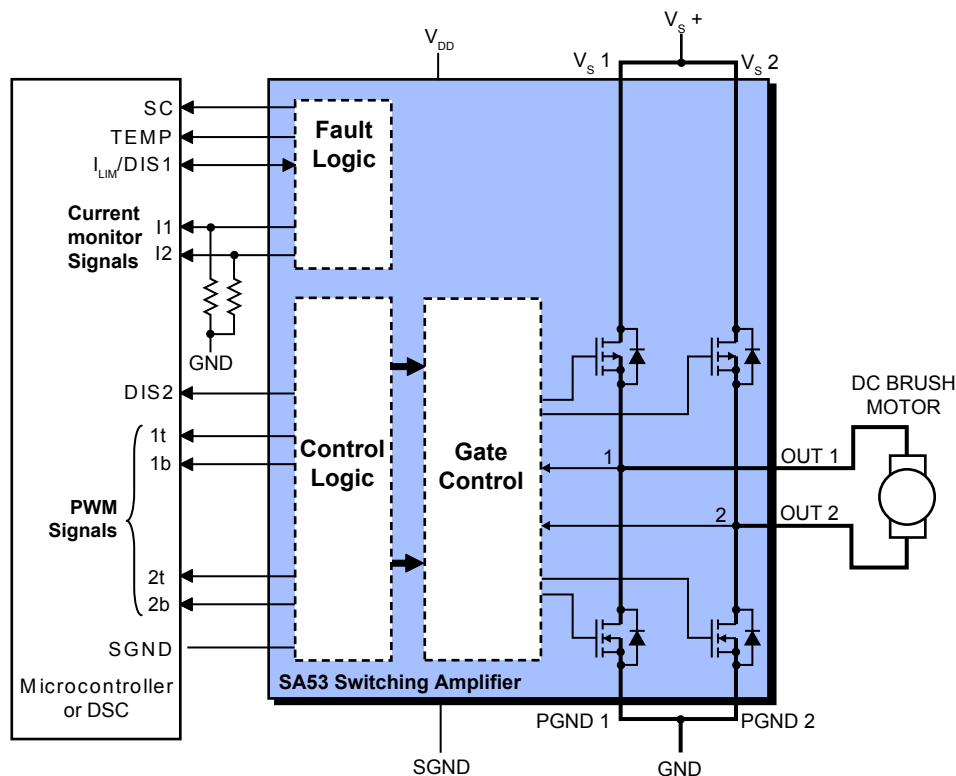
**TEMP:** This logic level output goes high when the die temperature of the SA53 reaches approximately 135°C. This pin WILL NOT automatically disable the device. The TEMP pin includes a 12kΩ series resistor.

**HS:** These pins are internally connected to the thermal slug on the reverse of the package. They should be connected to GND. Neither the heat slug nor these pins should be used to carry high current.

**NC:** These “no-connect” pins should be left unconnected.

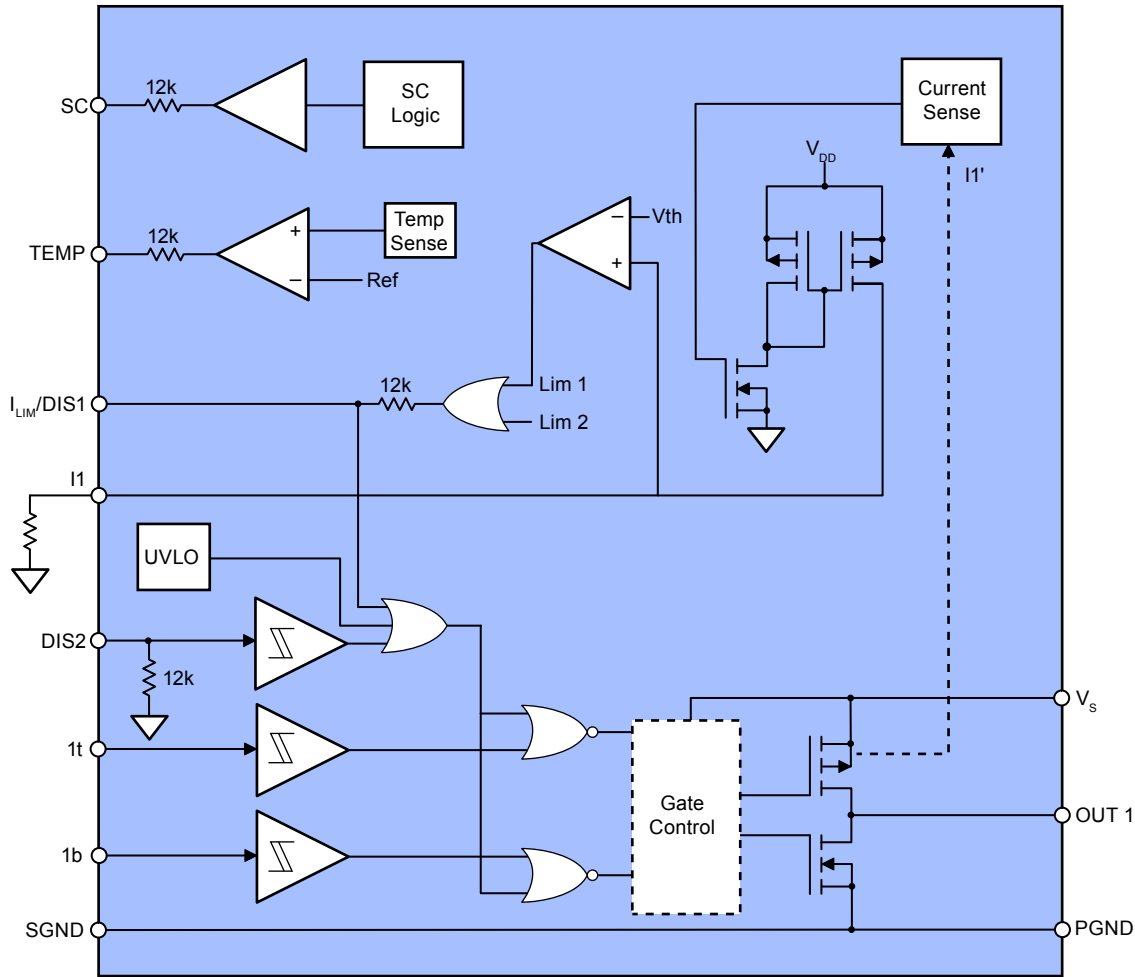
## 2. SA53 OPERATION

The SA53 is designed primarily to drive DC brush motors. However, it can be used for any application requiring two high current outputs. The signal set of the SA53 is designed specifically to interface with a DSP or microcontroller. A typical system block diagram is shown in the figure below. Over-temperature, Short-Circuit and Current Limit fault signals provide important feedback to the system controller which can safely disable the output drivers in the presence of a fault condition. High side current monitors for both phases provide performance information which can be used to regulate or limit torque.



**FIGURE 4. SYSTEM DIAGRAM**

The block diagram in Figure 5 illustrates the features of the input and output structures of the SA53. For simplicity, a single phase is shown.



**FIGURE 5. INPUT AND OUTPUT STRUCTURES FOR A SINGLE PHASE**

| TABLE 2. TRUTH TABLE |        |                                 |                        |      |                          |  |
|----------------------|--------|---------------------------------|------------------------|------|--------------------------|--|
| 1t, 2t               | 1b, 2b | I <sub>1</sub> , I <sub>2</sub> | I <sub>LIM</sub> /DIS1 | DIS2 | OUT 1<br>OUT 2           | Comments   |
| 0                    | 0      | X                               | X                      | X    | High-Z                   | Top and Bottom output FETs for that phase are turned off.  |
| 0                    | 1      | <V <sub>th</sub>                | 0                      | 0    | PGND                     | Bottom output FET for that phase is turned on.   |
| 1                    | 0      | <V <sub>th</sub>                | 0                      | 0    | V <sub>s</sub>           | Top output FET for that phase is turned on.  |
| 1                    | 1      | X                               | X                      | X    | High-Z                   | Both output FETs for that phase are turned off.  |
| X                    | X      | >V <sub>th</sub>                | 1                      | X    | High-Z                   | Voltage on I1 or I2 has exceeded V <sub>th</sub> , which causes I <sub>LIM</sub> /DIS1 to go high. This internally disables Top and Bottom output FETs for ALL phases. |
| X                    | X      | X                               | X                      | 1    | High-Z                   | DIS2 pin pulled high, which disables all outputs.  |
| X                    | X      | X                               | Pulled High            | X    | High-Z                   | Pulling the I <sub>LIM</sub> /DIS1 pin high externally acts as a second disable input, which disables ALL output FETs.   |
| X                    | X      | X                               | Pulled Low             | 0    | Determined by PWM inputs | Pulling the DIS2 pin low externally disables the cycle-by-cycle current limit function. The state of the outputs is strictly a function of the PWM inputs.             |
| X                    | X      | X                               | X                      | X    | High-Z                   | If V <sub>s</sub> is below the UVLO threshold all output FETs will be disabled.  |

## 2.1 LAYOUT CONSIDERATIONS

Output traces carry signals with very high  $dV/dt$  and  $dI/dt$ . Proper routing and adequate power supply bypassing ensures normal operation. Poor routing and bypassing can cause erratic and low efficiency operation as well as ringing at the outputs.

The  $V_S$  supply should be bypassed with a surface mount ceramic capacitor mounted as close as possible to the  $V_S$  pins. Total inductance of the routing from the capacitor to the  $V_S$  and GND pins must be kept to a minimum to prevent noise from contaminating the logic control signals. A low ESR capacitor of at least  $25\mu F$  per ampere of output current should be placed near the SA53 as well. Capacitor types rated for switching applications are the only types that should be considered.

The bypassing requirements of the  $V_{DD}$  supply are less stringent, but still necessary. A  $0.1\mu F$  to  $0.47\mu F$  surface mount ceramic capacitor (X7R or NPO) connected directly to the  $V_{DD}$  pin is sufficient.

SGND and PGND pins are connected internally. However, these pins must be connected externally in such a way that there is no motor current flowing in the logic and signal ground traces as parasitic resistances in the small signal routing can develop sufficient voltage drops to erroneously trigger input transitions. Alternatively, a ground plane may be separated into power and logic sections connected by a pair of back to back Schottky diodes. This isolates noise between signal and power ground traces and prevents high currents from passing between the plane sections.

Unused area on the top and bottom PCB planes should be filled with solid or hatched copper to minimize inductive coupling between signals. The copper fill may be left unconnected, although a ground plane is recommended.

## 2.2 FAULT INDICATIONS

In the case of either an over-temperature or short circuit fault, the SA53 will take no action to disable the outputs. Instead, the SC and TEMP signals are provided to an external controller, where a determination can be made regarding the appropriate course of action. In most cases, the SC pin would be connected to a FAULT input on the processor, which would immediately disable its PWM outputs. The TEMP fault does not require such an immediate response, and would typically be connected to a GPIO, or Keyboard Interrupt pin of the processor. In this case, the processor would recognize the condition as an external interrupt, which could be processed in software via an Interrupt Service Routine. The processor could optionally bring all inputs low, or assert a high level to either of the disable inputs on the SA53.

Figure 6 shows an external SR flip-flop which provides a hard wired shutdown of all outputs in response to a fault indication. An SC or TEMP fault sets the latch, pulling the disable pin high. The processor clears the latched condition with a GPIO. This circuit can be used in safety critical applications to remove software from the fault-shutdown loop, or simply to reduce processor overhead.

In applications which may not have available GPIO, the TEMP pin may be externally connected to the adjacent DIS1 pin. If the device temperature reaches  $\sim 135^\circ C$  all outputs will be disabled, de-energizing the motor. The SA53 will re-energize the motor when the device temperature falls below approximately  $95^\circ C$ . The TEMP pin hysteresis is wide to reduce the likelihood of thermal oscillations which can greatly reduce the life of the device.

## 2.3 UNDER-VOLTAGE LOCKOUT

The undervoltage lockout condition results in the SA53 unilaterally disabling all output FETs until  $V_S$  is above the UVLO threshold indicated in the spec table. There is no external signal indicating that an undervoltage lockout condition is in progress. The SA53 has two  $V_S$  connections: one for phase 1 and another for phase 2. The supply voltages on these pins need not be the same, but the UVLO will engage if either is below the threshold. Hysteresis on the UVLO circuit prevents oscillations with typical power supply variations.

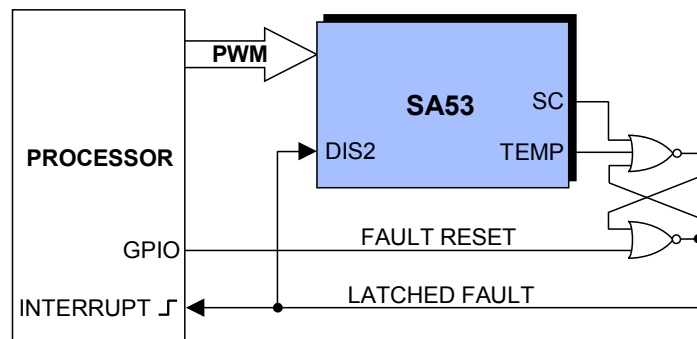


FIGURE 6. EXTERNAL FAULT LATCH CIRCUIT

## 2.4 CURRENT SENSE

External power shunt resistors are not required with the SA53. Forward current in each top, P-channel output FET is measured and mirrored to the respective current sense output pin, Ia, Ib and Ic. By connecting a resistor between each current sense pin and a reference, such as ground, a voltage develops across the resistor that is proportional to the output current for that phase. An ADC can monitor the voltages on these resistors for protection or for closed loop torque control in some application configurations. The current sense pins source current from the  $V_{DD}$  supply. Headroom required for the current sense circuit is approximately 0.5V. The nominal scale factor for each proportional output current is shown in the typical performance plot on page 4 of this datasheet.

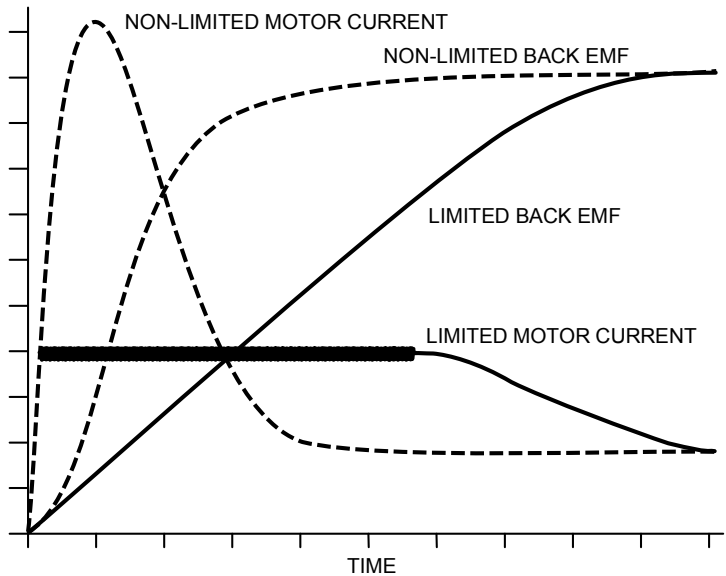
## 2.5 CYCLE-BY-CYCLE CURRENT LIMIT

In applications where the current in the motor is not directly controlled, both the average current rating of the motor and the inrush current must be considered when selecting a proper amplifier. For example, a 1A continuous motor might require a drive amplifier that can deliver well over 10A peak in order to survive the inrush condition at startup.

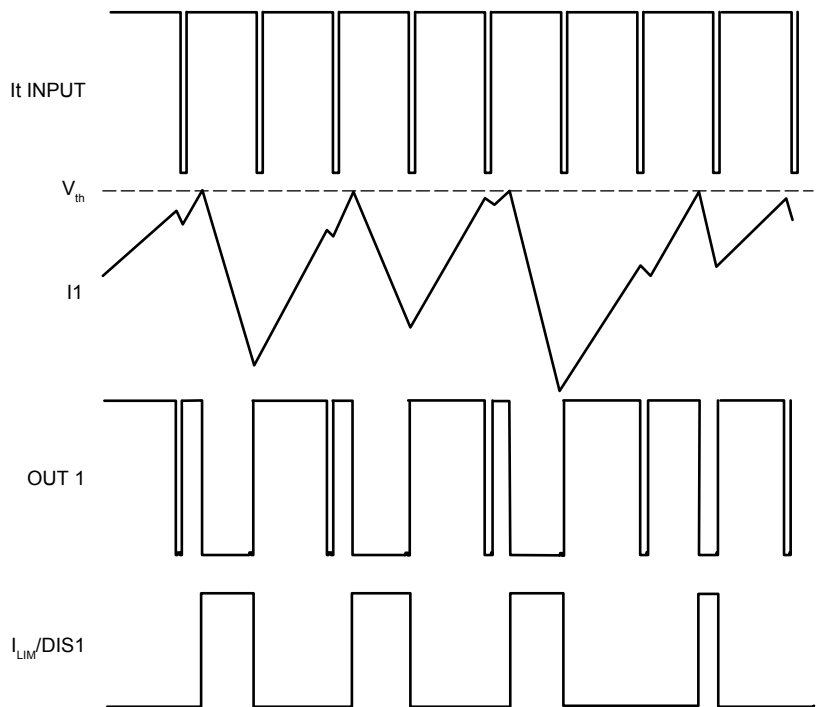
Because the output current of each upper output FET is measured, the SA53 is able to provide a very robust current limit scheme. This enables the SA53 to safely and easily drive virtually any DC brush motor through a startup inrush condition. With limited current, the starting torque and acceleration are also limited. The plot in Figure 7 shows starting current and back EMF with and without current limit enabled.

If the voltage of any of the two current sense pins exceeds the current limit threshold voltage ( $V_{th}$ ), all outputs are disabled. After all current sense pins fall below the  $V_{th}$  threshold voltage AND the offending phase's top side input goes low, the output stage will return to an active state on the rising edge of ANY top side input command signal ( $1t$  or  $2t$ ). With most commutation schemes, the current limit will reset each pwm cycle. This scheme regulates the peak current in each phase during each pwm cycle as illustrated in the timing diagram below. The ratio of average to peak current depends on the inductance of the motor winding, the back EMF developed in the motor, and the width of the pulse.

Figure 8 illustrates the current limit trigger and reset sequence. Current limit engages and  $I_{LIM}/DIS1$  goes high when any current sense pin exceeds  $V_{th}$ . Notice that the moment at which the current sense signal exceeds the  $V_{th}$  threshold is asynchronous with respect to the input PWM signal. The difference between the PWM period and the motor winding L/R time constant will



**FIGURE 7. START-UP VOLTAGE AND CURRENT**



**FIGURE 8. CURRENT LIMIT WAVEFORMS**

often result in an audible beat frequency sometimes called a sub-cycle oscillation.

This oscillation can be seen on the  $I_{LIM}/DIS1$  pin waveform in Figure 8. Input signals commanding 0% or 100% duty cycle may be incompatible with the current limit feature due to the absence of rising edges of 1t and 2t except when commutating phases. At high RPM, this may result in poor performance. At low RPM, the motor may stall if the current limit trips and the motor current reaches zero without a commutation edge which will typically reset the current limit latch.

The current limit feature may be disabled by tying the  $I_{LIM}/DIS1$  pin to GND. The current sense pins will continue to provide top FET output current information.

Typically, the current sense pins source current into grounded resistors which provide voltages to the current limit comparators. If instead the current limit resistors are connected to a voltage output DAC, the current limit can be controlled dynamically from the system controller. This technique essentially reduces the current limit threshold voltage to  $(V_{th}-VDAC)$ . During expected conditions of high torque demand, such as start-up or reversal, the DAC can adjust the current limit dynamically to allow periods of high current. In normal operation when low current is expected, the DAC output voltage can increase, reducing the current limit setting to provide more conservative fault protection.

### 2.6 EXTERNAL FLYBACK DIODES

External fly-back diodes will offer superior reverse recovery characteristics and lower forward voltage drop than the internal back-body diodes. In high current applications, external flyback diodes can reduce power dissipation and heating during commutation of the motor current. Reverse recovery time and capacitance are the most important parameters to consider when selecting these diodes. Ultra-fast rectifiers offer better reverse recovery time and Schottky diodes typically have low capacitance. Individual application requirements will be the guide when determining the need for these diodes and for selecting the component which is most suitable.

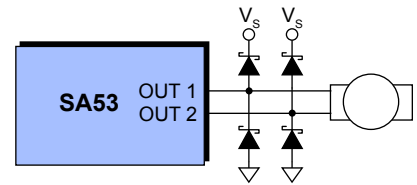


FIGURE 9. SCHOTTKY DIODES

### 3. POWER DISSIPATION

The thermally enhanced package of the SA53 allows several options for managing the power dissipated in the three output stages. Power dissipation in traditional PWM applications is a combination of output power dissipation and switching losses. Output power dissipation depends on the quadrant of operation and whether external flyback diodes are used to carry the reverse or commutating currents. Switching losses are dependent on the frequency of the PWM cycle as described in the typical performance graphs.

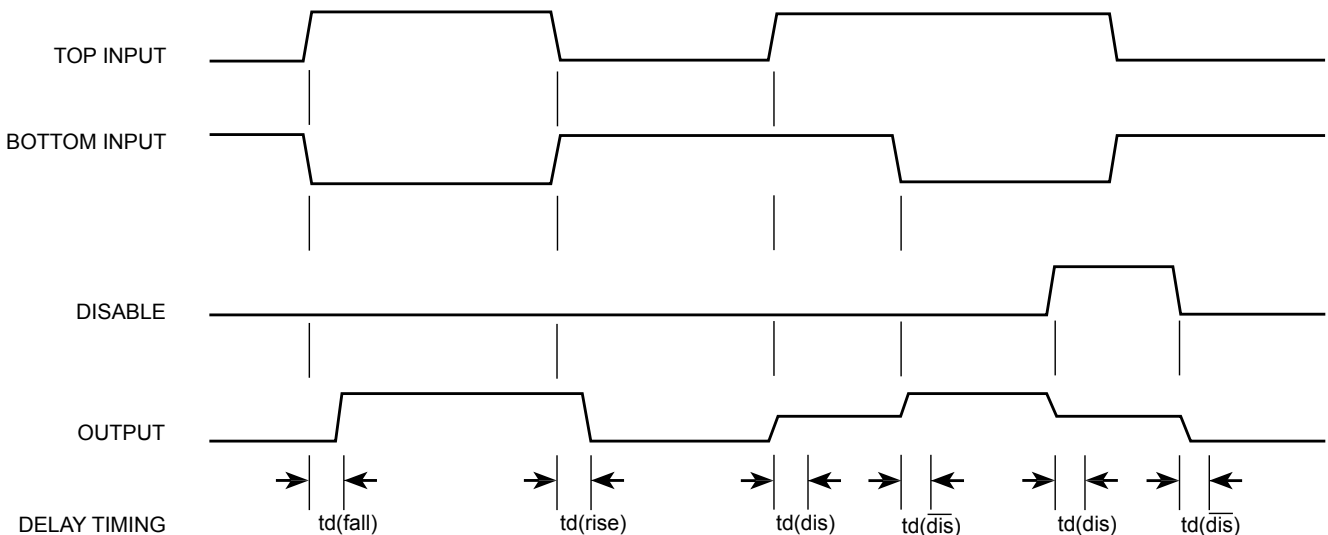
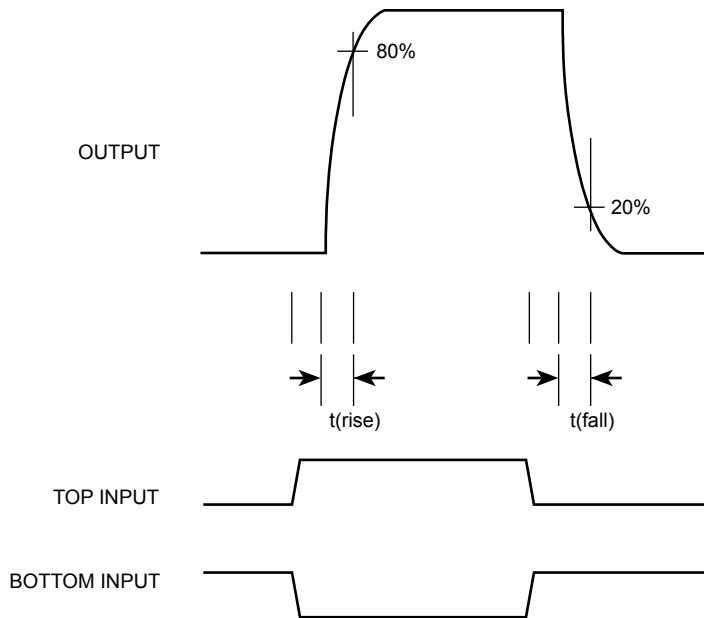


FIGURE 10. TIMING DIAGRAMS



**FIGURE 11. OUTPUT RESPONSE**

#### 4. ORDERING AND PRODUCT STATUS INFORMATION

| MODEL     | TEMPERATURE | PACKAGE                                       | PRODUCTION STATUS   |
|-----------|-------------|---|---------------------|
| SA53-IHZ  | -25 to 85°C | 64 pin Power QFP (HQ package drawing)         | Not for New Designs |
| SA53HU-IH | -25 to 85°C | 44 pin Power SOP-Slug Up (HU package drawing) | Samples Available   |

#### CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.

For inquiries via email, please contact [apex.support@cirrus.com](mailto:apex.support@cirrus.com).

International customers can also request support by contacting their local Cirrus Logic Sales Representative.

To find the one nearest to you, go to [www.cirrus.com](http://www.cirrus.com)

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