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SA639

Low voltage mixer FM IF system with filter amplifier and data switch

Rev. 4 — 10 July 2014 Product data sheet

1. General description

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two wideband limiting intermediate frequency amplifiers, quadrature detector, logarithmic Received Signal Strength Indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin Shrink Small Outline Package).

The SA639 was designed for high-bandwidth portable communication applications and functions down to 2.7 V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1 MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low-pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a Power-down mode which powers down the device when pin 8 (POWER_DOWN_CTRL) is HIGH. Power down logic levels are CMOS and TTL compatible with high input impedance.

2. Features and benefits

- V_{CC} = 2.7 V to 5.5 V
- Low power consumption: 8.6 mA (typical) at 3 V
- Wideband data output (1 MHz minimum)
- Fast RSSI rise and fall times
- Mixer input to >500 MHz
- Mixer conversion power gain of 9.2 dB and noise figure of 11 dB at 110 MHz
- XTAL oscillator effective to 150 MHz (L.C. oscillator to 1 GHz local oscillator can be injected)
- 92 dB of IF amplifier/limiter power gain
- 25 MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80 dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch

- Excellent sensitivity: 2.24 μV into 50 Ω matching network for 10 dB S/N (Signal-to-Noise ratio) with RF at 110 MHz and IF at 9.8 MHz
- ESD hardened
- Power-down mode

3. Applications

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
SA639DH/01	SA639DH	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SA639DH/01	SA639DH/01,112	TSSOP24	Standard marking *IC's tube - DSC bulk pack	1575	T_{amb} = −40 °C to +85 °C
	SA639DH/01,118	TSSOP24	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

5. Block diagram

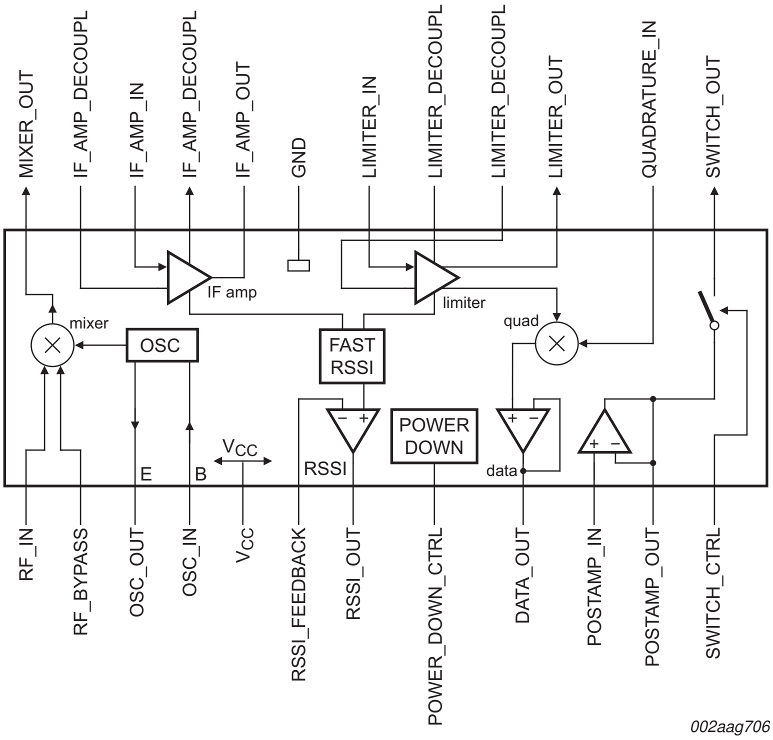


Fig 1. Block diagram of SA639

6. Pinning information

6.1 Pinning

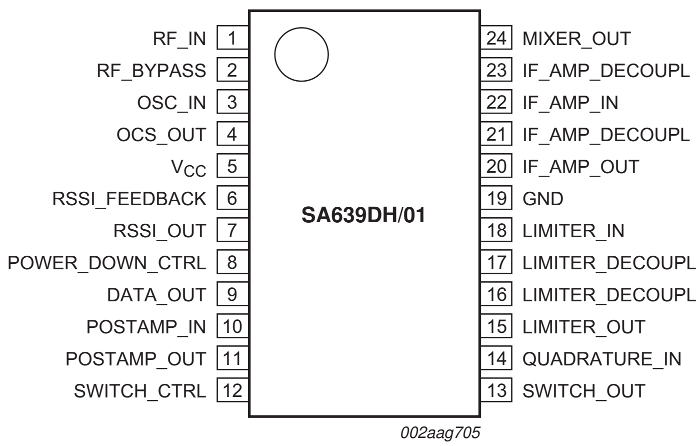


Fig 2. Pin configuration for TSSOP24

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
RF_IN	1	RF input
RF_BYPASS	2	RF bypass
OSC_OUT	3	oscillator output (emitter)
OSC_IN	4	oscillator input (base)
V_{CC}	5	positive supply voltage
RSSI_FEEDBACK	6	RSSI amplifier negative feedback terminal
RSSI_OUT	7	RSSI output
POWER_DOWN_CTRL	8	power-down control; active HIGH
DATA_OUT	9	data output
POSTAMP_IN	10	postamplifier input
POSTAMP_OUT	11	postamplifier output
SWITCH_CTRL	12	switch control
SWITCH_OUT	13	switch output
QUADRATURE_IN	14	quadrature input
LIMITER_OUT	15	limiter output
LIMITER_DECOUPL	16	limiter amplifier decoupling pin
LIMITER_DECOUPL	17	limiter amplifier decoupling pin
LIMITER_IN	18	limiter amplifier input
GND	19	ground; negative supply
IF_AMP_OUT	20	IF amplifier output
IF_AMP_DECOUPL	21	IF amplifier decoupling pin
IF_AMP_IN	22	IF amplifier input
IF_AMP_DECOUPL	23	IF amplifier decoupling pin
MIXER_OUT	24	mixer output

7. Functional description

7.1 Circuit description

The SA639 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1 GHz. The bandwidth of the IF amplifier is about 40 MHz, with 44 dB of gain from a 50 Ω source. The bandwidth of the limiter is about 28 MHz with about 58 dB of gain from a 50 Ω source. However, the gain/bandwidth distribution is optimized for 9.8 MHz, 330 Ω source applications. The overall system is well-suited to battery operation as well as high performance and high-quality products of all types, such as digital cordless phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11 dB, conversion power gain of 9.2 dB, and input third-order intercept of –9.5 dBm. The oscillator operates in excess of 1 GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100 MHz for crystal configurations. Butler oscillators are recommended for crystal configurations up to 150 MHz.

The output of the mixer is internally loaded with a 330 Ω resistor permitting direct connection to a 330 Ω ceramic filter. The input resistance of the limiting IF amplifiers is also 330 Ω. With most 330 Ω ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6 dBV insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6 dBV insertion loss, a fixed or variable resistor can be added between the first IF output (IF_AMP_OUT, pin 20) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90 dB for operation at intermediate frequency at 9.8 MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output (DATA_OUT) of the quadrature is a low-impedance voltage output. This output is designed to handle a minimum bandwidth of 1 MHz. This is designed to demodulate wideband data, such as in DECT applications.

7.1.1 Post detection filter amplifier

The filter amplifier may be used to realize a group delay optimized low-pass filter for post detection. The filter amplifier can be configured for Sallen and Key low-pass with Bessel characteristic and a 3 dB cut frequency of about 800 kHz.

The filter amplifier provides a gain of 0 dB. To reduce frequency response changes as a result of amplifier load variations, the output impedance is less than 500 Ω. To keep the amplifier frequency response influence on the filter group delay characteristic at a minimum, the filter amplifier has a 3 dB bandwidth of at least 4 MHz. At the center of the carrier, it is mandatory to provide a filter output DC bias voltage of 1.6 V to be within the input common mode range of the external data comparator. The filter output DC bias voltage specification holds for an exactly center tuned demodulator tank and for the demodulator output connected to the filter amplifier input.

7.1.2 Data switch

The SA639 incorporates an active data switch used to derive the data comparator reference voltage with an external integration circuit. The data switch is typically closed for 10 μs before and during reception of the synchronization word pattern, and is otherwise open. The external integration circuit is formed by an R/C low-pass with a time constant of 5 μs to 10 μs.

The active data switch provides excellent tracking behavior over a DC input range of 1.2 V to 2.0 V. For this range with an RC load (no static current drawn), the DC output voltage does not differ more than ±5 mV from the input voltage. Since the active data switch is designed to behave like a non-linear charge pump (to allow fast tracking of the input signal without slew rate limitations under dynamic conditions of a 576 kHz input signal with 400 mV peak-to-peak and the RC load), the output signal has a 340 mV peak-to-peak output with a DC average that does not vary from the input DC average by more than ±10 mV.

The data switch is able to sink/source 3 mA from/to the external integration circuit to minimize the settling time after long power-down periods (DECT paging mode). In addition, during power-down conditions a reference voltage of approximately 1.6 V is used as the input to the switch. The switch is in a low current mode to maintain the voltage on the external RC load. This will further reduce the settling time of the capacitor after power-up. During power-down the switch can only source and sink a trickle current (10 μA). Thus, the user should make sure that other circuits (like the data comparator inputs) are not drawing current from the RC circuit.

The data switch provides a slew rate better than 1 V/μs to track with system DC offset from receive slot to receive slot (DECT idle lock or active mode). When the data switch is opened, the output is in a 3-state mode with a leakage current of less than 100 nA. This reduces discharge of the external integration circuit. When powered-down, the data switch outputs a reference of approximately 1.6 V to maintain a charge on the external RC circuit.

A Received Signal Strength Indicator (RSSI) completes the circuitry. The output range is greater than 80 dB and is temperature compensated. This log signal strength indicator exceeds the criteria for DECT cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or second-order temperature compensation of the RSSI, if needed.

Remark: dBV = 20log V_O/V_I.

8. Internal circuitry

Table 4. Internal circuits for each pin

All DC voltages measured with POWER_DOWN_CTRL (pin 8) = SWITCH_CTRL (pin 12) = GND (pin 19) = 0 V; V_{CC} (pin 5) = 3 V; DATA_OUT (pin 9) connected to POSTAMP_IN (pin 10).

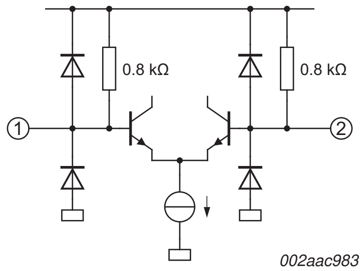
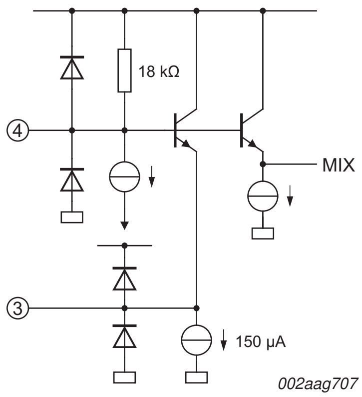
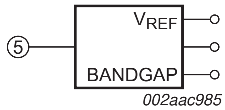
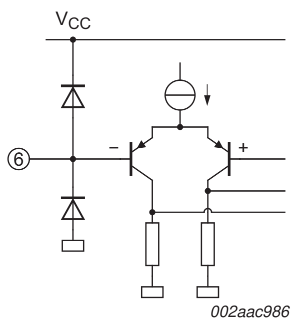
Symbol	Pin	DC V	Equivalent circuit
RF_IN	1	+1.07 V	
RF_BYPASS	2	+1.07 V	
OSC_OUT	3	+1.57 V	
OSC_IN	4	+2.32 V	
V_{CC}	5	+3.00 V	
RSSI_FEEDBACK	6	+0.20 V	

Table 4. Internal circuits for each pin *…continued*

All DC voltages measured with POWER_DOWN_CTRL (pin 8) = SWITCH_CTRL (pin 12) = GND (pin 19) = 0 V; V_{CC} (pin 5) = 3 V; DATA_OUT (pin 9) connected to POSTAMP_IN (pin 10).

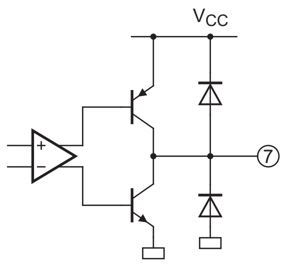
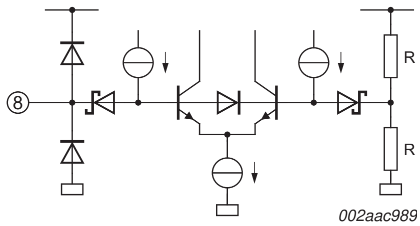
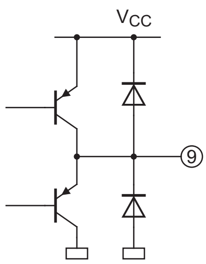
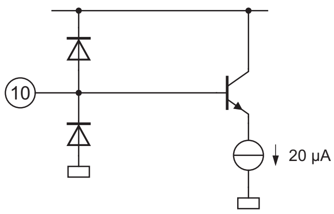
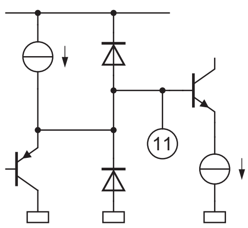
Symbol	Pin	DC V	Equivalent circuit
RSSI_OUT	7	+0.20 V	 002aac988
POWER_DOWN_CTRL	8	0 V	 002aac989
DATA_OUT	9	+1.7 V	 002aag708
POST_AMP_IN	10	+1.70 V	 002aag709
POST_AMP_OUT	11	+1.70 V	 002aag710

Table 4. Internal circuits for each pin *...continued*

All DC voltages measured with POWER_DOWN_CTRL (pin 8) = SWITCH_CTRL (pin 12) = GND (pin 19) = 0 V; V_{CC} (pin 5) = 3 V; DATA_OUT (pin 9) connected to POSTAMP_IN (pin 10).

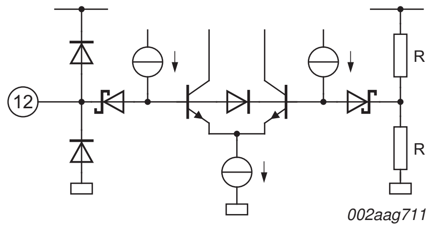
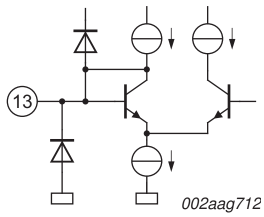
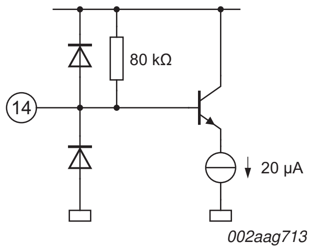
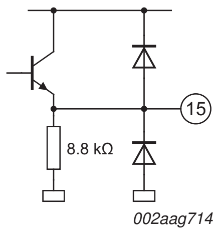
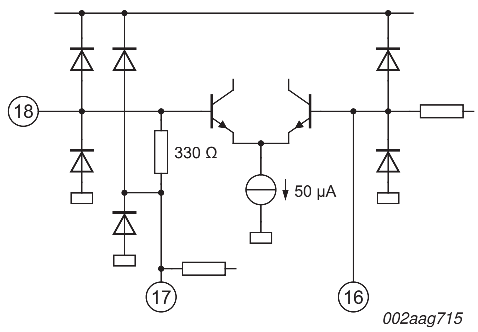
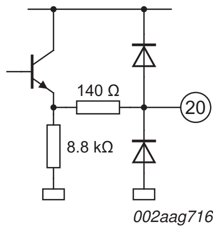
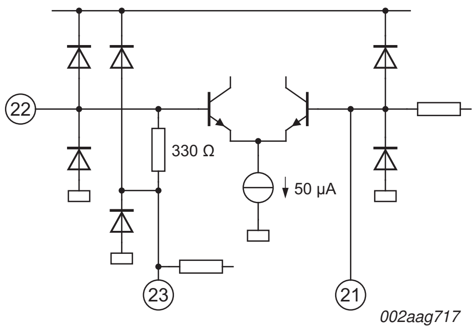
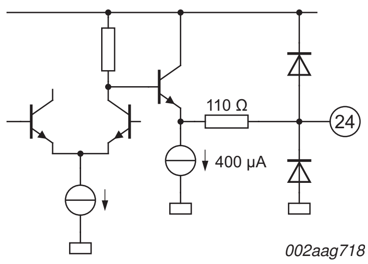
Symbol	Pin	DC V	Equivalent circuit
SWITCH_CTRL	12	0 V	
SWITCH_OUT	13	+1.70 V	
QUADRATURE_IN	14	+3.00 V	
LIMITER_OUT	15	+1.35 V	
LIMITER_DECOUPL	16	+1.23 V	
LIMITER_DECOUPL	17	+1.23 V	
LIMITER_IN	18	+1.23 V	
GND	19	0 V	-

Table 4. Internal circuits for each pin *…continued*

All DC voltages measured with POWER_DOWN_CTRL (pin 8) = SWITCH_CTRL (pin 12) = GND (pin 19) = 0 V; V_{CC} (pin 5) = 3 V; DATA_OUT (pin 9) connected to POSTAMP_IN (pin 10).

Symbol	Pin	DC V	Equivalent circuit
IF_AMP_OUT	20	+1.22 V	
IF_AMP_DECOUPL	21	+1.22 V	
IF_AMP_IN	22	+1.22 V	
IF_AMP_DECOUPL	23	+1.22 V	
MIXER_OUT	24	+1.03 V	

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+6	V
V_n	voltage on any other pin	[1]	–0.3	V_{CC} + 0.3	V
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C

[1] Except logic input pins (POWER_DOWN_CTRL and SWITCH_CTRL), which can have 6 V maximum.

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	TSSOP24 package	117	°C/W

11. Static characteristics

Table 7. Static characteristics
V_{CC} = 3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	3.0	5.5	V
I_{CC}	supply current	DC current drain; POWER_DOWN_CTRL = LOW; SWITCH_CTRL = HIGH; $-3\ \sigma$ = 8.33 mA; $+3\ \sigma$ = 8.87 mA	-	8.6	10	mA
$I_{CC(stb)}$	standby supply current	POWER_DOWN_CTRL = LOW; SWITCH_CTRL = HIGH $-3\ \sigma$ = 131.9 µA; $+3\ \sigma$ = 148.1 µA	-	140	500	µA
I_I	input current	POWER_DOWN_CTRL = LOW	-	-	10	µA
		POWER_DOWN_CTRL = HIGH	-	-	4	µA
V_I	input voltage	POWER_DOWN_CTRL = LOW	0	-	$0.3 \times V_{CC}$	V
		POWER_DOWN_CTRL = HIGH [1]	$0.7 \times V_{CC}$	-	6	V
t_{ON}	power-up time	RSSI valid (10 % to 90 %)	-	10	-	µs
t_{OFF}	power-down time	RSSI invalid (90 % to 10 %)	-	5	-	µs
	power-up settling time	data output valid	-	100	200	µs
Switching						
V_I	input voltage	switch closed; SWITCH_CTRL = LOW; POWER_DOWN_CTRL = LOW	0	-	$0.3 \times V_{CC}$	V
		switch open; output 3-state; SWITCH_CTRL = HIGH	$0.7 \times V_{CC}$	-	6	V
I_I	input current	SWITCH_CTRL = LOW	-	-	10	µA
		SWITCH_CTRL = HIGH	-	-	4	µA
	switch activation time		-	0.5	1	µs

[1] When the device is forced in Power-down mode via POWER_DOWN_CTRL (pin 8), the data switch outputs a voltage close to 1.6 V and the state of the SWITCH_CTRL (pin 12) input has no effect.

12. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = 25 °C; V_{CC} = +3 V, unless otherwise stated. RF frequency = 110.592 MHz; LO frequency = 120.392 MHz; IF frequency = 9.8 MHz; RF level = −45 dBm; FM modulation = 576 kHz with ±288 kHz peak deviation, discriminator tank circuit Q = 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout improves many of the listed parameters.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mixer/oscillator section (external LO = −14 dBm)						
f_i	input frequency	signal	-	500	-	MHz
f_{osc}	oscillator frequency	external oscillator (buffer)	0.2	500	-	MHz
NF	noise figure	at 110 MHz	-	11	-	dB
$IP3_i$	input third-order intercept point	matched f1 = 110.592 MHz; f2 = 110.852 MHz	-	−9.5	-	dBm
$G_{p(conv)}$	conversion power gain		6	9.2	-	dB
$R_{i(RF)}$	RF input resistance	single-ended input	-	800	-	Ω
$C_{i(RF)}$	RF input capacitance		-	3.5	-	pF
$R_{o(mix)}$	mixer output resistance	MIXER_OUT pin	-	330	-	Ω
IF section						
$G_{amp(IF)}$	IF amplifier gain		-	40	-	dB
G_{lim}	limiter gain		-	52	-	dB
$P_{i(IF)}$	IF input power	for −3 dB input limiting sensitivity; test at IF_AMP_IN pin	-	−100	-	dBm
$Z_{i(IF)}$	IF input impedance		-	330	-	Ω
$Z_{o(IF)}$	IF output impedance		-	330	-	Ω
$Z_{i(lim)}$	limiter input impedance		-	330	-	Ω
$Z_{o(lim)}$	limiter output impedance		-	330	-	Ω
$V_{o(RMS)}$	RMS output voltage	no load; LIMITER_OUT pin	-	130	-	mV
RF/IF section (external LO = −14 dBm)						
	peak-to-peak data level	R_L = 10 kΩ; C_L = 30 pF	260	360	-	mV
	data bandwidth		-	2.4	-	MHz
S/N	signal-to-noise ratio	no modulation for noise	-	60	-	dB
α_{AM}	AM rejection	80 % AM 1 kHz	-	36	-	dB
$V_{o(RSSI)}$	RSSI output voltage	RF; with buffer				
		RF level = −90 dBm	0	0.4	0.75	V
		RF level = −45 dBm	0.5	0.9	1.3	V
		RF level = −10 dBm	0.8	1.2	1.6	V
$t_{r(o)}$	output rise time	RF RSSI output; 10 kHz pulse with 9.8 MHz filter; no RSSI bypass capacitor; IF frequency = 9.8 MHz				
		RF level = −45 dBm	-	0.8	-	μs
		RF level = −28 dBm	-	0.8	-	μs

Table 8. Dynamic characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = +3 V, unless otherwise stated. RF frequency = 110.592 MHz; LO frequency = 120.392 MHz; IF frequency = 9.8 MHz; RF level = −45 dBm; FM modulation = 576 kHz with ±288 kHz peak deviation, discriminator tank circuit Q = 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout improves many of the listed parameters.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{f(o)}$	output fall time	RF RSSI output; 10 kHz pulse with 9.8 MHz filter; no RSSI bypass capacitor; IF frequency = 9.8 MHz					
		RF level = −45 dBm		-	2.0	-	μs
		RF level = −28 dBm		-	1.8	-	μs
$\alpha_{RSSI(range)}$	RSSI range			-	80	-	dB
$\Delta\alpha_{RSSI}$	RSSI variation			-	±1.5	-	dB
SINAD	signal-to-noise-and-distortion ratio	RF level = −85 dBm		-	12	-	dB
S/N	signal-to-noise ratio	RF level = −100 dBm		-	10	-	dB
Post detection filter amplifier							
B_{3dB}	3 dB bandwidth	amplifier; AC coupled; R_L = 10 kΩ; C_L = 33 pF		-	12.8	-	MHz
G	gain	amplifier; AC coupled; R_L = 10 kΩ; V_O (DC) = 1.6 V		-	−0.2	-	dB
	slew rate	AC coupled; R_L = 10 kΩ; C_L = 33 pF		-	2.4	-	V/μs
R_i	input resistance			300	-	-	kΩ
C_i	input capacitance			-	-	3	pF
Z_o	output impedance			-	150	800	Ω
$R_{L(o)}$	output load resistance	AC coupled		5	-	-	kΩ
$C_{o(L)}$	output load capacitance	AC coupled	[1]	-	30	-	pF
	DC output level		[2]	1.5	1.7	1.9	V
Data switch							
	DC input voltage range		[3]	1.2	1.6	2.0	V
	peak-to-peak AC input swing			-	400	-	mV
Z_i	input impedance			100	-	-	kΩ
C_i	input capacitance			-	-	5	pF
$R_{L(o)}$	output load resistance			-	500	-	Ω
Through mode (SWITCH_CTRL = LOW)							
G_v	voltage gain	AC voltage	[4]	-	−1.5	-	dB
	output drive capability	sink/source; V_O (DC) = 1.6 V		3	-	-	mA
	slew rate	V_O (DC) = 1.6 V		-	>14.0	-	V/μs
	static offset voltage	V_I (DC) = 1.2 V to 2.0 V	[5]	-	0.30	±5	mV
$V_{offset(DC)}$	DC offset voltage	V_I (DC) = 1.4 V to 2.0 V; V_{CC} = 3.0 V to 5.0 V	[2][6]				
		RF level = −70 dBm to −40 dBm		−7	-	+7	mV
		RF level = −40 dBm to −5 dBm		−10	-	+10	mV

Table 8. Dynamic characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = +3 V, unless otherwise stated. RF frequency = 110.592 MHz; LO frequency = 120.392 MHz; IF frequency = 9.8 MHz; RF level = −45 dBm; FM modulation = 576 kHz with ±288 kHz peak deviation, discriminator tank circuit Q = 4. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout improves many of the listed parameters.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3-state mode (SWITCH_CTRL = HIGH)						
I_{LO}	output leakage current	V_O (DC) = 1.2 V to 2.0 V	-	20	100	nA

[1] Includes filter feedback capacitance, comparator input capacitance. PCB stray capacitances and switch input capacitance.

[2] Demodulator output DC coupled with Post Detection Filter Amplifier input and the demodulator tank exactly tuned to center frequency.

[3] Includes DC offsets due to frequency offsets between Rx and Tx carrier and demodulator tank offset due to mis-tuning.

[4] With a 400 mV (peak-to-peak) sinusoid at 600 kHz driving POSTAMP_IN pin. Output load resistance 500 Ω in series with 10 nF.

[5] With a DC input and capacitor in the RC load fully charged.

[6] The switch is closed every 10 ms for a duration of 40 μs. The DC offset is determined by calculating the difference of two DC measurements, which are determined as follows:

a) The first DC value is measured at the integrating capacitor of the switch when the switch is in the closed position immediately before it opens. The value to be measured is in the middle of the peak-to-peak excursion of the superimposed sine-wave. (DClow + (DChigh − DClow) / 2).

b) The second DC value (calculated as above) is measured at POSTAMP_OUT pin immediately after the switch opens, and is the DC value that gives the largest DC offset to the first DC measurement within a 400 μs DECT burst. Minimum and maximum limits are not tested, however, they are guaranteed by design and characterization using an optimized layout and application circuit.

13. Performance curves

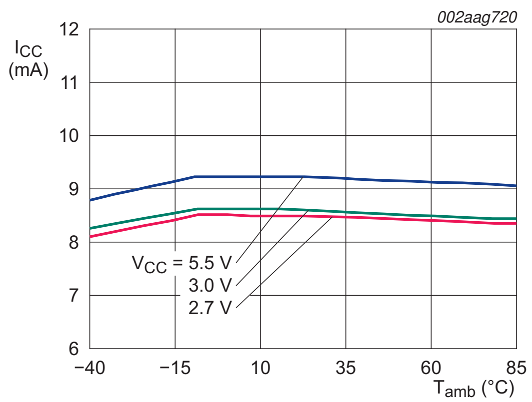


Fig 3. Supply current versus ambient temperature

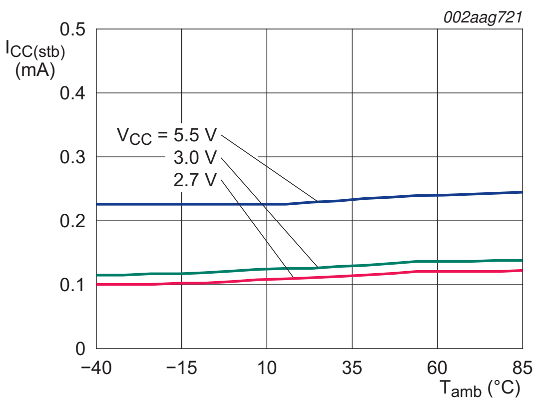
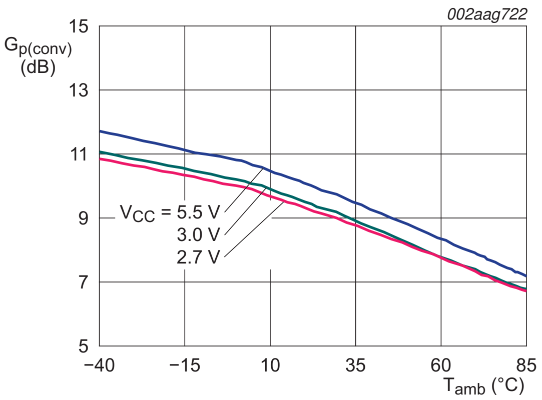


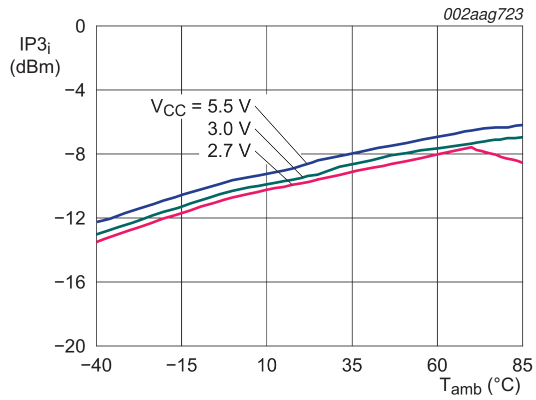
Fig 4. Standby supply current versus ambient temperature



RF = −40 dBm, 110.592 MHz

LO = −10 dBm, 120.392 MHz

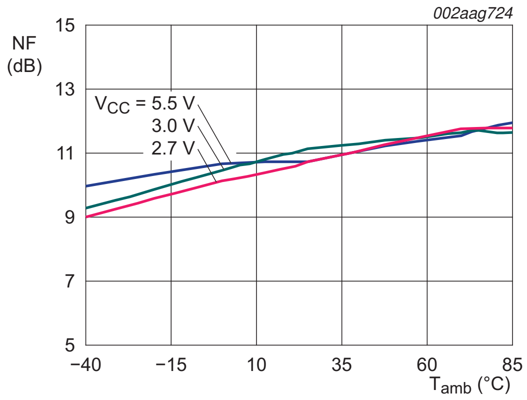
Fig 5. Mixer conversion power gain versus ambient temperature



RF = −40 dBm, 110.592 MHz

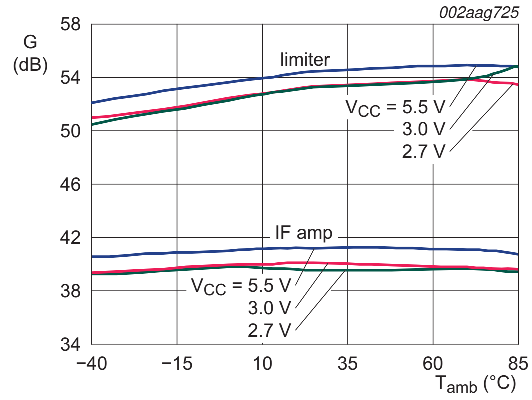
LO = −10 dBm, 120.392 MHz

Fig 6. Mixer input third-order intercept point versus ambient temperature



IF = 11 MHz

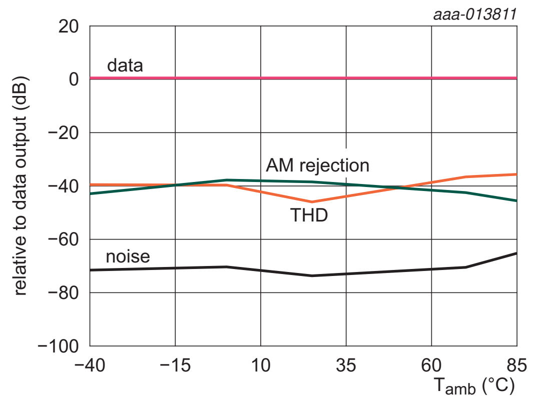
Fig 7. Mixer noise figure versus ambient temperature



IF input = −90 dBm, 9.8 MHz

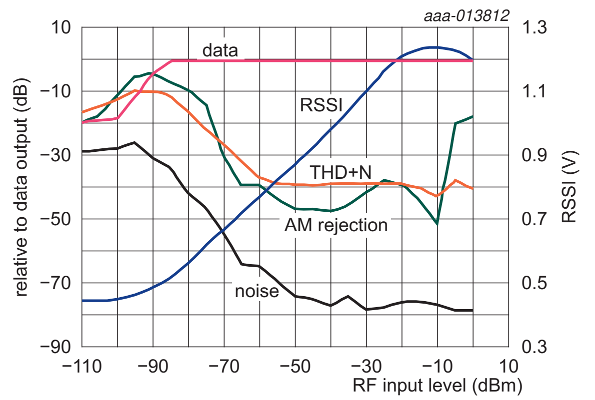
Limiter input = −100 dBm, 9.8 MHz

Fig 8. Limiter and IF gain versus ambient temperature



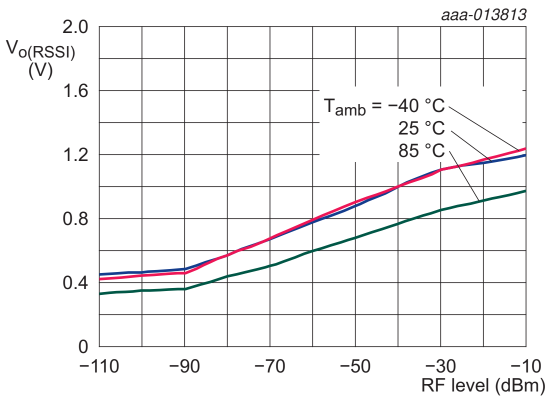
RF = 110 MHz; level = −50 dBm; deviation = 288 kHz; LO = 119.8 MHz; −14 dBm; V_{CC} = 3 V

Fig 9. Relative data output level, THD, noise and AM rejection versus ambient temperature



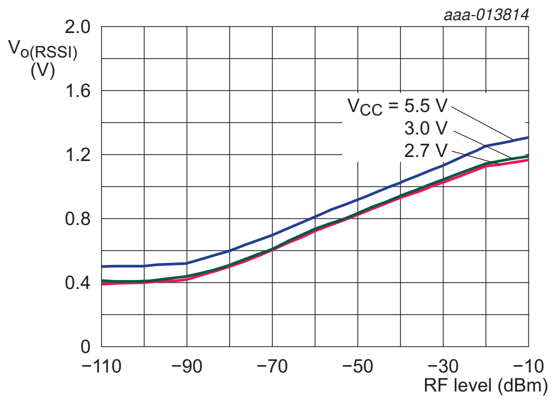
RF = 110 MHz; LO = 119.8 MHz; data = 430.76 mV (peak-to-peak); V_{CC} = 3 V; T_{amb} = 25 °C; 576 kHz sine

Fig 10. Receiver RF performance



V_{CC} = 3 V

Fig 11. RSSI versus RF level and temperature



T_{amb} = 25 °C

Fig 12. RSSI versus RF level and V_{CC}

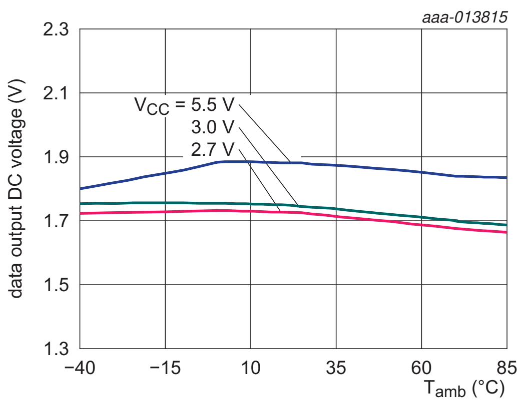


Fig 13. Data output DC voltage versus ambient temperature

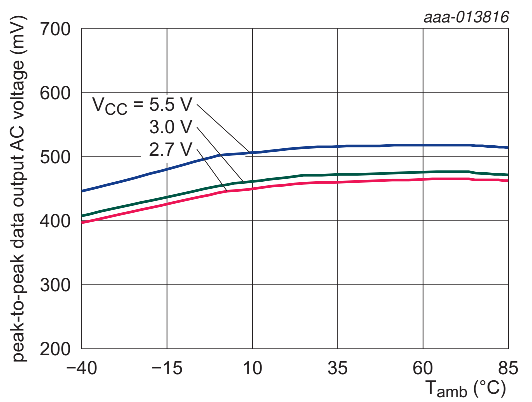


Fig 14. Data output AC voltage versus ambient temperature

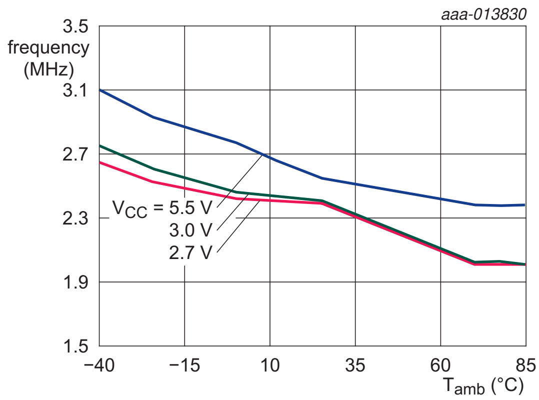


Fig 15. Data output −3 dB bandwidth versus ambient temperature

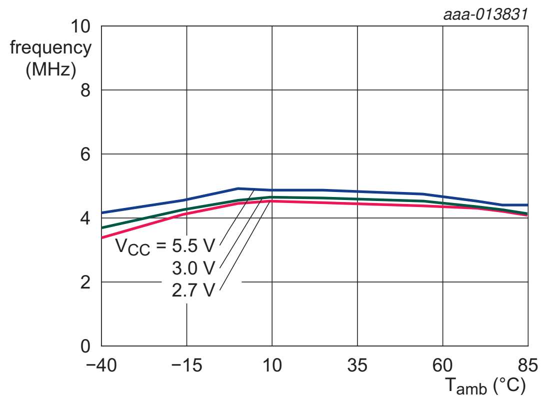


Fig 16. Switch −3 dB bandwidth versus ambient temperature

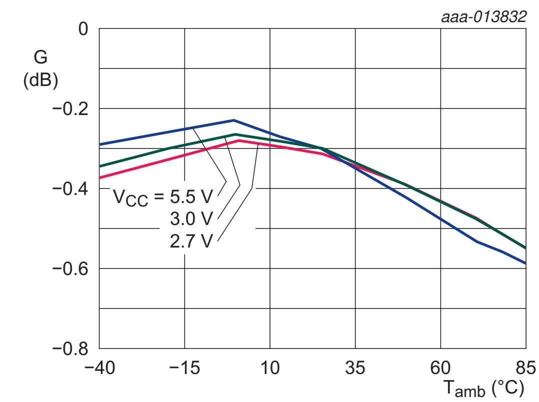


Fig 17. Post detection amplifier versus ambient temperature

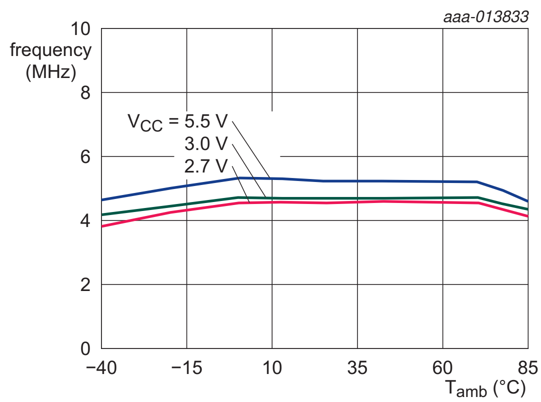


Fig 18. Post detection amplifier −3 dB bandwidth versus ambient temperature

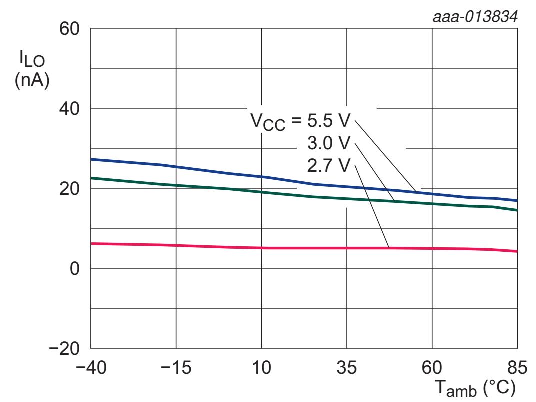


Fig 19. Switch output leakage current versus ambient temperature

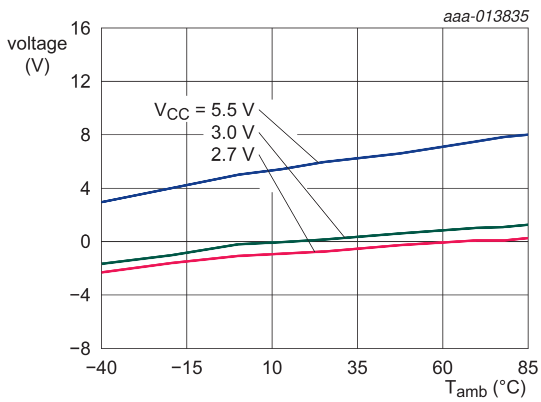


Fig 20. Switch output to input offset voltage versus ambient temperature

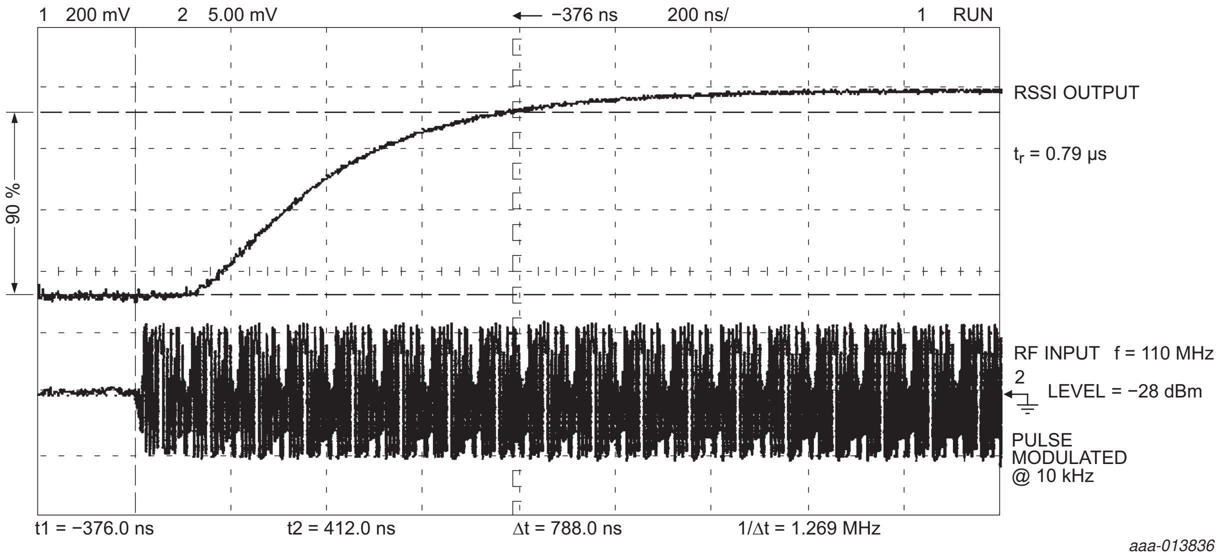


Fig 21. RSSI rise time

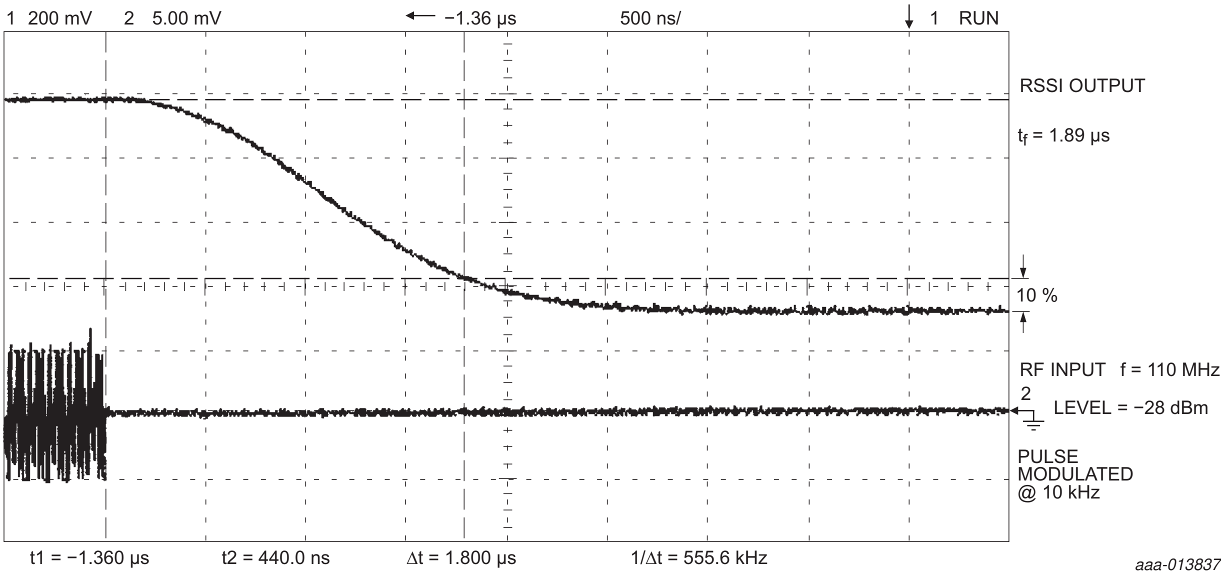


Fig 22. RSSI fall time

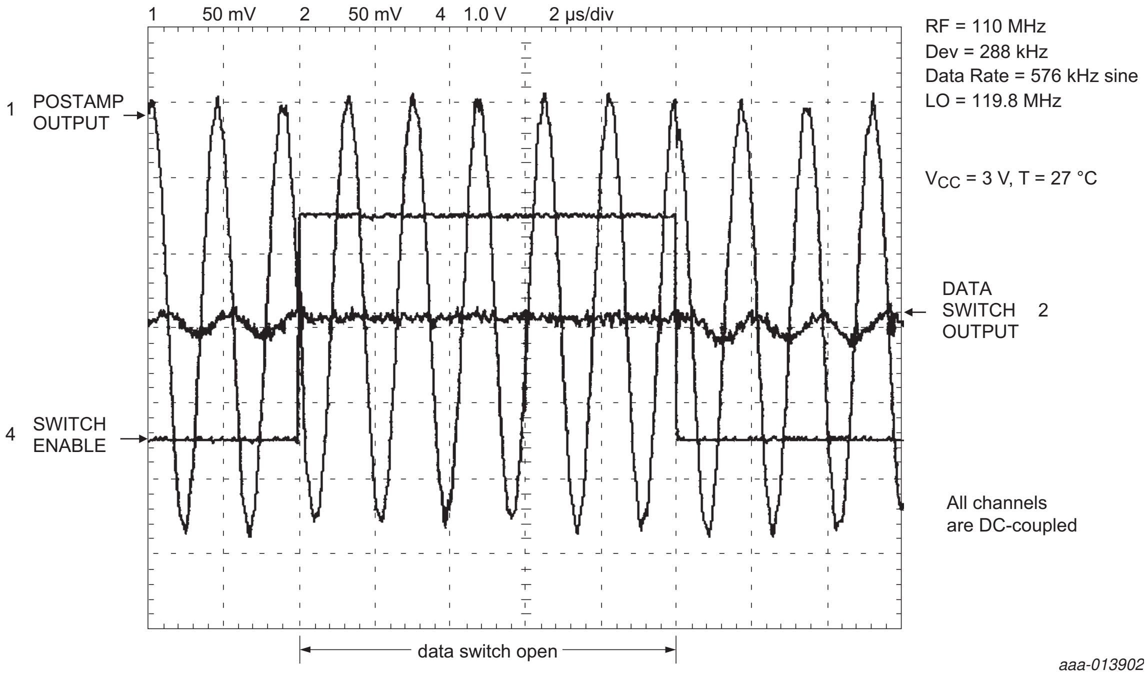


Fig 23. System dynamic response

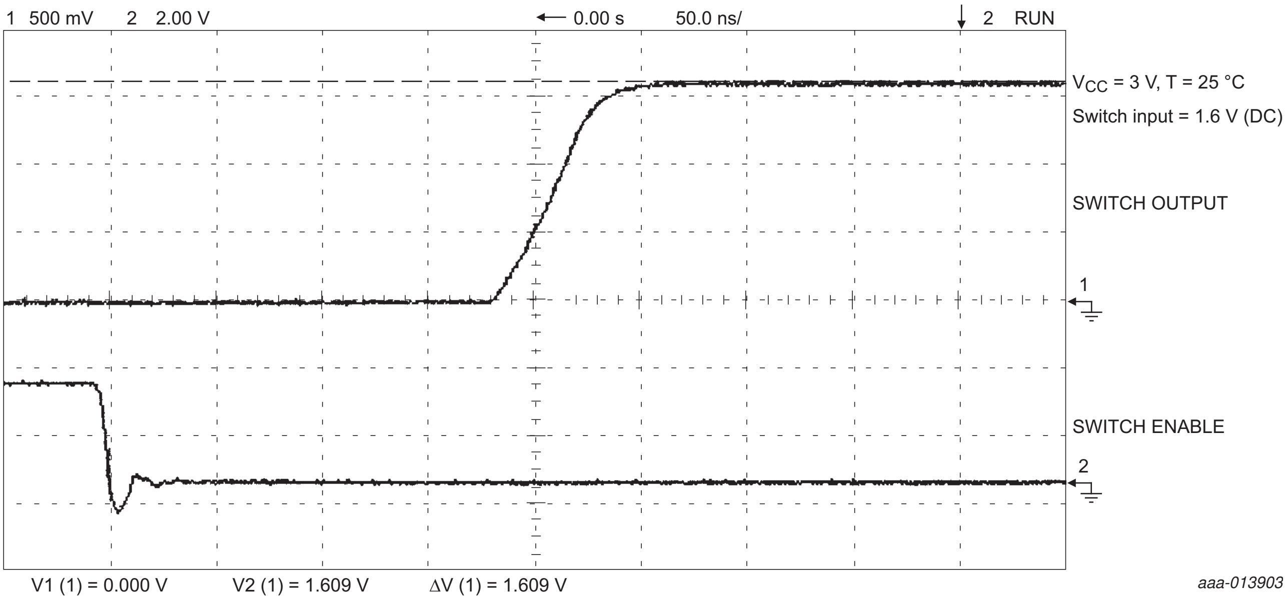


Fig 24. Data switch activation time

14. Test information

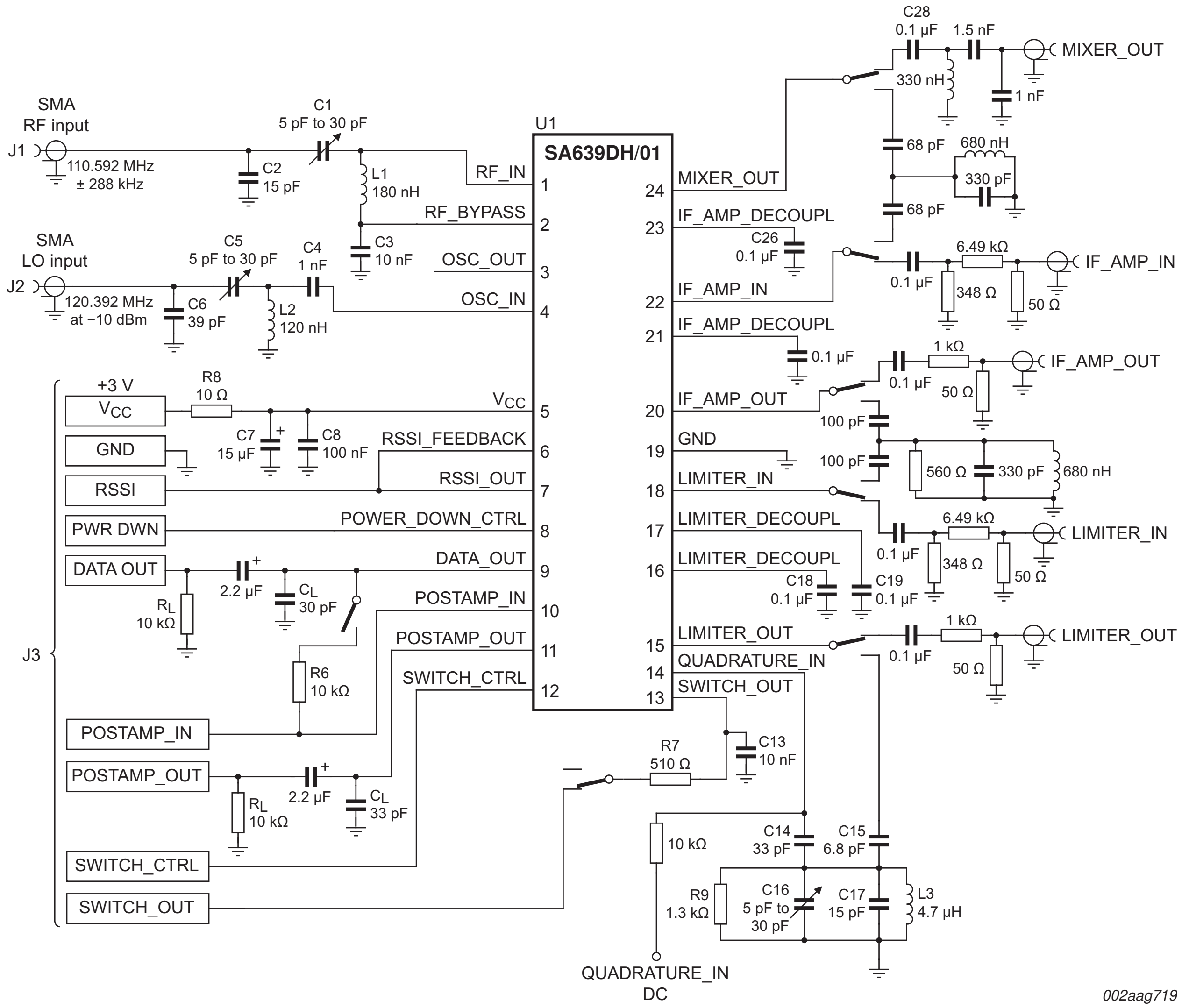
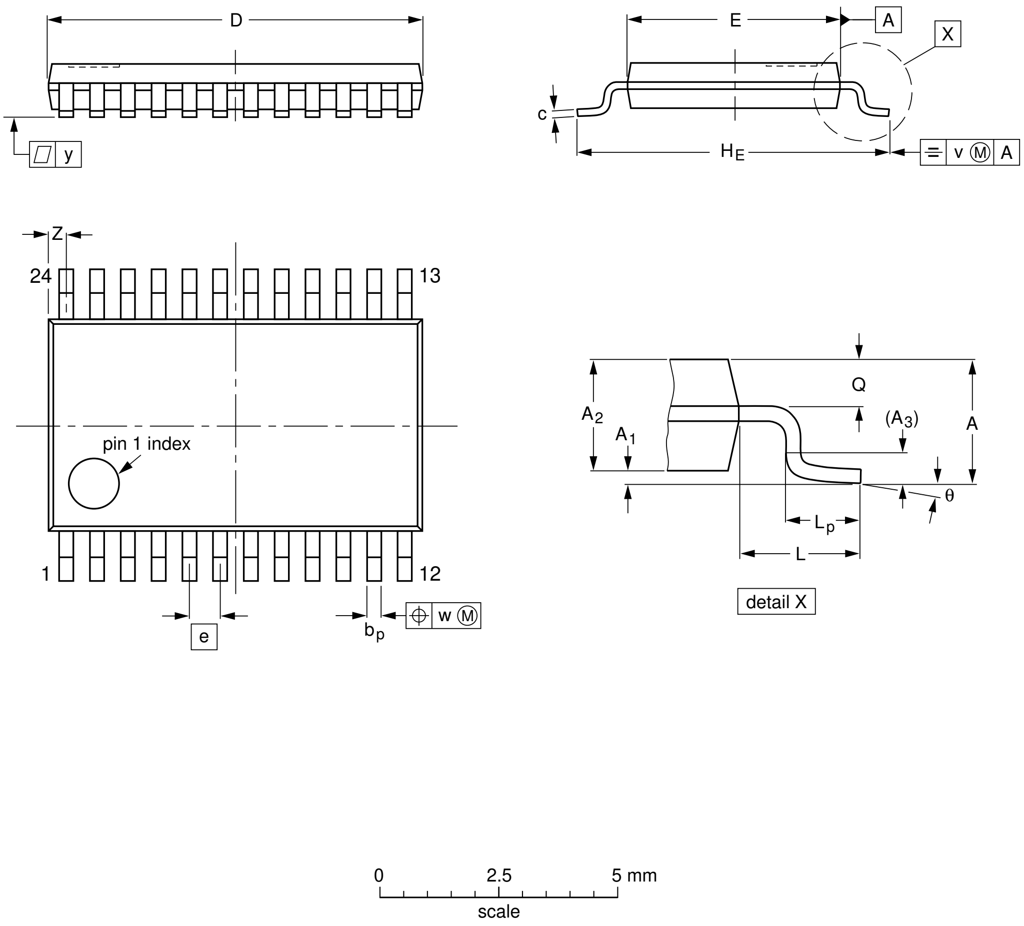


Fig 25. SA639 test circuit

15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

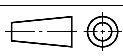
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 26. Package outline SOT355-1 (TSSOP24)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 27) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020D)

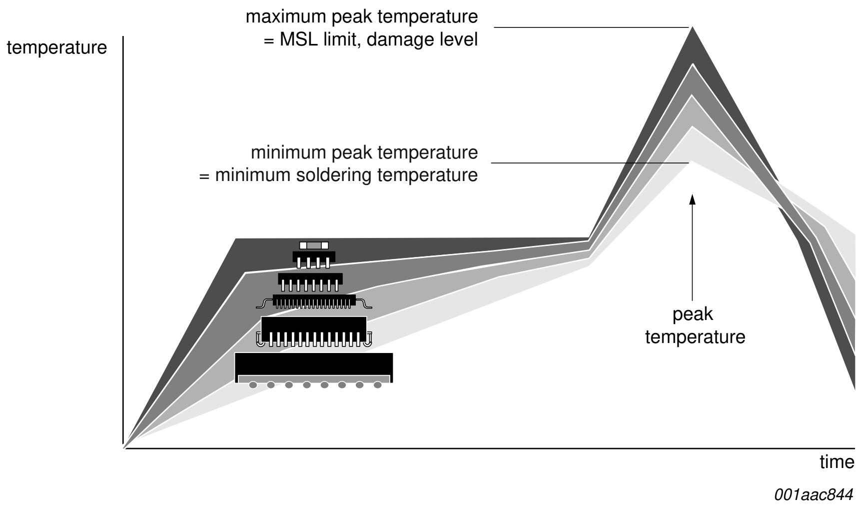
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 27.



MSL: Moisture Sensitivity Level

Fig 27. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
CMOS	Complementary Metal-Oxide Semiconductor
DECT	Digital European Cordless Telephone
ESD	ElectroStatic Discharge
FM	Frequency Modulation
FSK	Frequency Shift Keying
IF	Intermediate Frequency
LC	inductor-capacitor network
LO	Local Oscillator
PCB	Printed-Circuit Board
RC	resistor-capacitor network
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
THD	Total Harmonic Distortion
TTL	Transistor-Transistor Logic