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DATA SHEET

SAA6588
RDS/RBDS pre-processor

Product specification
Supersedes data of 1997 Sep 01
File under Integrated Circuits, IC01

2002 Jan 14

Philips
Semiconductors

PHILIPS

FEATURES

- Integrated switched capacitor filters
- Demodulation of the European Radio Data System (RDS) or the USA Radio Broadcast Data System (RBDS) signal
- RDS and RBDS block detection
- Error detection and correction
- Fast block synchronization
- Synchronization control (flywheel)
- Mode control for RDS/RBDS processing
- Different RDS/RBDS block information output modes (e.g. A-block output mode)
- Fast I²C-bus interface
- Multi-path detector
- Signal quality detector with sensitivity adjustment
- Pause detector with pause level and time adjustment
- Alternatively oscillator frequency: n × 4.332 MHz (n = 1 to 4)
- UART compatible with 17.328 MHz (n = 4)
- CMOS device
- Single supply voltage
- Extended temperature range (−40 to +85 °C).

GENERAL DESCRIPTION

Today most FM radio stations in Europe and meanwhile also many FM/AM radio broadcasting stations in the USA transmit the inaudible European RDS (Radio Data System) or the USA RBDS (Radio Broadcast Data System) informations respectively. Likewise nowadays receivers, most car radios and also some home and portable radios on the market include at least some of the RDS features.

The RDS/RBDS system offers a large range of applications by its many functions to be implemented. For car radios the most important are:

- Program Service (PS) name
- Traffic Program (TP) identification
- Traffic Announcement (TA) signal
- Alternative Frequency (AF) list
- Program Identification (PI)
- Enhanced Other Networks (EON) information.

The RDS/RBDS pre-processor is a CMOS device that integrates all RDS/RBDS relevant functions in one chip. The IC contains filtering and demodulation of the RDS/RBDS signal, symbol decoding, block synchronization, error detection, error correction and additional detectors for multi-path, signal quality and audio signal pauses. The pre-processed RDS/RBDS information is available via the I²C-bus.

The RDS/RBDS pre-processor replaces a number of ICs and peripheral components used nowadays in car radio concepts with RDS or RBDS features. The integration of the relevant RDS/RBDS data processing functions provides, in an economic manner, high performance of RDS/RBDS processing and reduces the real-time requirements for the main radio microcontroller considerably. In addition it simplifies the development of the RDS specific software for the main controller of the radio set.

Compared with standard radio systems, RDS/RBDS controlled radio systems additionally require an RDS/RBDS demodulator with a 57 kHz band-pass filter, information about the current reception situation (reception quality, multi-path disturbance etc.), and additional microcontroller power for RDS/RBDS data processing, decoding and radio control.

The new RDS/RBDS pre-processor includes all these specific functions and meets all requirements of a high end RDS/RBDS radio. Moreover the timing requirements of the set controller, regarding RDS/RBDS data processing are reduced due to the integration of decoder functions, so that the development of radio control software can be concentrated specifically on radio set features.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
$I_{DD(tot)}$	total supply current		–	14.0	–	mA
$V_{i(MPX)}$	RDS input sensitivity at pin MPX		1	–	–	mV
ΔG_{SQ}	step size for signal quality input gain		–	0.6	–	dB
CR_{GSQ}	control range for signal quality input gain		–	18.6	–	dB
$t_{PON(min)}$	minimum time for pause	adjustable in 4 steps	20.2	–	161.7	ms
$f_{i(xtal)}$	crystal input frequency	n = 1	–	4.332	–	MHz
		n = 2	–	8.664	–	MHz
		n = 3	–	12.996	–	MHz
		n = 4	–	17.328	–	MHz

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6588	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
SAA6588T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

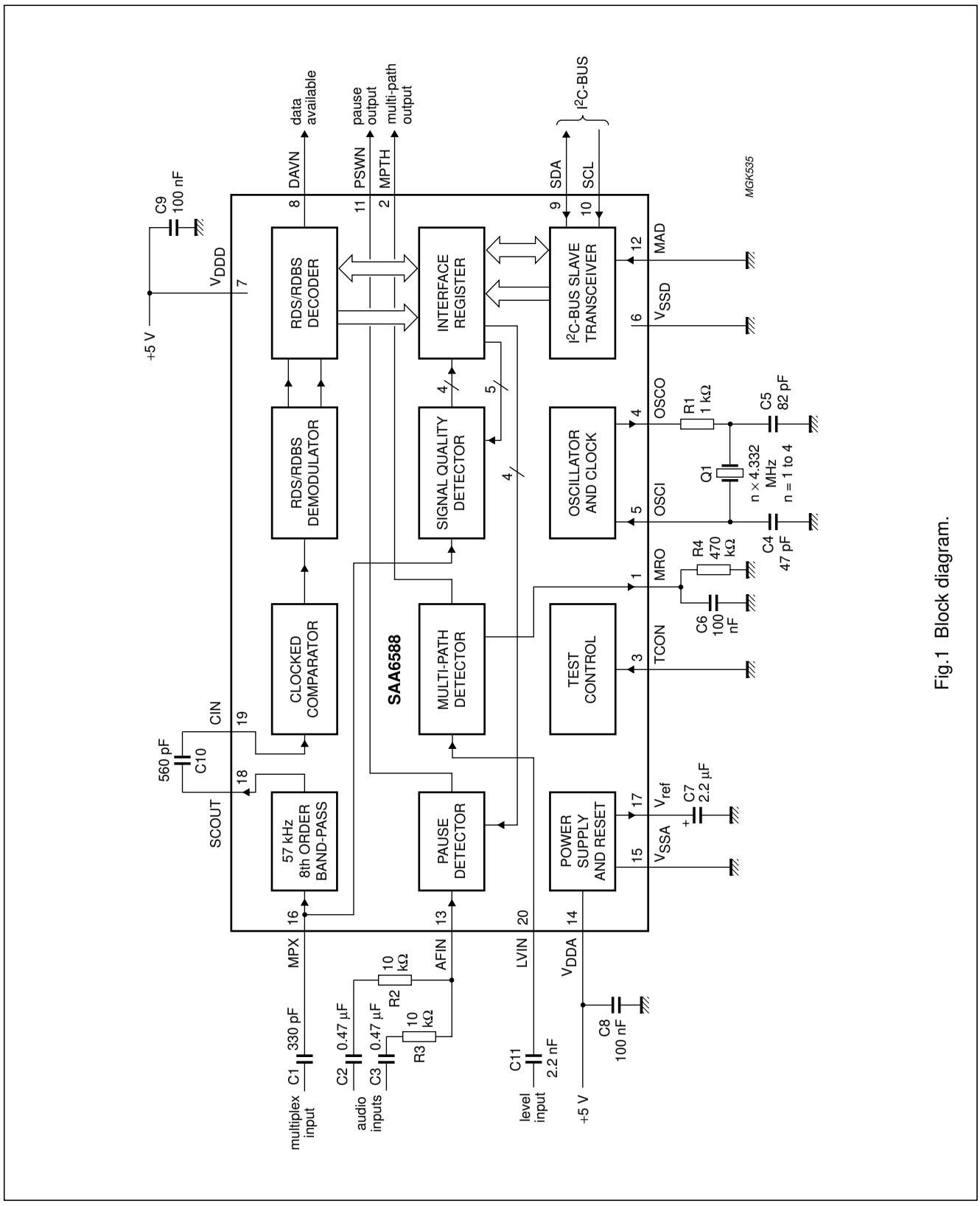


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MRO	1	multi-path rectifier output
MPTH	2	multi-path detector output
TCON	3	test control input pin
OSCO	4	oscillator output
OSCI	5	oscillator input
V_{SSD}	6	digital ground (0 V)
V_{DDD}	7	digital supply voltage (5 V)
DAVN	8	data available output (active LOW)
SDA	9	I^2C-bus serial data I/O
SCL	10	I^2C-bus serial clock input
PSWN	11	pause switch output (active LOW)
MAD	12	slave address (LSB) input
AFIN	13	audio signal input
V_{DDA}	14	analog supply voltage (5 V)
V_{SSA}	15	analog ground (0 V)
MPX	16	multiplex input signal
V_{ref}	17	reference voltage output
SCOUT	18	band-pass filter output
CIN	19	comparator input
LVIN	20	level input

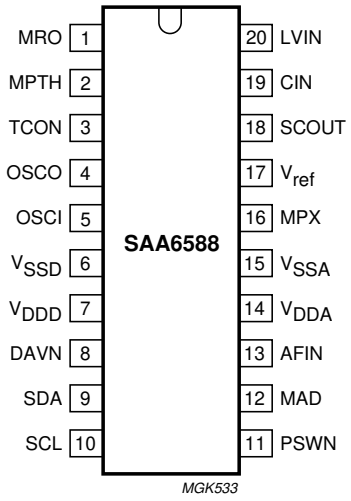


Fig.2 Pin configuration (DIP20).

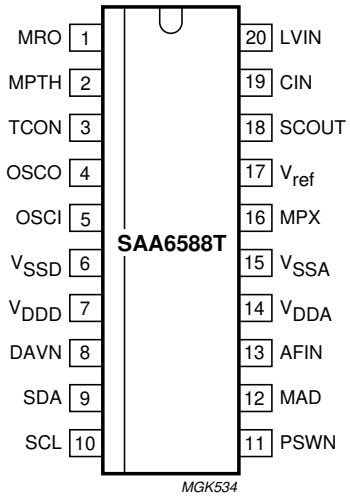


Fig.3 Pin configuration (SO20).

FUNCTIONAL DESCRIPTION

General

The following functions are performed by the SAA6588:

- Selection of the RDS/RBDS signal from the MPX input signal
- 57 kHz carrier regeneration
- Demodulation of the RDS/RBDS signal
- Symbol decoding
- RDS/RBDS block detection
- Error detection and correction of transmission errors
- Fast block synchronization and synchronization control
- Detection of multi-path distortion and audio signal pauses
- Determination of the signal quality
- Mode control of processing and RDS/RBDS data output via I^{2}C-bus interface
- Sensing of pause and multi-path, information via extra output pins.

The block diagram of the RDS/RBDS pre-processor is shown in Fig.1. For the application of the device only a few external components are required. The pre-processors functional blocks are described in the following sections.

RDS/RBDS signal demodulation

BAND-PASS FILTER

The band-pass filter has a centre frequency of 57 kHz. It selects the RDS/RBDS sub-band from the multiplex signal MPX and suppresses the audio signal components. The filter block contains an analog anti-aliasing filter at the input followed by an 8th order switched capacitor band-pass filter and a reconstruction filter at the output.

CLOCKED COMPARATOR

The comparator digitizes the output signal from the 57 kHz band-pass filter for further processing by the digital RDS/RBDS demodulator. To attain high sensitivity and to avoid phase distortion, the comparator input stage contains an automatic offset compensation.

DEMODULATION

The demodulator provides all functions of the SAA6579 but has improved performance under weak signal conditions.

The demodulator includes:

- 57 kHz carrier regeneration from the two sidebands (Costas loop)
- Symbol integration over one RDS clock period
- Bi-phase symbol decoding
- Differential decoding
- Synchronization of RDS/RBDS output data with clock.

The RDS/RBDS demodulator recovers and regenerates the continuously transmitted RDS/RBDS data stream out of the multiplex signal (MPX) and provides the internal signals clock (RDCL) and data (RDDA) for further processing by the RDS/RBDS decoder block.

RDS/RBDS data processing

The RDS/RBDS data processing of the pre-processor handles the complete processing and decoding of the continuous serial RDS/RBDS demodulator output data stream.

Different data processing modes are software controllable by the external main controller via I^{2}C-bus.

Processed RDS/RBDS data blocks, decoder status information and signal quality information are also available via the I^{2}C-bus.

RDS/RBDS DECODER

The RDS/RBDS decoder contains:

- RDS/RBDS block detection
- Error detection and correction
- Synchronization
- Flywheel for synchronization hold
- Bit slip correction
- Data processing control
- RDS/RBDS data output.

RDS/RBDS block detection

The RDS/RBDS block detection is always active.

For a received sequence of 26 data bits, a valid block and its offset are identified via syndrome calculation.

During synchronization search, the syndrome is calculated with every new received data bit (bit-by-bit) for a received 26-bit sequence. If the decoder is synchronized, syndrome calculation is activated only after 26 data bits for each new block received.

Under RBDS reception situation, beside the RDS block sequences with (A, B, C/C', D) offset also block sequences of 4 blocks with offset E may be received. If the decoder detects an E-block, this block is marked in the block identification number BL and is available via an I^{2}C-bus request. In RBDS processing mode the block is signed as valid E-block and in RDS processing mode, where only RDS blocks are expected, signed as invalid E-block (see Table 13).

This information can be used by the main controller to detect E-block sequences and identify RDS or RBDS transmitter stations.

Error detection and correction

The RDS/RBDS error detection and correction recognizes and corrects potential transmission errors within a received block via parity-check in consideration of the offset word of the expected block. Burst errors with a maximum length of 5 bits are corrected with this method.

After synchronization has been found the error correction is always active, but cannot be carried out in every reception situation.

During synchronization search, the error correction is disabled for detection of the first block and is enabled for processing of the second block depending on the pre-selected error correction mode for synchronization (mode SYNCA to SYNCC, see Table 4).

The processed block data and the status of error correction are available for data request via the I^{2}C-bus for the last two blocks.

Processed blocks are characterized as uncorrectable under the following conditions:

- During synchronization search, if the burst error is higher than allowed by the pre-selected correction mode.
- After synchronization has been found, if the burst error is higher than 5 bits or if errors are detected but error correction is not possible.

Synchronization

The decoder is synchronized if two successive valid blocks in a valid sequence are detected by the block detection.

For detection of the second block of this sequence, error correction is also enabled depending on the pre-selected correction mode (see Table 4). Only valid (correctable) blocks are accepted for synchronization (see also Section “Error detection and correction”).

If synchronization is found, the synchronization status flag (SYNC) is set and available via an I^{2}C-bus request.

The synchronization is held until the flywheel (for synchronization hold) detects a loss of synchronization (see Section “Flywheel for synchronization hold”) or an external restart of synchronization is performed (see Section “Data processing control”).

Flywheel for synchronization hold

For a fast detection of loss of synchronization the internal flywheel counter checks the number of uncorrectable blocks (error blocks). Error blocks increment and valid blocks decrement the block error counter.

The flywheel counter is only active if the decoder is synchronized. The synchronization is held until the flywheel counter detects an error block overflow (loss of synchronization). The maximum value for the error block counter is adjustable via the I^{2}C-bus in a range of 0 to 63 (see Table 6).

The value 32 is set after reset and the values 0 and 63 have a special function.

- If the value 0 is programmed then no flywheel is active
- If the value 63 is programmed then the flywheel is endless and no new start of synchronization is effected automatically (synchronization hold).

Bit slip correction

During poor reception situation phase shifts of one bit to the left or right (±1 bit slip) between the RDS/RBDS clock and data may occur, depending on the lock conditions of the demodulators clock regeneration.

If the decoder is synchronized and detects a bit slip, the synchronization is corrected by +1 or −1 bit via block detection on the respectively shifted expected new block.

Data processing control

The pre-processor provides different operating modes selectable via the external I²C-bus. The data processing control performs the pre-selected operating modes and controls the requested output of the RDS/RBDS information.

Restart of synchronization mode:

The 'restart synchronization' (NWSY) control mode immediately terminates the actual synchronization and restarts a new synchronization search procedure. The NWSY flag is automatically reset after the restart of synchronization by the decoder.

This mode is required for a fast new synchronization on the RDS/RBDS data from a new transmitter station if the tuning frequency is changed by the radio set.

Restart of synchronization search is furthermore automatically carried out if the internal flywheel signals a loss of synchronization (see Section "Flywheel for synchronization hold").

Error correction control mode for synchronization:

For error correction and identification of valid blocks during synchronization search, three different modes are selectable. (SYM1, SYM0, see Table 4).

RBDS processing mode:

The pre-processor is suitable for receivers intended for the European (RDS) as well as for the USA (RBDS) standard. If RBDS mode is selected via the I²C-bus, the block detection and the error detection and correction are adjusted to RBDS data processing.

Data available control mode:

The pre-processor provides three different RDS/RBDS data output processing modes selectable via the 'data available' control mode: (see also Section "RDS/RBDS data output" and Table 5).

Standard processing mode: if the decoder is synchronized and a new block is received (every 26 bits), the actual RDS/RBDS information of the last two blocks is available with every new received block.

Fast PI search mode: during synchronization search and if a new A-block is received, the actual RDS/RBDS information of this or the last two A-blocks respectively is available with every new received A-block. If the decoder is synchronized, the standard processing mode is valid.

Reduced data request processing mode: if the decoder is synchronized and two new blocks are received (every 52 bits), the actual RDS/RBDS information of the last two blocks is available with every two new received blocks.

The RDS/RBDS pre-processor provides data output of the block identification, the RDS/RBDS information words and error detection and correction status of the last two blocks as well as signal quality indication and general decoder status information.

In addition, the decoder controls also the data request from the external main controller. The pre-processor activates the 'data overflow' status flag DOFL (see Section "Programming"), if the decoder is synchronized and a new RDS/RBDS block is received before the previously processed block was completely transmitted via I²C-bus. After detection of data overflow the interface registers are not updated until reset of the data overflow flag by reading via the I²C-bus.

RDS/RBDS data output

The decoded RDS/RBDS block information and the current pre-processor status is available via the I²C-bus. For synchronization of data request between main controller and pre-processor the additional data available output signal is used.

If the decoder has processed new information for the main controller the data available signal (DAVN) is activated (LOW) under the following conditions (see also Table 5):

- During synchronization search in DAVB mode if a valid A-block has been detected. This mode can be used for fast search tuning (detection and comparison of the PI code contained in the A-block).
- During synchronization search in any DAV mode, if two blocks in correct sequence have been detected (synchronization criterion).
- If the pre-processor is synchronized and in mode DAVA and DAVB a new block has been processed. This mode is the standard data processing mode, if the decoder is synchronized.
- If the pre-processor is synchronized and in DAVC mode two new blocks have been processed.
- If the pre-processor is synchronized and in any DAV mode loss of synchronization is detected (flywheel counter overflow and resulting restart of synchronization).
- In any DAV mode, if a reset condition caused by power-on or voltage-drop is detected.

The processed RDS/RBDS data are available for I²C-bus request for at least 20 ms after the DAVN signal was activated.

The DAVN signal is always automatically deactivated (HIGH) after 10 ms or almost after the main controller has read the RDS/RBDS data via I²C-bus (see Fig.4).

The decoder ignores new processed RDS/RBDS blocks if the DAVN signal is active or if data overflow occurs (see Section “Data processing control”).

Multi-path detector

The multi-path detector takes its information from the unweighted level signal of the FM IF amplifier, input LVIN (see Fig.1). The part of frequency components around 21 kHz is selected by a band-pass filter and rectified by a full-wave rectifier. The capacitor at pin MRO is the charge capacitor. In combination with internal current sources the time constants of the rectifier are defined.

The analogous output voltage of the multi-path rectifier is buffered and available via pin MPTH.

Signal quality detector

The signal quality detector takes its information from the multiplex signal. Disturbances caused by adjacent-channel reception, noise, or multi-path, generate high frequency components (noise) on the multiplex signal besides the audible distortion.

The signal quality measurement is provided for fast testing alternative frequencies as well as for the tuned frequency. It is a short start/stop procedure. The measuring time is limited to 850 µs. To attain an average value over a longer time, multiple measurements are possible with integration by software processing.

The noise is detected from the frequency spectrum above 90 kHz. The noise voltage is selected by a 4th order high-pass filter. A full-wave rectifier, controlled by this noise voltage, charges an initially discharged capacitor (on chip). The time is measured until the voltage across the capacitor has reached a defined threshold value. Then that time equivalent value is stored. The resolution of the signal quality measurement is 4 bits (16 steps).

For operating the noise detector two modes are provided, the triggered mode and the continuous mode. The mode is defined by the bit SQCM (Signal Quality Continuous Measurement) as described in Section “Programming”.

The triggered mode is provided for a fast signal quality test of e.g. an alternative frequency. After the alternative frequency has been tuned, the signal quality detector has to be started (triggered) by transmitting the bits SQCM = 0 and TSQD = 1 via the I²C-bus (see Fig.5). This causes a single shot measurement immediately after the acknowledgement of this byte.

The bit TSQD is internally reset during the measurement (TSQD = 0). The result of the measurement is stored and is available for reading out, as long as no new measurement is started again e.g. after tuning back to the previous frequency.

The continuous mode minimizes the required I²C-bus activities for multiple measurements. After transmission of SQCM = 1 and TSQD = 1, the signal quality detector starts a new measurement as described above. But every time after finishing one measuring procedure the result is stored (overwrites the previous value within the I²C-bus buffer SQI3 to SQI0) and a new measurement starts automatically. If at any time the pre-processor is read out by his master, the last measured value will be transmitted.

After transmitting the control information SQCM = 0 and TSQD = 0, the measurement activity will be stopped. A previously started but not yet finished measurement will be completed and this last result will also be available.

The control bit combination SQCM = 1 and TSQD = 0 must not be used. It is reserved for later applications.

At a maximum time of 850 µs after triggering or automatic restart of the signal quality detector, the result of the measurement (signal quality indication) is available and represented by the four bits SQI3 to SQI0, in a value range of 0 to 15 and is available via the I²C-bus (see Section “Programming”). The result 0 characterizes no or less noise/distortion and 15 high noise/distortion.

Tolerances of the signal quality detector as well as characteristics and tolerances of the FM IF amplifier can be compensated by adjusting the sensitivity of the signal quality detector with the control bits SQS0 to SQS4. The sensitivity can be adjusted over a range of 18.6 dB (−9.0 to +9.6 dB) in steps of 0.6 dB as given in Table 10.

Pause detector

The pause detector watches the audio modulation for pauses or very low levels. This function can be used for performing inaudible RDS AF-tests if the radio is in FM mode as well as for Automatic Music Search (AMS) if the radio is in cassette mode.

The input of the pause detector (AFIN) is low-ohmic and must be current driven (negative input of an operational amplifier). This has the following advantages:

- One (MPX) as well as two (left and right) AF channel application is possible and requires only one pin
- Unwanted crosstalk is avoided if two AF channel application is chosen
- Matching the input sensitivity is possible by external resistors.

For combined application (RDS and AMS) variations of the switching threshold level as well as the minimum time for pause detection are possible via I²C-bus control.

The level can be adjusted in four steps of 4 dB by the control bits PL0 and PL1, see Table 8 (for 1 channel: R = 5 kΩ; for 2 channels: R = 10 kΩ).

The corresponding values of FM deviation are calculated for stereo decoders with an output voltage of 270 mV at 22.5 kHz deviation.

The minimum time for detecting a pause can be adjusted by the control bits SOSC, PTF0 and PTF1; see Table 9.

The minimum time for detecting 'no pause' is fixed to 5 ms to avoid interruptions of a pause by a short pulse.

The output signal of the pause detector is a digital switching signal (active LOW). It is directly available via the output pin PSWN. A detected pause may initiate an AF search if required (FM mode).

Oscillator and clock

For good performance of the band-pass and demodulator stages, the pre-processor requires a crystal oscillator with a frequency of n × 4.332 MHz. The pre-processor can be operated with one of four different oscillator frequencies (n = 1 to 4). The 17.328 MHz frequency (n = 4) is also UART interface compatible for 8051 based microcontrollers with a 9600 baud rate (frequency error = 4.5%), so that a radio set with microcontroller can run in this case with one crystal only. The pre-processor oscillator can drive the microcontroller or vice versa.

According to the used oscillator frequency, the mode control bits PTF1, PTF0 and SOSC have to be set via the I²C-bus after every reset, see Section "Programming"

The clock generator circuitry generates hereof the internally used 4.332 MHz system clock and further derived timing signals.

Power supply and reset

The pre-processor has separate power supply inputs for the digital and analog parts of the device. For the analog functions an additional reference voltage ($\frac{1}{2}V_{DDA}$) is internally generated and available via the output pin V_{ref}.

The I²C-bus interface requires a defined reset condition. The pre-processor generates a reset signal:

- After the supply voltage V_{DDD} is switched on
- At a supply voltage drop
- If the oscillator frequency is lower than 400 Hz.

This internal reset initializes the I²C-bus interface registers as well as the I²C-bus slave control and releases the data line SDA (SDA = HIGH) for input of control mode settings from the main controller.

If the decoder detects a reset condition, the status information 'reset detected' (RSTD) is set and available via I²C-bus request. The RSTD flag is deactivated after the decoder status register was read by the I²C-bus. This status information is important to signal the main controller about a voltage drop in the pre-processor IC.

By default, the bits in the write registers (except bit SOSC) are set to the values in Table 11. If these values are the required values, no further initialization is necessary.

Programming

I²C-BUS SLAVE TRANSCEIVER

For communication with the external main controller (master transceiver) the standard I²C-bus is used.

The pre-processors I²C-bus interface acts as a slave transceiver with fast mode option, that allows a transfer bit rate up to 400 kbits/s but is also capable of operating at lower rates (≤100 kbits/s).

The I²C-bus interface is connected to the external I²C-bus via the serial clock line SCL and the serial data line SDA. The clock line is supplied by the master and is only input for the slave transceiver. The data line is a serial 8-bit oriented bidirectional data transfer line, and acts as input for control mode settings from the main controller to the pre-processor, as output for requested RDS/RBDS data from the pre-processor to the main controller and acknowledge between pre-processor and main controller.

The transfer of requested data to the main controller is synchronized via the additional data available output signal DAVN to avoid loss of RDS/RBDS data. The DAVN signal is activated if the pre-processor has provided new data information for the main controller (see Section “RDS/RBDS data output”) and can be used for the polling mode as well as for the interrupt mode of the main microcontroller.

I²C-BUS INTERFACE REGISTERS

The I²C-bus interface is connected to other blocks of the pre-processor via internal registers (byte oriented). Those can either be written by the pre-processor control and read by the main controller I²C-bus or vice versa.

The device provides 3 input control registers to which may be written via the I²C-bus and 7 output registers which may be read via the I²C-bus.

The decoder control updates the output registers after the detection of a new RDS/RBDS information block and reads the new mode control settings of the input control registers. Both operations may occur in the same time slot, provided that the read operation is complete before a new RDS/RBDS data bit is processed by the demodulator.

For the corresponding access the registers are addressed by two separate register pointers, write-enable and read-enable signals, which are activated either via the decoder control or via the I²C-bus interface control.

During a read or write transmission from the I²C-bus the read/write pointer selects the register of the first byte for transmission and is auto-incremented by the I²C-bus control for the transfer of subsequent bytes.

During a write transmission after reception of the device slave address and write bit, the mode control settings for the pre-processor have to be send in the protocol sequence as shown in Table 1 and Fig.5.

During a read cycle after reception of the device slave address and read bit the requested RDS/RBDS data has to be received in the protocol sequence as given in Table 2 and Fig.7.

Table 1 Input control registers

DATA	FUNCTION
Byte 0_W	initialization and mode control setting; see Table 3
Byte 1_W	pause level and flywheel setting; see Table 6
Byte 2_W	pause time/oscillator frequency and quality detector sensitivity setting; see Table 7

Table 2 Output registers

DATA	FUNCTION
Byte 0_R	decoder and data status information; see Table 12
Byte 1_R	last processed block (HIGH byte); see Table 15
Byte 2_R	last processed block (LOW byte); see Table 15
Byte 3_R	previously processed block (HIGH byte); see Table 15
Byte 4_R	previously processed block (LOW byte); see Table 15
Byte 5_R	error status information; see Table 15
Byte 6_R	signal quality indication; see Table 15

WRITE TRANSMISSION FORMAT

Table 3 Description of initialization and mode control byte (byte 0_W)

BIT	NAME	FUNCTION
7	SQCM	0: triggered signal quality measurement
		1: signal quality continuous measurement
6	TSQD	0: no determination of signal quality
		1: trigger of signal quality detector measurement
5	NWSY	0: normal processing mode
		1: restart of synchronization
4	SYM1	selection of error correction mode for synchronization search; see Table 4
3	SYM0	
2	RBDS	0: RDS processing mode
		1: RBDS processing mode
1	DAC1	selection of data output protocol and indirectly control of data available output signal (DAVN); see Table 5
0	DAC0	

Table 4 Selection of error correction mode for synchronization search

SYM1	SYM0	MODE	DESCRIPTION
0	0	SYNCA	no error correction
0	1	SYNCB	error correction of a burst error maximum 2 bits
1	0	SYNCC	error correction of a burst error maximum 5 bits
1	1	SYNCD	no error correction; no E-E block sequence allowed (for RBDS mode, E-A or D-E block sequences are still allowed)

Table 5 Selection of data output protocol and DAVN signal

DAC1	DAC0	MODE	FUNCTION	DESCRIPTION
0	0	DAVA	standard processing mode	RDS standard output mode; synchronization search: DAVN = HIGH; synchronized: block information available and DAVN active after detection of a new block (every 26 bits)
0	1	DAVB	fast PI search mode	synchronization search: for fast PI search, block information available and DAVN active only if a correct A-block is detected; synchronized: same as standard DAVA mode
1	0	DAVC	reduced data request processing mode	synchronization search: DAVN inactive = HIGH; synchronized: block information available and DAVN active only after detection of two new blocks (every 52 bits)
1	1	–	–	–

Table 6 Description of pause level and flywheel setting bytes (byte 1_W)

BIT	NAME	FUNCTION
7	PL1	level sensitivity for pause detection; see Table 8
6	PL0	
5 to 0	FEB5 to FEB0	maximum number of error blocks for synchronization hold flywheel (0 to 63)

Table 7 Description of pause time/oscillator frequency and quality detector sensitivity setting (byte 2_W)

BIT	NAME	FUNCTION
7	PTF1	time criteria for pause (20 to 160 ms); see Table 9 oscillator frequency: n × 4.332 MHz (n = 1 to 4); see Table 9
6	PTF0	
5	SOSC	0: set pause time criteria via PFT1 and PFT0
		1: select oscillator frequency via PFT1 and PFT0
4 to 0	SQS4 to SQS0	adjustment of signal quality detector sensitivity (–9 to +9.6 dB); see Table 10

Table 8 Control bits PL0 and PL1

PL1	PL0	PAUSE LEVEL (mV RMS)	BELOW DOLBY LEVEL (dB)	FM DEVIATION (kHz)
0	0	11	30.2	1.0
0	1	17	26.2	1.6
1	0	27	22.2	2.5
1	1	43	18.2	4.0

Table 9 Control bits SOSC, PTF0 and PTF1

SOSC	PTF1	PTF0	SOSC = 0	SOSC = 1
			MINIMUM TIME (ms)	OSCILLATOR FREQUENCY (MHz)
0	0	0	20.2	4.332 (n = 1)
0	0	1	40.4	8.664 (n = 2)
0	1	0	80.8	12.996 (n = 3)
0	1	1	161.7	17.328 (n = 4)

Table 10 Control bits SQS0 to SQS4

SQS						CORRECTION (dB)
SQS4	SQS3	SQS2	SQS1	SQS0	HEX	
0	0	0	0	0	00	−9.0
0	0	0	0	1	01	−8.4
0	0	0	1	0	02	−7.8
0	0	0	1	1	03	−7.2
0	0	1	0	0	04	−6.6
0	0	1	0	1	05	−6.0
0	0	1	1	0	06	−5.4
0	0	1	1	1	07	−4.8
0	1	0	0	0	08	−4.2
0	1	0	0	1	09	−3.6
0	1	0	1	0	0A	−3.0
0	1	0	1	1	0B	−2.4
0	1	1	0	0	0C	−1.8
0	1	1	0	1	0D	−1.2
0	1	1	1	0	0E	−0.6
0	1	1	1	1	0F	0
1	0	0	0	0	10	+0.6
1	0	0	0	1	11	+1.2
1	0	0	1	0	12	+1.8
1	0	0	1	1	13	+2.4
1	0	1	0	0	14	+3.0
1	0	1	0	1	15	+3.6
1	0	1	1	0	16	+4.2
1	0	1	1	1	17	+4.8
1	1	0	0	0	18	+5.4
1	1	0	0	1	19	+6.0
1	1	0	1	0	1A	+6.6
1	1	0	1	1	1B	+7.2
1	1	1	0	0	1C	+7.8
1	1	1	0	1	1D	+8.4
1	1	1	1	0	1E	+9.0
1	1	1	1	1	1F	+9.6

Table 11 Default values of the write register bits after reset

BIT	VALUE	COMMENTS
SQCM	0	triggered signal quality measurement
TSQD	0	no determination of signal quality
NWSY	1	restart of synchronization
SYM1 and SYM0	00	no error correction during synchronization
RBDS	0	RDS processing mode
PL1 and PL0	00	pause level 12 mV
DAC1 and DAC0	00	DAVA mode RDS standard output mode
FEB5 to FEB0	100000	flywheel = 32 decimal
PTF1 and PTF0	00	oscillator frequency = 4.332 MHz (SOSC = 1); pause time = 20.2 ms (SOSC = 0)
SQS4 to SQS0	01111	gain = 0 dB

READ TRANSMISSION FORMAT

Table 12 Description of decoder and data status information byte (byte 0_R)

BYTE	BIT	NAME	FUNCTION
0_R	7 to 5	BL2 to BL0	block identification number of last processed block; see Table 13
	4	SYNC	0: not synchronized
			1: synchronized
	3	DOFL	0: no data overflow
			1: data overflow detected
	2	RSTD	0: no reset detected
			1: reset detected
	1	ELB1	error status of last processed block; see Table 14
	0	ELB0	

Table 13 Block identification number (last detected block)

BL2/ BP2	BL1/ BP1	BL0/ BP0	BLOCK IDENTIFICATION
0	0	0	block A
0	0	1	block B
0	1	0	block C
0	1	1	block D
1	0	0	block C’
1	0	1	block E (RBDS mode)
1	1	0	invalid block E (RDS mode)
1	1	1	invalid block

Table 14 Processed error correction

ELB1/ EPB1	ELB0/ EPB0	MODE	DESCRIPTION
0	0	ERDA	no errors detected
0	1	ERDB	burst error of maximum 2 bits corrected
1	0	ERDC	burst error of maximum 5 bits corrected
1	1	ERDD	uncorrectable block

Table 15 Bytes 1_R to 6_R

BYTE	BIT	NAME	FUNCTION
1_R	7 to 0	M15 to M08	HIGH byte of last processed block
2_R	7 to 0	M07 to M00	LOW byte of last processed block
3_R	7 to 0	PM15 to PM08	HIGH byte of previously processed block
4_R	7 to 0	PM07 to PM00	LOW byte of previously processed block
5_R	7 to 2	BEC5 to BEC0	number of counted block errors (0 to 63)
	1	EPB1	error status of previously processed block; see Table 14
	0	EPB0	
6_R	7 to 5	BP2 to BP0	block identification number of previous processed block; see Table 13
	4	–	not used (undefined)
	3 to 0	SQI3 to SQI0	signal quality indication (0 to 15)

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		0	6.5	V
V_n	voltage at pins 1 to 5, 8 to 13, and 16 to 20 with respect to pins 6 and 15		−0.5	V_{DD} + 0.5 ≤ 6.5	V
$V_{i(MPX)(p-p)}$	input voltage at pin MPX (peak-to-peak value)	note 1	−	6	V
I_i	input current				
	pins 1 to 5, 8, 10 to 13 and 16 to 20		−10	+10	mA
	pin 9		−20	+20	mA
$I_{lu(prot)}$	latch-up protection current in pulsed mode	T_{amb} = −40 to +85 °C with voltage limiting −2 to +10 V	−100	+100	mA
		T_{amb} = 25 °C with voltage limiting −2 to +12 V	−200	+200	mA
		T_{amb} = −40 to +85 °C without voltage limiting	−10	+10	mA
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−65	+150	°C
V_{es}	electrostatic handling	note 2	−4000	+4000	V
		note 3	−250	+250	V

Notes

1. Without latching in the entire temperature range.
2. Human body model (equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor). Except pin 17: −4000 V minimum and +2500 V maximum.
3. Machine model (equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor and 0.75 μH inductance).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	SAA6588T (SOT163-1)		85	K/W
	SAA6588 (SOT146-1)		62	K/W

CHARACTERISTICS DIGITAL PART

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	6.0	–	mA
P_{tot}	total power dissipation		–	70	–	mW
Inputs						
V_{IL1}	LOW-level input voltage at pins TCON, OSCI and MAD		–	–	$0.3V_{DDD}$	V
V_{IL2}	LOW-level input voltage at pins SCL and SDA	V_{DDD} = 4.5 to 5.0 V	–0.5	–	+1.5	V
		V_{DDD} = 5.0 to 5.5 V	–0.5	–	$+0.3V_{DDD}$	V
V_{IH1}	HIGH-level input voltage at pins TCON, OSCI and MAD		$0.7V_{DDD}$	–	–	V
V_{IH2}	HIGH-level input voltage at pins SCL and SDA	V_{DDD} = 4.5 to 5.5 V	3.0	–	V_{DDD} + 0.5	V
$\lvert I_{LI} \rvert$	input leakage current at pins TCON, SCL and SDA	V_{MAD} = 0 to V_{DDD}	–	–	10	µA
$I_{i(pu)}$	input pull-up current at pin MAD	$V_{MAD} = V_{IL1}$	–30	–20	–	µA
		V_{MAD} = 3.5 V	–	–20	–10	µA
Outputs						
V_{OL1}	LOW-level output voltage at pins DAVN, PSWN and OSCO	I_{OL} = 2 mA	–	–	0.4	V
V_{OL2}	LOW-level output voltage at pin SDA	I_{OL1} = 4.0 mA	–	–	0.4	V
		I_{OL2} = 6.0 mA	–	–	0.6	V
V_{OH}	HIGH-level output voltage at pins DAVN, PSWN and OSCO	I_{OH} = –2 mA	4.0	–	–	V
Crystal parameters						
$f_{i(xtal)}$	crystal input frequency	n = 1	–	4.332	–	MHz
		n = 2	–	8.664	–	MHz
		n = 3	–	12.996	–	MHz
		n = 4	–	17.328	–	MHz
$\lvert \Delta f_{osc} \rvert$	adjustment tolerance of oscillator frequency		–	–	30	ppm
$\lvert \Delta f_{osc(T)} \rvert$	temperature drift of oscillator frequency	T_{amb} = –40 to +85 °C	–	–	30	ppm
C_L	load capacitance		–	30	–	pF
R_{xtal}	crystal resonance resistance	$f_{osc} \leq 12.996$ MHz	–	–	120	Ω
		f_{osc} = 17.328 MHz	–	–	60	Ω

CHARACTERISTICS ANALOG PART

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = 25$ °C; measurements taken in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
$\lvert V_{DDA} - V_{DDD} \rvert$	voltage difference between analog and digital supply		–	0	0.5	V
$I_{DD(tot)}$	total supply current		–	14.0	–	mA
V_{ref}	reference voltage	$V_{DDA} = 5$ V	2.25	2.5	2.75	V
$Z_{o(Vref)}$	output impedance at pin V_{ref}		–	25	–	kΩ
MPX input (signal before the capacitor on pin MPX)						
$V_{i(MPX)(rms)}$	RDS amplitude (RMS value)	$\Delta f = \pm 1.2$ kHz RDS signal; $\Delta f = \pm 3.2$ kHz spurious signal	1	–	–	mV
$V_{i(max)(p-p)}$	maximum input signal capability (peak-to-peak value)	f = 57 ±2 kHz	200	–	–	mV
		f < 50 kHz	1.4	–	–	V
		f < 15 kHz	2.8	–	–	V
		f > 70 kHz	3.5	–	–	V
$R_{i(MPX)}$	input resistance	f = 0 to 100 kHz	33	–	–	kΩ
57 kHz band-pass filter						
f_c	centre frequency	$T_{amb} = -40$ to +85 °C	56.5	57.0	57.5	kHz
B_{-3dB}	−3 dB bandwidth		2.5	3.0	3.5	kHz
G_{MPX}	signal gain	f = 57 kHz	17	20	23	dB
α_{sb}	stop band attenuation	$\Delta f = \pm 7$ kHz	31	–	–	dB
		f < 45 kHz	40	–	–	dB
		f < 20 kHz	50	–	–	dB
		f > 70 kHz	40	–	–	dB
$R_{o(SCOUT)}$	output resistance at pin SCOUT	f = 57 kHz	–	30	60	Ω
Comparator input (pin CIN)						
$V_{i(min)(rms)}$	minimum input level (RMS value)	f = 57 kHz	–	1	10	mV
R_i	input resistance		70	110	150	kΩ
Multi-path detector (pins LVIN, MPTH and MRO)						
$Z_{i(LVIN)}$	input impedance at pin LVIN	f = 21 kHz	24	30	36	kΩ
$V_{i(LVIN)}$	input voltage at pin LVIN		1.0	2.5	4.0	V
$f_{c(MPD)}$	centre frequency of the multi-path detector band-pass filter		20	21	22	kHz
B_{MPD}	bandwidth of the multi-path detector band-pass filter		3.6	4.0	4.4	kHz
α_{sb}	stop band attenuation	f = 11 kHz	16	–	–	dB
		f = 31 kHz	12	–	–	dB
$t_{att(MRO)}$	attack time of the rectifier	C6 = 100 nF; R4 = 470 kΩ	–	6.4	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{dec(MRO)}$	decay time of the rectifier	C6 = 100 nF; R4 = 470 kΩ	–	50	–	ms
$G_{v(MPTH)}$	rectifier voltage gain; $G_{v(MPTH)} = 20 \log \frac{V_{MPTH(DC)}}{V_{LVIN(rms)}}$	$V_{LVIN(rms)}$ = 0.1 V; f_{LVIN} = 21 kHz	–	20	–	dB
$Z_{o(MPTH)}$	output impedance at pin MPTH		150	200	250	Ω
$V_{o(MPTH)}$	output voltage swing at pin MPTH		0.5	–	3.5	V
$Z_{L(MPTH)}$	load impedance at pin MPTH	with respect to ground	5	–	–	kΩ
$C_{L(MPTH)}$	load capacitance at pin MPTH	with respect to ground	–	–	20	pF
Signal quality detector (pin MPX)						
f_{co}	cut-off frequency		85	90	95	kHz
PBRR	pass-band ripple rejection		–	–	1	dB
α_{sb}	stop band attenuation	f = 40 kHz	30	–	–	dB
$V_{STEP2-3(rms)}$	input voltage (RMS value) for transition of signal quality indication between step 2 and 3 (SQI = 0010 and 0011)	sensitivity = 0 dB (SQS = 01111; see Table 10); f = 100 kHz	–	85	–	mV
ΔG_{SQ}	step size for signal quality input gain		0.4	0.6	0.8	dB
CR_{GSQ}	control range for signal quality input gain		15.6	18.6	21.6	dB
t_{SQD}	measuring time	after acknowledgement of the I^2C-bus transceiver	–	–	850	µs
Pause detector (pins AFIN and PSWN)						
$Z_{i(AFIN)}$	input impedance	f = 10 kHz	–	–	10	Ω
$V_{I(AFIN)}$	DC input voltage	unloaded	–	V_{ref}	–	V
$I_{th(rms)}$	AC input current for threshold (RMS value)	PL1 = 1; PL0 = 1	3.1	4.4	6.2	µA
$TH_{pause(step)}$	step size for pause threshold		3	4	5	dB
$TH_{pause(R)}$	control range for pause threshold		10	12	14	dB
$I_{i(offset)}$	input offset current		–	–	0.4	µA
$t_{PON(min)}$	minimum time for pause	PT1 = 0; PT0 = 0	–	20.2	–	ms
		PT1 = 0; PT0 = 1	–	40.4	–	ms
		PT1 = 1; PT0 = 0	–	80.8	–	ms
		PT1 = 1; PT0 = 1	–	161.7	–	ms
$t_{POFF(min)}$	minimum time for no pause		–	5	–	ms
Δt	time error (all values)		–	–	1.0	ms

I²C-BUS PROTOCOL

I²C-bus format

In communication with the pre-processor two basic types of I²C-bus protocols are allowed (see Tables 16 and 17).

Every transmission begins with a START condition ‘S’ followed by the 7-bit slave address and the R/$\overline{W}$ mode bit, all generated by the external master.

The 6 higher bits of the pre-processors slave address are fixed to 001000. The least significant bit of the slave address can be set via the external input pin MAD to enable a variation if the slave address is already occupied by another device of the radio set. Data is transferred with the most significant bit (MSB) first.

Each transmitted byte is followed by an acknowledge bit ‘A’ (SDA = LOW). Every transmission is completed with a STOP condition ‘P’ generated by the master.

During read or write transfer the master can abridge the data transfer by generation of a STOP condition. In case of transmission errors during a write cycle, the pre-processor can indirectly stop the transfer by generating no acknowledge (SDA = HIGH) hereafter the master can send the STOP condition.

Table 16 Transmitting to the pre-processor (write transfer)

S[1]	SLAVE ADDRESS[2]	$\overline{W}$[3]	A[4]	DATA[5]	A[4]	DATA[5]	A[4]	DATA[5]	A[4]	P[6]

Notes

1. S = START condition.
2. Slave address (depends on level at pin MAD) = 0010000 or 0010001.
3. W = write mode.
4. A = acknowledge bit (SDA = LOW).
5. Subsequently data bytes 0_W, 1_W and 2_W.
6. P = STOP condition.

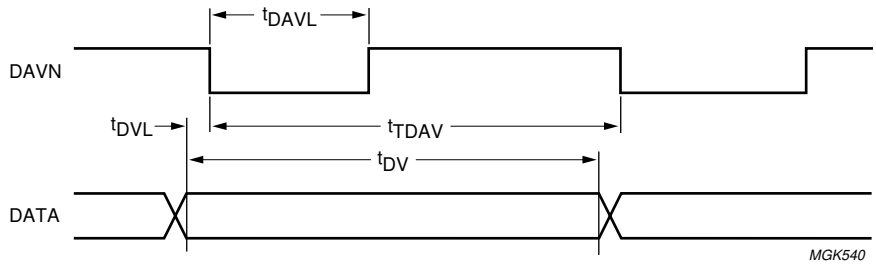
Table 17 Receiving from the pre-processor (read transfer)

S[1]	SLAVE ADDRESS[2]	R[3]	A[4]	DATA[5]	A[4]	DATA[5]	$\overline{A}$[6]	P[7]

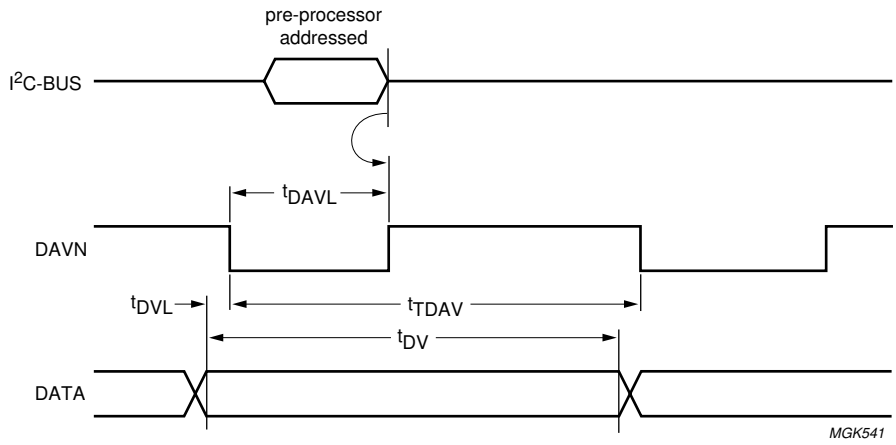
Notes

1. S = START condition.
2. Slave address (depends on level at pin MAD) = 0010000 or 0010001.
3. R = read mode.
4. A = acknowledge bit (SDA = LOW). Six DATA-acknowledge sequences must occur before the DATA-not acknowledge sequence.
5. Subsequently data bytes 0_R to 6_R.
6. $\overline{A}$ = no acknowledge (SDA = HIGH).
7. P = STOP condition.

Timing data



a. No I²C-bus request during DAVN LOW-time (decoder is synchronized).



b. DAVN LOW-time shortened by data-request via I²C-bus (decoder is synchronized).

Fig.4 Data available signal (DAVN).

Table 18 Data available signal (DAVN)

SYMBOL	PARAMETER	TYP.	UNIT
t_{DVL}	data valid to DAVN LOW	2.0	µs
t_{TDAV}	data valid period	21.9	ms
t_{DV}	data valid	21.9	ms
t_{DAVL}	data available signal is LOW	10.1(1)	ms
		depends on data request via I²C-bus(2)	ms

Notes

1. See Fig.4a.
2. See Fig.4b.

PROGRAMMING AND I²C-BUS SUMMARY

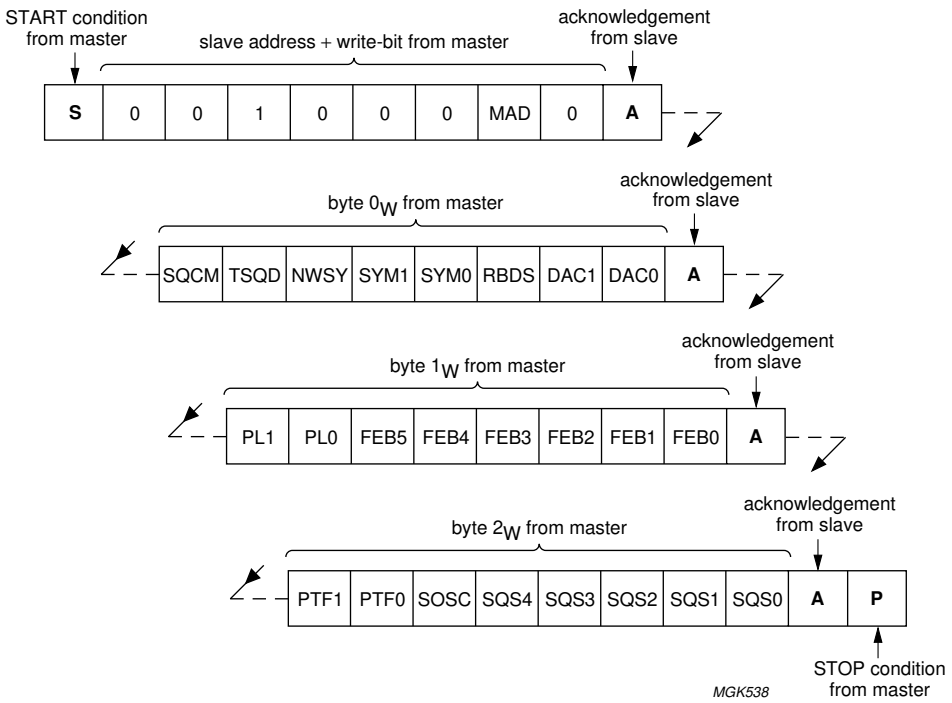


Fig.5 RDS pre-processor control commands: mode control and preset settings for the pre-processor.

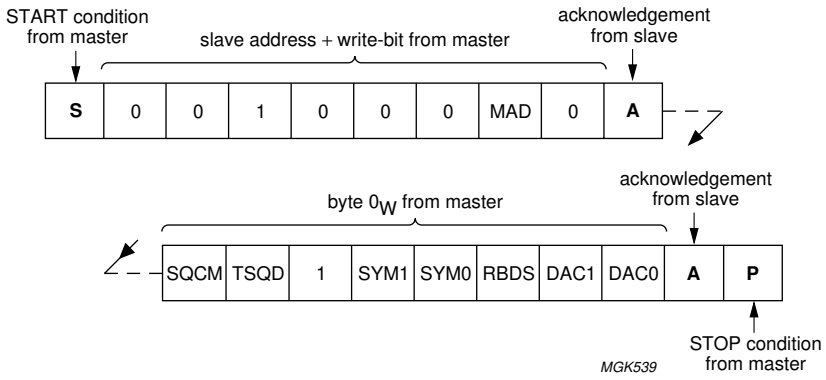


Fig.6 RDS pre-processor control commands: abridged protocol, for example for immediate restart synchronization.

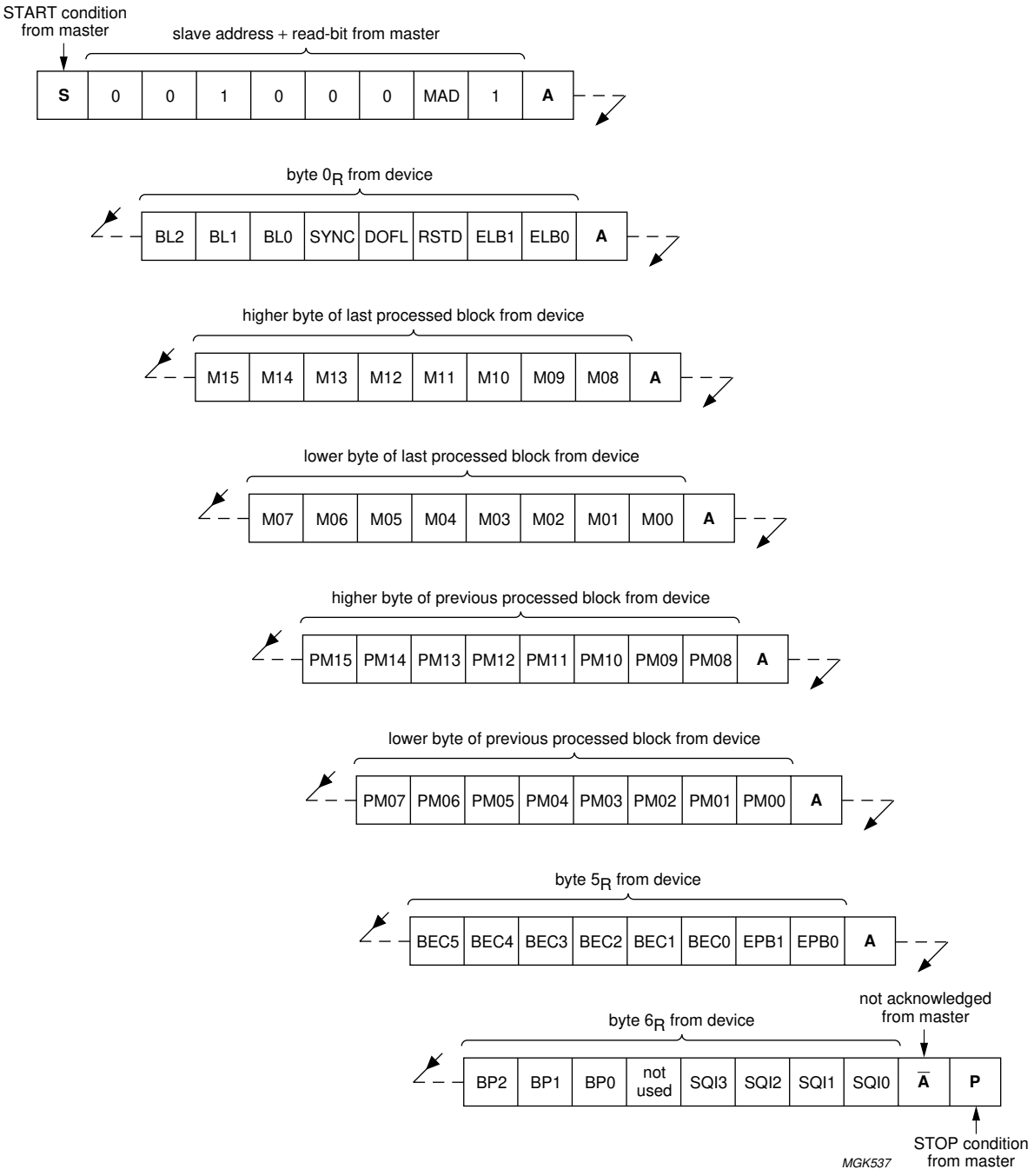


Fig.7 Data output protocol (RDS data output).

APPLICATION DIAGRAM

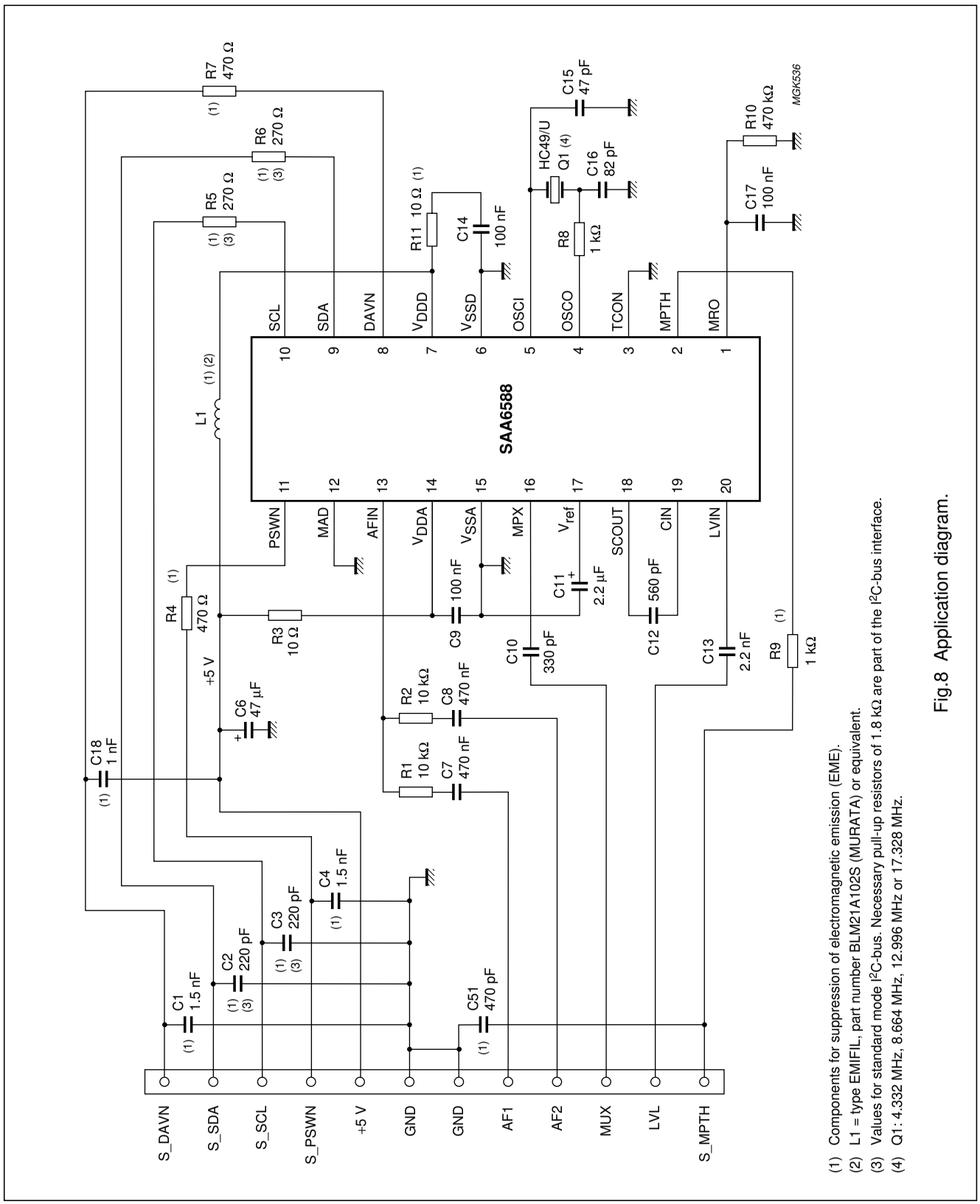
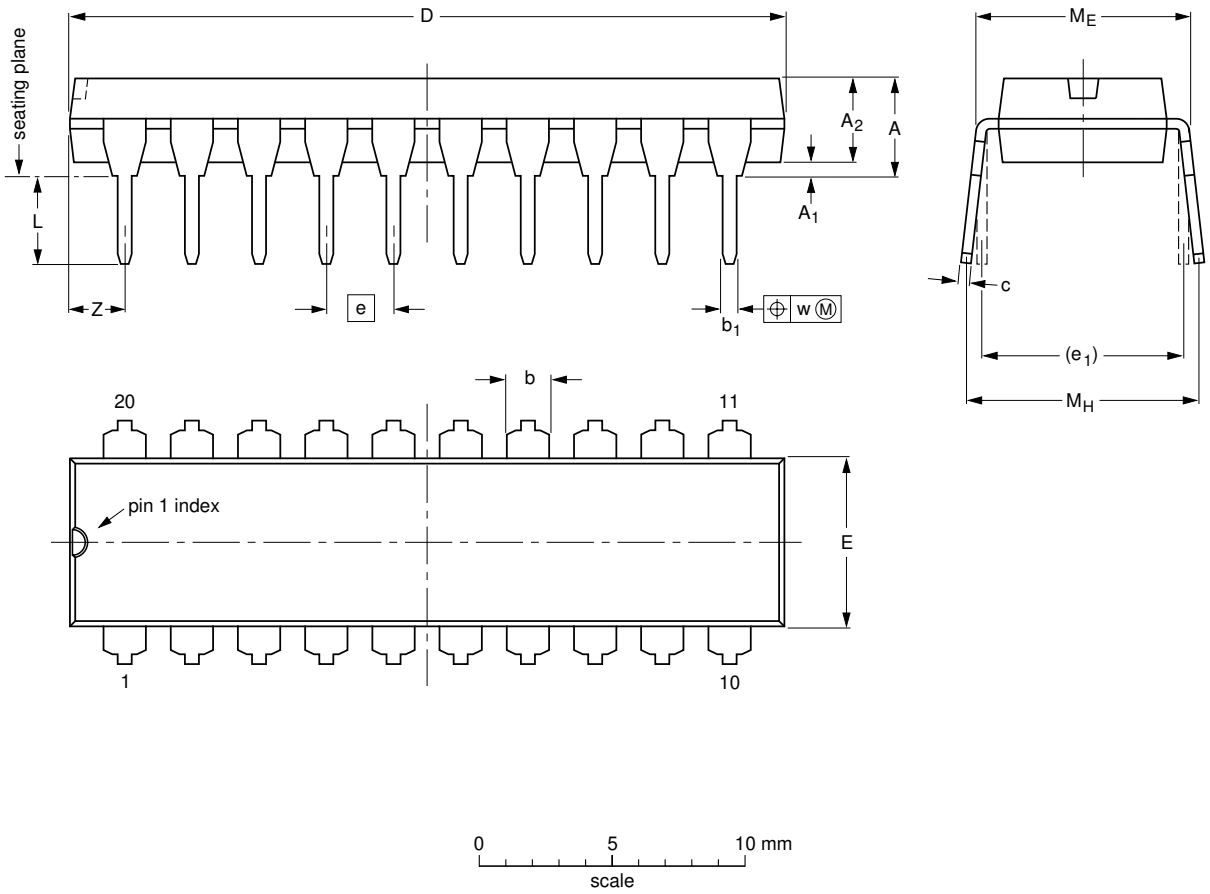


Fig.8 Application diagram.

(1) Components for suppression of electromagnetic emission (EME).
(2) L1 = type EMIFIL, part number BLM21A102S (MURATA) or equivalent.
(3) Values for standard mode I²C-bus. Necessary pull-up resistors of 1.8 kΩ are part of the I²C-bus interface.
(4) Q1: 4.332 MHz, 8.664 MHz, 12.996 MHz or 17.328 MHz.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

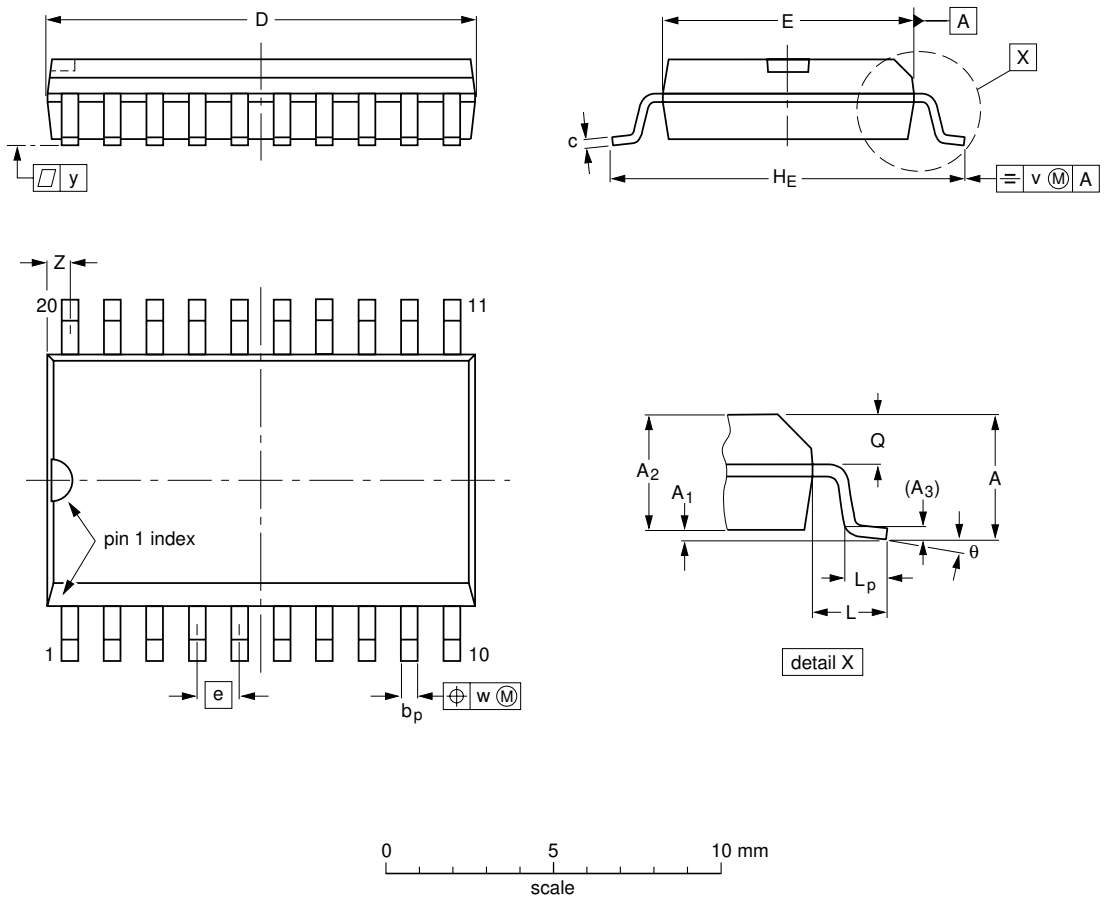
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27