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DATA SHEET



SAA6752HS MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

Product specification
Supersedes data of 2002 Dec 09

2004 Jan 26

**MPEG-2 video and MPEG-audio/AC-3
audio encoder with multiplexer****SAA6752HS**

CONTENTS	8	BOUNDARY SCAN TEST
1	FEATURES	8.1 Initialization of boundary scan circuit
1.1	Video input and preprocessing	8.2 Device identification codes
1.2	Video compression	9 I²C-BUS CONTROL AND STATUS REGISTERS
1.3	Audio input	10 LIMITING VALUES
1.4	Audio compression	11 THERMAL CHARACTERISTICS
1.5	Stream multiplexer	12 CHARACTERISTICS
1.6	Output interface	13 PACKAGE OUTLINE
1.7	Control domain	14 SOLDERING
1.8	Other features	14.1 Introduction to soldering surface mount packages
2	GENERAL DESCRIPTION	14.2 Reflow soldering
2.1	General	14.3 Wave soldering
2.2	Application fields	14.4 Manual soldering
3	QUICK REFERENCE DATA	14.5 Suitability of surface mount IC packages for wave and reflow soldering methods
4	ORDERING INFORMATION	15 DATA SHEET STATUS
5	BLOCK DIAGRAM	16 DEFINITIONS
6	PINNING	17 DISCLAIMERS
7	FUNCTIONAL DESCRIPTION	18 PURCHASE OF PHILIPS I²C COMPONENTS
7.1	System operation	
7.2	Digital video input	
7.3	Video compression	
7.4	Digital audio input	
7.5	Audio compression	
7.6	SDRAM interface	
7.7	Multiplexer	
7.8	MPEG stream output port	
7.9	Clock generation	
7.10	Power control and reset	
7.11	I ² C-bus interface	
7.12	Exception handling	

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

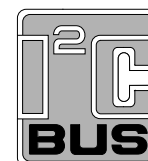
1 FEATURES

1.1 Video input and preprocessing

- Digital YUV input according to "ITU-R BT.656" (8 bits at 27 MHz) and "ITU-R BT.601"
- Support of enhanced "ITU-R BT.656" input format containing decoded VBI data readable via I²C-bus; Closed Caption (CC), Wide Screen Signalling (WSS) and copyright information with Copy Generation Management System (CGMS)
- Processing of non-broadcast video signals from analog VCR according to IEC 756
- Two video clock input pins for switching two digital video sources
- "ITU-R BT.601" format conversion to 1/2D1, 2/3D1 and Standard Interchange Format (SIF)
- 4 : 2 : 2 to 4 : 2 : 0 colour format conversion
- Decimation filtering for all format conversions
- Adaptive median filter and motion compensated filter for input noise reduction.

1.2 Video compression

- Real-time MPEG-2 encoding compliant to Main Profile at Main Level (MP@ML) for 625 and 525 interlaced line systems
- Supported resolutions: D1, 2/3D1, 1/2D1 and SIF
- IPB frame, IP frame and I frame only encoding supported at all modes
- Supported bit rates: up to 25 Mbit/s I-only encoding; up to 15 Mbit/s IP-only or IBP encoding.
- Variable video bit rate mode for constant picture quality and constant bit rate mode to gain optimum picture quality from a fixed channel transfer rate
- Access to bit rate control parameters whilst encoding to support external real-time control algorithms (e.g. constrained variable bit rate control)
- Programmable Group Of Pictures (GOP) structure
- Innovative motion estimation with wide search range
- Adaptive quantization
- Motion compensated noise filter.



1.3 Audio input

- Audio inputs: I²S format or EIAJ format (16, 18 or 20 bits), master or slave mode at 32, 44.1 and 48 kHz
- Two digital I²S input ports for selection between two digital audio sources
- Audio clock generation: 256f_s or 384f_s (where f_s = 48 kHz) locked to video frame rate (if video is present and locking is enabled)
- Sample rate conversion to 48 kHz (locked to video frame rate if enabled) for slave mode operation in all modes except Digital Versatile Disc (DVD) compliant bypass.

1.4 Audio compression

- Dolby[®](1) Digital Consumer Encoding (DDCE) also known as AC-3⁽²⁾ 2 channel audio encoding at 256 kbit/s or 384 kbit/s (only for SAA6752HS/V103)
- MPEG-1 layer 2 audio encoding at 256 kbit/s or 384 kbit/s
- Input data bypass for Linear Pulse Code Modulation (LPCM) and compressed audio data [MPEG-1, MPEG-2, Dolby[®] Digital (DD) and Digital Theatre System (DTS)] according to IEC 61937
- Preamble Pc, Preamble Pd and bit stream information captured for identification of modes during bypass of compressed audio data for MPEG-1, MPEG-2, DD and DTS according to IEC 61937
- Audio mute via I²C-bus control for all modes except DVD-compliant bypass.

(1) Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

(2) AC-3 is a registered trademark of Dolby Laboratories Licensing Corporation.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

1.5 Stream multiplexer

- Multiplexing of video and audio streams according to the MPEG-2 systems standard ("*ISO 13818-1*")
- Generation and output of MPEG-2 Transport Streams (TS), MPEG-2 Program Streams (PS), Packetized Elementary Streams (PES) and Elementary Streams (ES) compliant to the DVD, D-VHS and DVB standards
- MPEG time stamp (PTS/DTS/SCR/PCR) generation and insertion (synchronization)
- Insertion of metadata
- Optional generation of empty time slots for subsequent insertion of application specific data packets
- Optional insertion of user data in the GOP header and in the picture header
- Optional automatic insertion of Closed Caption data according to DVD or ATSC standard
- Optional generation of transport streams with variable bit rate.

1.6 Output interface

- Parallel interface 8-bit master/slave output
- 3-state output port
- Glueless interfacing with IEEE 1394 chip sets (for example, PDI 1394 L11)
- Data Expansion Bus Interface (DEBI) interface.

1.7 Control domain

- All control done via I²C-bus
- I²C-bus slave transceiver up to 400 kbit/s
- I²C-bus slave address select pin
- Host interrupt flag pin.

1.8 Other features

- Single external clock or single crystal 27 MHz
- Separate 27 MHz system clock output
- Interface voltage 3.3 V
- TTL compatible digital outputs
- Power supply voltage 3.3 and 2.5 V
- Boundary Scan Test (BST) supported
- Power-down mode
- Single SDRAM system memory (16 Mbit@16 bit or 64 Mbit@16 bit).

2 GENERAL DESCRIPTION

2.1 General

Philips Semiconductors' second generation real time MPEG-2 encoder, the SAA6752HS, is a highly integrated single-chip audio and video encoding solution with flexible multiplexing functionality. With our expertise in two critical areas for consumer video encoding, noise filtering and motion estimation, we have pushed the boundaries for video quality even further, providing enhanced quality for low bit rates and enabling increased recording times for a given storage capacity. The SAA6752HS will also enable a key driver for new consumer digital recording applications and system cost reduction. By integrating all audio encoding and multiplexing functionality we will be moving from a three chip to a one chip system, with cost efficient design and process technology, thus providing a truly low cost, high quality encoding system.

The SAA6752HS/V104 is intended for customers whose application does not require the DDCE function.

The SAA6752HS gives significant advantages to customers developing digital recording applications:

- **Fast time-to-market and low development resources.** By adding a simple external video input processor IC, an audio analog-to-digital converter, and an external SDRAM, analog video and audio sources are compressed into high quality MPEG-2 video and MPEG-1 layer 2 or AC-3 audio streams, multiplexed into a single program or transport stream for simple connection to various storage media or broadcast media. Hence, making design effort for our customers a minimum, as well as removing the need for in-depth experience in MPEG encoding.
- **Low system host resources.** All video and audio encoding algorithms and software are run on an internal MIPS^{®(1)} processor. The SAA6752HS only requires a small amount of communication from the system host processor to set up and control required encoding parameters via the I²C-bus.

(1) MIPS is a registered trademark of MIPS Technologies.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

2.2 Application fields

2.2.1 DVD BASED OPTICAL DISC RECORDERS (DVD+RW, DVD-RW, DVD-RAM)

Emerging optical disc based recording systems target to replace the existing consumer recording (VCR) and playback (DVD and VCD) products. The first generation recordable DVD based products will want to maximise recording times for the 4.7 Gbyte storage capacity. For these systems the SAA6752HS is critical, with its superior noise filtering and motion estimation, in enabling high quality at low bit rates.

Playback compatibility with existing DVD decoding solutions will also be important, which is why the SAA6752HS provides Dolby® digital consumer (AC-3) audio encoding to allow playback through existing players implementing DDCE (AC-3) decoding dominant in current DVD platforms.

The DVD stream is based on MPEG Program Stream (PS). The SAA6752HS directly outputs MPEG PS compliant to the DVD standard.

2.2.2 HDD BASED TIME SHIFT RECORDING

Hard Disc Drive (HDD) based time-shift systems enable Personalized TV (PTV) functionality, providing consumers with new powers of control over what and when to watch broadcast content. With the audio and video content recorded digitally, identification, search and retrieval becomes a 'no brainer' task as compared to traditional VCR functionality. Combine this with electronic program guides and intelligent control, and the PTV can also analyse the viewers watching habits to search for programs likely to be of interest and automatically recorded in anticipation of the viewers preferences.

Since HDD recorders are closed systems, the recording format stream can be proprietary. The SAA6752HS flexible multiplexing formats support a number of recording stream formats for HDD including MPEG Transport Stream (TS) or MPEG Packetized Elementary Stream (PES).

2.2.3 DIGITAL VCR (DVHS) RECORDING

A DVHS player records streams based on MPEG Transport Streams (TS) packed in logical tape tracks. The SAA6752HS output streams are compliant with DVHS standard requirements.

2.2.4 VIDEO EDITING/TRANSMISSION/SURVEILLANCE/ CONFERENCING

The SAA6752HS can operate as a stand-alone device in all the above applications. The SAA6752HS full features and flexibility allows customers to tailor functionality and performance to specific application requirements. All required control settings such as GOP size and bit rate modes can be selected via the I²C-bus.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DDP}	digital supply voltage (pad cells)	3.0	3.3	3.6	V
V _{DDCO}	digital supply voltage (core)	2.3	2.5	2.7	V
V _{DDA}	analog supply voltage (oscillator and PLL)	2.3	2.5	2.7	V
I _{DD(tot)}	total analog plus digital supply current	407	453	525	mA
P _{tot}	total power dissipation	0.95	1.16	1.48	W
f _{DCXO}	quartz frequency (digital controlled tuning)	27 × [1 - (200 × 10 ⁻⁶)]	27	27 × [1 + (200 × 10 ⁻⁶)]	MHz
f _{SDRAM}	SDRAM clock frequency	–	108	–	MHz
f _{SCL}	I ² C-bus input clock frequency	100	–	400	kHz
B	output bit-rate	1.5	–	25	Mbit/s
V _{IH}	HIGH-level digital input voltage	1.7	–	3.6	V
V _{IL}	LOW-level digital input voltage	–0.5	–	+0.7	V
V _{OH}	HIGH-level digital output voltage	V _{DDP} – 0.4	–	V _{DDP}	V
V _{OL}	LOW-level digital output voltage	0	–	0.4	V
T _{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6752HS/V103 ⁽¹⁾⁽³⁾	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT316-1
SAA6752HS/V104 ⁽²⁾⁽⁴⁾			

Notes

1. MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer.
2. MPEG-2 video and MPEG-audio encoder with multiplexer, but without AC-3 audio encoder.
3. SAA6752HS/V103 is a replacement of SAA6752HS/V101 with enhanced functionality.
4. SAA6752HS/V104 is a replacement of SAA6752HS/V102 with enhanced functionality.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

5 BLOCK DIAGRAM

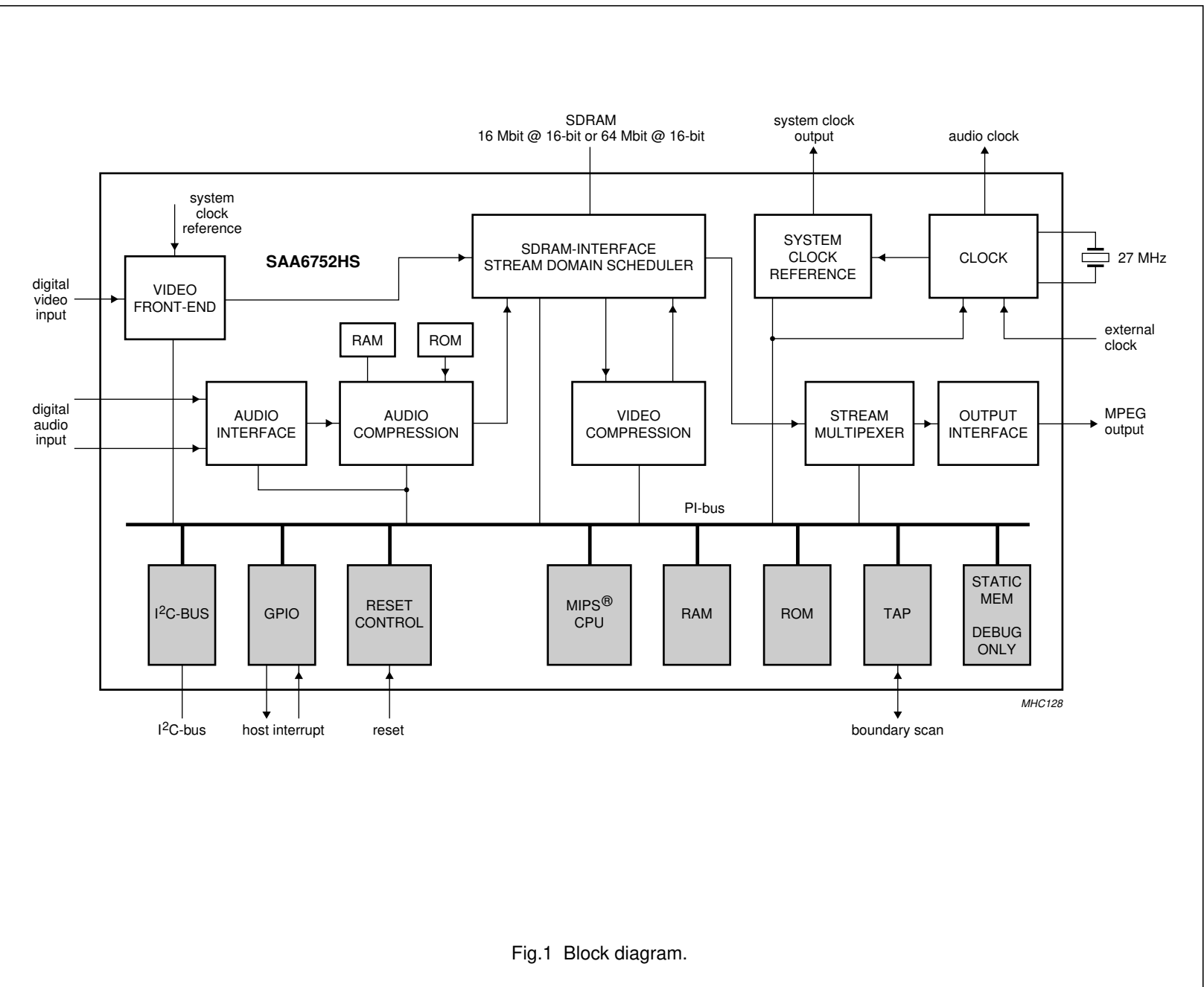


Fig.1 Block diagram.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

6 PINNING

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSP}	1	ground	–	pad ground
SDATA1	2	input	–	I ² S-bus serial data input port 1 with internal pull-down resistor
SCLK1	3	input/output	4	I ² S-bus serial clock port 1 with internal pull-down resistor
SWS1	4	input/output	4	I ² S-bus word select port 1 with internal pull-down resistor
V _{DDP}	5	supply	–	pad ring supply voltage (3.3 V)
SDATA2	6	input/output	4	I ² S-bus serial data port 2 with internal pull-down resistor
SCLK2	7	input/output	4	I ² S-bus serial clock port 2 with internal pull-down resistor
SWS2	8	input/output	4	I ² S-bus word select port 2 with internal pull-down resistor
ACLK	9	output	4	audio clock output (256f _s or 384f _s)
V _{SSP}	10	ground	–	pad ground
IDQ	11	input	–	reserved input with internal pull-down resistor; (recommended to connect to pin V _{SSP})
YUV0	12	input	–	video input signal bit 0 (LSB)
YUV1	13	input	–	video input signal bit 1
YUV2	14	input	–	video input signal bit 2
YUV3	15	input	–	video input signal bit 3
YUV4	16	input	–	video input signal bit 4
YUV5	17	input	–	video input signal bit 5
YUV6	18	input	–	video input signal bit 6
YUV7	19	input	–	video input signal bit 7 (MSB)
V _{SSP}	20	ground	–	pad ground
HSYNC	21	input	–	horizontal sync input (video) with internal pull-down resistor
VSYNC	22	input	–	vertical sync input (video) with internal pull-down resistor
FID	23	input	–	video field identification input (odd/even field) with internal pull-down resistor
VCLK1	24	input	–	video clock input 1 (27 MHz) with internal pull-down resistor
V _{SSCO}	25	ground	–	core ground
V _{SSCO}	26	ground	–	core ground
V _{DDCO}	27	supply	–	core supply voltage (2.5 V)
V _{DDCO}	28	supply	–	core supply voltage (2.5 V)
V _{DDP}	29	supply	–	pad ring supply voltage (3.3 V)
VCLK2	30	input	–	video clock input 2 (27 MHz) with internal pull-down resistor
PDOAV	31	3-state output	4	parallel stream data output for audio/video identifier
PDIDS	32	input	–	parallel stream data input for data strobe [request for packet in Data Expansion Bus Interface (DEBI) slave mode] with internal pull-up resistor
PDOSYNC	33	3-state output	4	parallel stream data output for packet sync
V _{SSP}	34	ground	–	pad ground
PDOVAL	35	3-state output	4	parallel stream data valid output with internal pull-up resistor
PDO0	36	3-state output	4	parallel stream data output bit 0 (LSB)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
PDO1	37	3-state output	4	parallel stream data output bit 1
PDO2	38	3-state output	4	parallel stream data output bit 2
V _{DDP}	39	supply	–	pad ring supply voltage (3.3 V)
PDO3	40	3-state output	4	parallel stream data output bit 3
PDO4	41	3-state output	4	parallel stream data output bit 4
PDO5	42	3-state output	4	parallel stream data output bit 5
PDO6	43	3-state output	4	parallel stream data output bit 6
V _{SSP}	44	ground	–	pad ground
PDO7	45	3-state output	4	parallel stream data output bit 7 (MSB)
PDIOCLK	46	input/output	4	parallel stream clock input/output
I2CADDRSEL	47	input	–	I ² C-bus address select input with internal pull-up resistor
SD_DQ15	48	input/output	8	SDRAM data input/output bit 15 (MSB)
V _{DDP}	49	supply	–	pad ring supply voltage (3.3 V)
SD_DQ0	50	input/output	8	SDRAM data input/output bit 0 (LSB)
SD_DQ14	51	input/output	8	SDRAM data input/output bit 14
SD_DQ1	52	input/output	8	SDRAM data input/output bit 1
V _{SSP}	53	ground	–	pad ground
SD_DQ13	54	input/output	8	SDRAM data input/output bit 13
SD_DQ2	55	input/output	8	SDRAM data input/output bit 2
SD_DQ12	56	input/output	8	SDRAM data input/output bit 12
V _{DDP}	57	supply	–	pad ring supply voltage (3.3 V)
SD_DQ3	58	input/output	8	SDRAM data input/output bit 3
SD_DQ11	59	input/output	8	SDRAM data input/output bit 11
SD_DQ4	60	input/output	8	SDRAM data input/output bit 4
SD_DQ10	61	input/output	8	SDRAM data input/output bit 10
V _{SSP}	62	ground	–	pad ground
SD_DQ5	63	input/output	8	SDRAM data input/output bit 5
SD_DQ9	64	input/output	8	SDRAM data input/output bit 9
SD_DQ6	65	input/output	8	SDRAM data input/output bit 6
SD_DQ8	66	input/output	8	SDRAM data input/output bit 8
V _{DDP}	67	supply	–	pad ring supply voltage (3.3 V)
SD_DQ7	68	input/output	8	SDRAM data input/output bit 7
SD_DQM1	69	output	8	SDRAM data mask enable output bit 1
SD_DQM0	70	output	8	SDRAM data mask enable output bit 0 (LSB)
SD _{WE}	71	output	8	SDRAM write enable output (active LOW)
V _{SSP}	72	ground	–	pad ground
SD _{CAS}	73	output	8	SDRAM column address strobe output (active LOW)
SD _{CLK}	74	output	8	SDRAM clock output
SD _{RAS}	75	output	8	SDRAM row address strobe output (active LOW)
SD _{CKE}	76	output	8	SDRAM clock enable output

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSCO}	77	ground	–	core ground
V _{SSCO}	78	ground	–	core and substrate ground
V _{DDCO}	79	supply	–	core supply voltage (2.5 V)
V _{DDCO}	80	supply	–	core supply voltage (2.5 V)
V _{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
SD_CS	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V _{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V _{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V _{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V _{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V _{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V _{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V _{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
SD_DQ21	117	input/output	8	reserved (do not connect)
SD_DQ25	118	input/output	8	reserved (do not connect)
V _{DDP}	119	supply	–	pad ring supply voltage (3.3 V)
SD_DQ22	120	input/output	8	reserved (do not connect)
SD_DQ24	121	input/output	8	reserved (do not connect)
SD_DQ23	122	input/output	8	reserved (do not connect)
EXTCLK	123	input	–	27 MHz external clock input with internal pull-up resistor
V _{SSP}	124	ground	–	pad ground
V _{SSA}	125	ground	–	oscillator analog ground
XTALI	126	analog input	–	crystal oscillator input (27 MHz); note 2
XTALO	127	analog output	–	crystal oscillator output (27 MHz)
V _{DDA}	128	supply	–	oscillator analog supply voltage (2.5 V)
V _{SSCO}	129	ground	–	core ground
V _{SSCO}	130	ground	–	core ground
V _{DDCO}	131	supply	–	core supply voltage (2.5 V)
V _{DDCO}	132	supply	–	core supply voltage (2.5 V)
V _{DDP}	133	supply	–	pad ring supply voltage (3.3 V)
TDI	134	input	–	boundary scan test data input; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TMS	135	input	–	boundary scan test mode select; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TCK	136	input	–	boundary scan test clock; pin must be set to LOW during normal operating; with internal pull-up resistor; note 3
TDO	137	3-state output	4	boundary scan test data output; pin not active during normal operating; with 3-state output; note 3
V _{SSP}	138	ground	–	pad ground
TRST	139	input	–	test reset input (active LOW), for boundary scan test (with internal pull-up resistor); notes 3 and 4
CLKOUT	140	output	4	27 MHz system clock output
TEST0	141	input/output	4	reserved (do not connect)
TEST1	142	input/output	4	reserved (do not connect)
V _{DDP}	143	supply	–	pad ring supply voltage (3.3 V)
TEST2	144	input/output	4	reserved (do not connect)
SDA	145	input/open-drain output	–	I ² C-bus serial data input/output
SCL	146	input/open-drain output	–	I ² C-bus serial clock input/output
RESET	147	input	–	reset input (active LOW); with internal pull-up resistor
V _{SSP}	148	ground	–	pad ground
RTS	149	output	4	reserved (do not connect); Universal Asynchronous Receiver/Transmitter (UART) request to send output (active LOW)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
CTS	150	input	–	reserved (recommended connect to pin V _{DDP}); UART clear to send input; external static memory select input (active LOW); with internal pull-up resistor
RXD	151	input	–	reserved (recommended connect to pin V _{DDP}); UART receive data; internal boot select input; with internal pull-up resistor
TXD	152	output	4	reserved (do not connect); UART transmit data
V _{DDP}	153	supply	–	pad ring supply voltage (3.3 V)
SM_LB	154	input/output	4	reserved (do not connect)
SM_UB	155	input/output	4	reserved (do not connect)
H_IRF	156	3-state output	4	host interrupt flag output; with internal pull-up resistor (active LOW)
V _{SSP}	157	ground	–	pad ground
SM_OE	158	output	4	reserved (do not connect); static memory output enable output (active LOW)
SM_A9	159	output	4	reserved (do not connect); static memory address output bit 9
SM_A10	160	output	4	reserved (do not connect); static memory address output bit 10
V _{DDP}	161	supply	–	pad ring supply voltage (3.3 V)
SM_A8	162	output	4	reserved (do not connect); static memory address output bit 8
SM_A11	163	output	4	reserved (do not connect); static memory address output bit 11
SM_A7	164	output	4	reserved (do not connect); static memory address output bit 7
SM_A12	165	output	4	reserved (do not connect); static memory address output bit 12
V _{SSP}	166	ground	–	pad ground
SM_A6	167	output	4	reserved (do not connect); static memory address output bit 6
SM_A13	168	output	4	reserved (do not connect); static memory address output bit 13
SM_A5	169	output	4	reserved (do not connect); static memory address output bit 5
SM_A14	170	output	4	reserved (do not connect); static memory address output bit 14
V _{DDP}	171	supply	–	pad ring supply voltage (3.3 V)
SM_WE	172	output	4	reserved (do not connect); static memory write enable output (active LOW)
SM_D7	173	input/output	4	reserved (do not connect); static memory data input/output bit 7 with internal pull-down resistor
SM_D8	174	input/output	4	reserved (do not connect); static memory data input/output bit 8 with internal pull-down resistor
SM_D6	175	input/output	4	reserved (do not connect); static memory data input/output bit 6 with internal pull-down resistor
V _{SSP}	176	ground	–	pad ground
SM_D9	177	input/output	4	reserved (do not connect); static memory data input/output bit 9 with internal pull-down resistor
SM_D5	178	input/output	4	reserved (do not connect); static memory data input/output bit 5 with internal pull-down resistor
SM_D10	179	input/output	4	reserved (do not connect); static memory data input/output bit 10 with internal pull-down resistor

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
SM_D4	180	input/output	4	reserved (do not connect); static memory data input/output bit 4 with internal pull-down resistor
V _{SSCO}	181	ground	–	internal pre-driver and substrate ground
V _{SSCO}	182	ground	–	core ground
V _{DDCO}	183	supply	–	core supply voltage (2.5 V)
V _{DDCO}	184	supply	–	internal pre-driver supply voltage (2.5 V)
V _{DDP}	185	supply	–	pad ring supply voltage (3.3 V)
SM_D11	186	input/output	4	reserved (do not connect); static memory data input/output bit 11 with internal pull-down resistor
SM_D3	187	input/output	4	reserved (do not connect); static memory data input/output bit 3 with internal pull-down resistor
SM_D12	188	input/output	4	reserved (do not connect); static memory data input/output bit 12 with internal pull-down resistor
SM_D2	189	input/output	4	reserved (do not connect); static memory data input/output bit 2 with internal pull-down resistor
V _{SSP}	190	ground	–	pad ground
SM_D13	191	input/output	4	reserved (do not connect); static memory data input/output bit 13 with internal pull-down resistor
SM_D1	192	input/output	4	reserved (do not connect); static memory data input/output bit 1 with internal pull-down resistor
SM_D14	193	input/output	4	reserved (do not connect); static memory data input/output bit 14 with internal pull-down resistor
SM_D0	194	input/output	4	reserved (do not connect); static memory data input/output bit 0 (LSB) with internal pull-down resistor
V _{DDP}	195	supply	–	pad ring supply voltage (3.3 V)
SM_D15	196	input/output	4	reserved (do not connect); static memory data input/output bit 15 (MSB) with internal pull-down resistor
SM_CS3	197	output	4	reserved (do not connect); static memory chip select output for external ROM or RAM (active LOW)
SM_A4	198	output	4	reserved (do not connect); static memory address output bit 4
SM_A3	199	output	4	reserved (do not connect); static memory address output bit 3
V _{SSP}	200	ground	–	pad ground
SM_A2	201	output	4	reserved (do not connect); static memory address output bit 2
SM_A15	202	output	4	reserved (do not connect); static memory address output bit 15
SM_A1	203	output	4	reserved (do not connect); static memory address output bit 1
SM_A16	204	output	4	reserved (do not connect); static memory address output bit 16
V _{DDP}	205	supply	–	pad ring supply voltage (3.3 V)
SM_A0	206	output	4	reserved (do not connect); static memory address output bit 0 (LSB)
SM_A17	207	output	4	reserved (do not connect); static memory address output bit 17 (MSB)
SM_CS0	208	output	4	reserved (do not connect)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

Notes

1. All input pins, input/output pins (in input mode), output pins (in 3-state mode) and open-drain output pins are limited to 3.3 V.
2. If used with external clock source the input voltage has to be limited to 2.5 V.
3. In accordance with the "IEEE 1149.1" standard.
4. Special function of pin $\overline{\text{TRST}}$:
 - a) For board designs without boundary scan implementation, pin $\overline{\text{TRST}}$ must be connected to ground.
 - b) Pin $\overline{\text{TRST}}$ provides easy initialization of the internal BST circuit. By applying a LOW level it can be used to force the internal Test Access Port (TAP) controller to the Test-Logic-Reset state (normal operating) immediately.

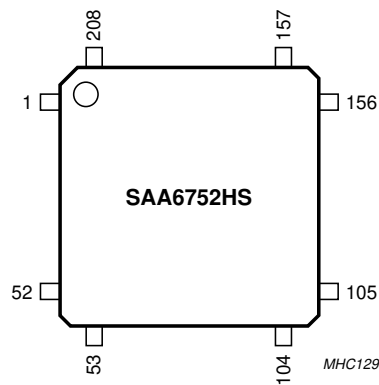


Fig.2 Pin configuration.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7 FUNCTIONAL DESCRIPTION

7.1 System operation

7.1.1 GENERAL

The SAA6752HS has a multi-processor architecture. The different processing and control modules are not locked to each other but run independently within the limits of the global scheduling. The data transfer between the processing units is carried out via FIFO memories or the external SDRAM. The device is configured and the operation modes are selected via the I²C-bus.

7.1.2 OPERATING MODES

There are five operating modes:

1. **Idle.** This mode is set after applying a hard reset (i.e. on power-up). In this mode the SAA6752HS can be initialized by the host to the required configuration. Video and audio processing is disabled. A hard reset always resets the SAA6752HS configuration parameters back to the default states.
2. **Stop.** In Stop mode, the video and audio input processing is enabled but the multiplexer output remains disabled. It is possible to read status information on the input video and audio signals via the I²C-bus. The SAA6752HS initialization settings cannot be modified, except to some specific dynamic encoding parameters (i.e. bit rate setting).
3. **Encode.** In this mode, the multiplexer output is enabled. Like Stop mode, only dynamic encoding parameters can be modified in this mode.
4. **Paused.** This mode allows the SAA6752HS to make seamless transitions. Restarting from Paused mode will generate a stream output with sequential time stamps and MPEG buffer model content.
5. **Power-down.** In this mode, the internal clock is disabled, sending the SAA6752HS into a (non-functional) power saving state. A hard reset will re-initialize the SAA6752HS.

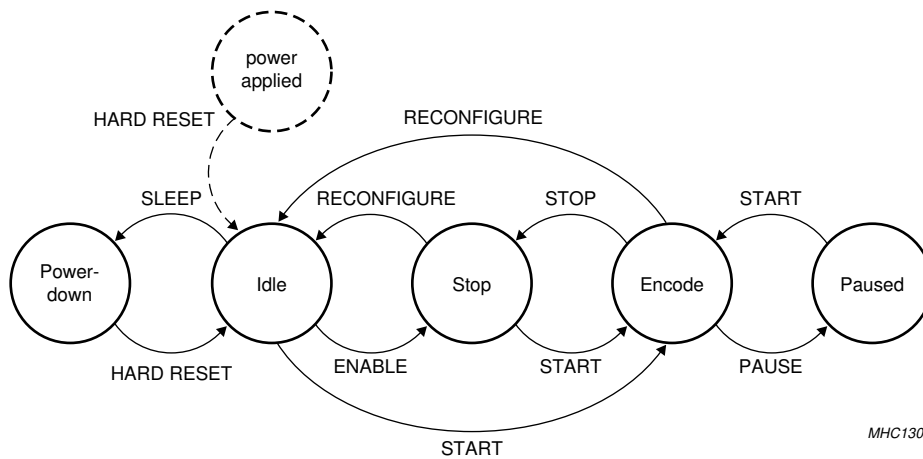


Fig.3 Mode transition diagram.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.1.3 MODE TRANSITION COMMANDS

There are seven mode transition commands:

1. **SOFT RESET.** Like a hard reset, a soft reset can be applied in any mode, setting the SAA6752HS back to Idle mode and resetting all configuration parameters back to the default settings.
2. **RECONFIGURE.** This command sets the SAA6752HS back to Idle mode without resetting the configuration parameters back to the default settings.
3. **ENABLE.** This transition sets Stop mode, enabling the video and audio input processing.
4. **START.** This transition sets Encode mode, enabling the multiplexer stream output. Note that if the SAA6752HS is commanded to start from the Idle mode, then the internal transition is via the Stop mode.
5. **STOP.** This command will disable the multiplexer stream output, setting the SAA6752HS to Stop mode. The current GOP and/or audio frame is completed and an end of sequence bit appended to the stream.
6. **PAUSE.** A PAUSE transition will cause the multiplexer to complete the current GOP and/or audio frame but no end of sequence bit is appended. The current MPEG buffer model contents are saved to provide a seamless transition on START.
7. **SLEEP.** This mode disables the internal clock.
8. **FORCED RECONFIGURE.** A STOP command whilst in the Encode mode will not work in case the video or audio input signal is interrupted, because for stopping, the SAA6752HS tries to finish the current GOP. The forced reconfigure command allows a mode transition back to the Idle state, without losing the actual configuration settings. The forced reconfiguration performs a soft reset and the automatic internal reprogramming of the I²C-bus registers. The forced reconfiguration will take about 200 ms; during the forced reconfiguration all register values will change to their default values before they are reprogrammed. Please note that outputs, which can be switched to high-impedance or to input mode, will not be active during the forced reconfiguration.

The SAA6752HS is not able to process any other commands during mode transitions. In this event, a get running mode request will return a busy flag. The completion of a mode transition can also be flagged as an event using the host interrupt pin.

7.2 Digital video input

7.2.1 GENERAL

The video front-end processes an "ITU-R BT.601/605" compliant video stream for conversion to 4 : 2 : 0 format (MP@ML). It includes synchronization, digital video signal processing through several filters, subsampling, sliced/raw VBI data handling, and SDRAM address generation.

The video interface is designed for use with Philips SAA7114 digital multi-standard decoder or similar video decoders. The input interface accepts a digital video input stream according to "ITU-R-BT.601". 625 lines standard at 50 Hz and 720 pixels by 576 lines as well as 525 lines at 60 Hz and 720 pixels by 480 lines are covered. The video synchronization may either follow "ITU-R-BT.656" recommendation or can also be supplied by external signals (HSYNC, VSYNC and FID). The formatter module performs a colour conversion from 4 : 2 : 2 to 4 : 2 : 0 format. Optionally, also SIF progressive downscaling and 2/3D1, 1/2D1 downscaling may be activated.

The SAA6752HS supports non-standard features of the SAA711x series of video input processors, such as hard-wired external synchronization signals (2 and 3-wire sync), special VCR playback signal streams (IEC 756 subset for VCR playback and still pictures), extraction of sliced data from the input video stream.

7.2.2 VIDEO FRONT-END CONFIGURATION OPTIONS

The following configuration options can be selected from the host:

- VIDEO INPUT PORT SELECTION. Two input clock pins are selectable.
- VIDEO INPUT FORMAT. 525 or 625-line formats can be selected.
- VIDEO SYNC FORMAT. Various combinations and polarities of HSYNC, VSYNC and Field Information (FID) can be selected as the source of sync signal processing.
- VIDEO FILTER SETTINGS. Noise pre-filter and horizontal filters can be enabled and, if the default coefficients are not suitable for an application, new coefficients can be set.
- VIDEO FORMAT CONVERSION. Selection of conversion from D1 to 1/2D1, 2/3D1 or SIF progressive downscaling.
- VBI DATA EXTRACTION. VBI data extraction of WSS or CC data can be enabled.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.2.3 VIDEO ENCODER STATUS INFORMATION

The following configuration option can be selected from the host:

- VBI DATA: WSS and CC data can be read back via the I²C-bus.

7.2.4 DATA INPUT FORMAT

7.2.4.1 Interface definition

The data input interface uses 13 pins, all of which are inputs (see Table 1). Pins YUV0 to YUV7 carry video and synchronization data and 3 pins are reserved for control purposes. Two separate clock inputs allow two different signal sources to be used. The input clock can be asynchronous to the SAA6752HS system clock.

Table 1 List of pins data input port

PIN	DESCRIPTION
YUV0 to YUV7	video input signal (synchronous to VCLK)
FID	odd/even field identification signal; note 1
HSYNC	horizontal synchronization signal; note 1
VSYNC	vertical synchronization signal; note 1
VCLK1 or VCLK2	video clock signal (from source 1 or 2)

Note

1. In ITU-T 656 mode sync signals are embedded in the video data input stream. The external sync signals are not used.

7.2.5 VIDEO SIGNAL PROCESSING

7.2.5.1 Acquisition of video data

Data is latched with the incoming video clock to provide robust data capture. Video clock and data is unlocked to the internal system clock therefore a clock domain bridge is used. This is performed by oversampling of video clock and data with 108 MHz.

7.2.5.2 Sync decoding and filtering

To allow selection of the right portion of the video input stream, synchronization signals from the stream are

recognized by a sync decoder. This checks the incoming field (FID), vertical sync and horizontal sync. It is possible to select either 'internal synchronization' (which means that SAV/EAV codes in the ITU 601/656 video streams are used) or externally applied hardware synchronization signals (which are given by the video input processor). In the latter case, 3 pin or 2 pin (V-sync and H-sync only) synchronization can be used.

Using 2 pin synchronization, the FID information is given by the timing of the transition of the V-sync. If a Vertical Blanking Interval (VBI) starts during H-sync, the next field will be the top field, otherwise it will be the bottom field.

A sync filter is used to inhibit sync signal triggering if an incorrect number of pixels or lines has been input. It also checks for the correct consecutive fields. The filter works on three different levels. An H-sync is only accepted after a predefined number of video cycles, a V-sync is only accepted after a programmed number of lines and a field is only accepted if top field follows bottom field or vice versa.

7.2.5.3 Horizontal and vertical shift

This function is intended for correction in synchronization of external sync signals if incorrectly timed. The amount of shift is programmable via the I²C-bus.

7.2.5.4 SAV/EAV decoder

A SAV/EAV decoder extracts the F, V and H bits from the video timing reference code. The decoder evaluates the protection bits to be able to correct one bit errors within the code word. If multiple bit errors are detected, the protection bits are ignored and the field (F), vertical sync (V) and horizontal sync (H) bits are directly extracted from the code.

7.2.5.5 Video format conversion

The SAA6752HS converts the input video input signal to the formats defined in Table 2 controlled by the I²C-bus command. A 4 : 2 : 2 to 4 : 2 : 0 colour conversion is performed as this is a pre-requisite of MPEG MP@ML encoding.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

Table 2 Format conversion

MODE	PICTURE FORMAT (PIXEL/LINES)
D1	720
2/3D1	480
1/2D1	352; note 1
SIF	352; notes 1 and 2

Notes

1. The 8 pixels at the right edge of the scaled picture are not encoded.
2. Top field only.

7.2.6 VIDEO FILTERING

7.2.6.1 Adaptive mean filter

The SAA6752HS uses an adaptive mean filter. There are three different filter modes that can be selected: median, averaging or no filter.

The median algorithm provides better noise performance and is well suited to suppress single noise spikes without degrading the signal edges. The averaging algorithm is a standard low-pass filter so has greater impact on signal edges.

The default threshold and gain coefficients of this filter can be overwritten via the I²C-bus to allow user optimization for different applications.

7.2.6.2 Horizontal pre-filter/decimation filter

There is a horizontal filter for Y and C and this can operate as a pre-filter or decimation filter. It is a symmetrical FIR filter with up to 8 coefficients programmable via the I²C-bus.

7.2.6.3 Vertical chrominance filtering

For 4 : 2 : 2 to 4 : 2 : 0 conversion, vertical filtering and subsampling of the chrominance is performed. The sequence of coefficients is mirrored in top and bottom field. This generates the right phases of the chrominance samples between the luminance samples (a non co-sited sampling scheme).

7.2.7 VBI DATA EXTRACTION

The SAA6752HS supports the extraction of WSS and CC data using two independent VBI data extractor modules. The data is available via the I²C-bus.

The following VBI data formats are supported: Closed Caption (CC525 and CC625) and Wide Screen Signalling (WSS525 and WSS625). For CC525, CC625 and WSS625 the sliced data from a video input processor (e.g. SAA7114, SAA7115 or SAA7118) are extracted from the digital video input signal and can be read via the I²C-bus. For WSS525 an internal data slicer is available which slices the oversampled raw data, which are delivered by the video input processor. The extracted WSS525 signal can be read via the I²C-bus.

Optionally the automatic insertion of extracted Closed Caption data into the user data area of a video stream is possible (for details see Section 7.3.8).

7.3 Video compression

7.3.1 GENERAL

Compression of video data is performed by the video compressor block; see Fig.4. The input to this block is the uncompressed video information pre-processed by the video front-end and stored in external SDRAM memory. The output is a compressed video stream, compliant to MPEG-2 Video Elementary Stream (VES) up to slice level. Controlling information (for example, quantizer step size) as well as the bit stream for higher layers of the VES is generated by the embedded MIPS[®] processor of the SAA6752HS.

The video compressor contains several subblocks. The MacroBlock Processor (MBP) performs generation of video ES on macroblock level. Controlling parameters for this task and MB headers as well as slice headers are generated by the core control subblock. Bitstream formatting and concatenation of MBP bitstream and header information is done by the subblocks pre-packer and packer.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.3.2 VIDEO ENCODER CONFIGURATION OPTIONS

The following configuration options can be selected from the host:

- VIDEO COMPRESSION SETTINGS. I, IP and IPB encoding with various GOP structures can be selected.
- ENCODER BIT RATE. The bit rate for variable bit rate or constant bit rate modes can be programmed using bit rate and quantization control parameters. These parameters can be adjusted whilst encoding, not just set at initialization.
- ENCODER PERFORMANCE TUNING. The ability for the user to tune encoding performance is provided by allowing control of adaptive quantization depth. Also the SAA6752HS allows download of new quantizer matrix contents.

7.3.3 VIDEO ENCODER STATUS INFORMATION

The following status information is available to the host:

- CURRENT ENCODER BIT RATE. The actual encoded bit rate, as number of bytes per GOP, is available allowing the use of constrained variable bit rate algorithms to fine tune the encoding efficiency.

7.3.4 GOP STRUCTURE

The programmable GOP structure features a reference frame distance (M) up to 3, and a GOP length (N) of up to 19. Supported structures are real closed GOP(M,N) and backward predicted closed GOP(M,N). For the use of B-frames in D1 and 2/3D1 mode a 64 Mbit SDRAM is needed.

In D1 mode, B-frames will be unidirectional. Backward predicted closed GOPs may have the first one (M = 2) or two (M = 3) B-frames referenced inside the GOP dependent on the I²C-bus register settings. This is intended for editable applications as GOPs are independent of each other. Non-editable GOPs allow the first one (M = 1) or two (M = 2) B-frames to be referenced to the P-frame in the previous GOP. This is a non-editable format but has optimum encoding efficiency. This structure is sometimes called an open GOP. The first one (M = 1) or two (M = 2) B-frames in the first GOP of a sequence are always forced backwards predicted.

Table 3 GOP

GOP LENGTH (N)	REFERENCE FRAME DISTANCE (M)			
	0	1	2	3
1	I	(1)	(1)	(1)
2	(1)	IP	(1)	(1)
3	(1)	IPP	IBP ⁽²⁾	(1)
4	(1)	IPPP	BIBP ⁽³⁾	IBBP ⁽²⁾
5	(1)	IPPPP	IBPB ⁽²⁾	(1)
6	(1)	IPP...PP	BIBBP ⁽³⁾	BBIBBP ⁽³⁾
7	(1)	IPP...PP	IBP...BP ⁽²⁾	IBBPBBP ⁽²⁾
8	(1)	IPP...PP	BIBP...BP ⁽³⁾	(1)
9	(1)	IPP...PP	IBP...BP ⁽²⁾	BBI...BBP ⁽³⁾
10	(1)	IPP...PP	BIBP...BP ⁽³⁾	IBBP...BBP ⁽²⁾
11	(1)	IPP...PP	IBP...BP ⁽²⁾	(1)
12	(1)	IPP...PP	BIBP...BP ⁽³⁾	BBI...BBP ⁽³⁾
13	(1)	IPP...PP	IBP...BP ⁽²⁾	IBBP...BBP ⁽²⁾
14	(1)	IPP...PP	BIBP...BP ⁽³⁾	(1)
15	(1)	IPP...PP	IBP...BP ⁽²⁾	BBI...BBP ⁽³⁾
16	(1)	IPP...PP	BIBP...BP ⁽³⁾	IBBP...BBP ⁽³⁾
17	(1)	IPP...PP	IBP...BP ⁽²⁾	(1)
18	(1)	IPP...PP	BIBP...BP ⁽³⁾	BBI...BBP ⁽³⁾
19	(1)	IPP...PP	IBP...BP ⁽²⁾	IBBP...BBP ⁽²⁾

Notes

1. Undefined.
2. This GOP structure is defined as a Real Closed GOP (RCG).
3. This GOP structure is defined as a Backward Predicted Closed GOP (BPCG) or Non-Editable GOP (NEG), selectable via the I²C-bus.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.3.5 BIT RATE CONTROL

The SAA6752HS supports two modes of video bit rate control: variable bit rate and constant bit rate.

The Variable Bit Rate (VBR) mode is intended for burst data transfer applications, where the bit rate is allowed to vary but the image quality should be constant. In this mode, a combination of three parameters can be set: Rvbr, Qmin_VBR and Qmax_VBR. While aiming at the target bit rate Rvbr, only quantizer scale values within the range between Qmin_VBR and Qmax_VBR are applied.

Broadening this range leads to greater variations in picture quality but better adherence to Rmax. Constriction of this range forces a better constancy in picture quality at the expense of meeting the target bit rate. Note that optimal control results require reasonable combinations of Rmax, Qmin_VBR and Qmax_VBR. Furthermore, the maximum bit rate Rmax can be set. If Rmax is reached in VBR mode, the CBR algorithm takes over the control by increasing the quantizer scale values temporarily (over Qmax_VBR) to guarantee that Rmax is never exceeded. Hence, the closer Rmax and Rvbr are chosen, the more the control in VBR mode turns to CBR mode behaviour.

The Constant Bit Rate (CBR) mode is intended for applications, where a fixed channel rate is provided (e.g. transmission systems). A tight control of the quantizer scale is applied to make optimal use of the given bandwidth. The parameter Rmax specifies the required constant bit rate.

Independent of the bit rate mode (CBR or VBR), a B-frame weighting factor (the weighting factor is applied to the quantization scale) can be applied to further reduce the bit rate of B-frames. In IP-only GOP structures, every second P-frame is weighted by this factor generating 'virtual B-frames' to simulate a bit rate distribution similar to IPB sequences. This feature can further improve the perceptual rate-distortion ratio by taking advantage of the inertia of the human visual system.

7.3.6 ADAPTIVE QUANTIZATION

Adaptive quantization is an algorithm that uses internal generated statistics to fine tune the quantizer scale used for encoding a specific macroblock. For example, the controller adapts the quantization scale with respect to the local complexity distribution within a frame, resulting in a perceptually smoother picture quality. The amount of fine tuning can be adjusted by control of the adaptive quantization depth.

7.3.7 QUANTIZER MATRIX TABLE DOWNLOAD

The MPEG standard default quantizer matrices can be overwritten to allow picture encoding optimization.

7.3.8 USER DATA INSERTION

User data insertion of up to 64 bytes is supported on GOP and picture level.

Different modes can be selected via I²C-bus.

7.3.8.1 External user data insertion (permanently repeated)

User data is downloaded via the I²C-bus to subaddresses 73H/76H and the number of inserted user data bytes is set via subaddresses 74H/75H. In Encode mode the downloaded user data will be inserted permanently into the user data area of the video stream.

It is possible to download a new set of user data during Encode mode. The new data will be repeatedly inserted as soon as the download is finished. It is possible to stop the user data insertion with a special command.

7.3.8.2 External user data insertion (each downloaded byte inserted only once)

In this mode each downloaded user data byte is inserted only once into the user data area. If no new user data is downloaded between two GOP or pictures then no user data will be inserted. This mode can be used to transmit more than 64 bytes of user data from the encoder to the decoder, e.g. 1 000 bytes distributed on 15 packets of 64 bytes and one packet of 40 bytes. The host has to control the insertion and repetition of user data. A host interrupt 'mode transition completed' is signalled, if not masked and the bit 9 of the exception status word is set when the user data have been read by the video encoder. Then new user data can be downloaded via I²C-bus.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.3.8.3 *Internal Closed Caption user data insertion compliant to ATSC/NTSC standard*

Automatic insertion of Closed Caption data into the user data 2 area on picture header level compliant to the ATSC and EIA-708 standard can be selected via the I²C-bus.

Closed Caption data, which is delivered from the video input processor (e.g. SAA7114) and captured in the video front-end will be inserted into the user data 2 area (picture header level) of the video stream. Preconditions are appropriate settings of the video input processor and the VBI data extractor in the video front-end. The Closed Caption user data will be written for both fields. If no valid Closed Caption data for field 2 is available these data will be marked as invalid in the stream. At SIF mode only field 1 Closed Captions can be inserted from the video input signal and dummy values (80H 80H) will be inserted for field 2.

If extended data services (XDS data, line 21 field 2) are inserted, the insertion will be transparent. No modification of the CGMS-A copy information will be done.

In accordance to EIA-708 the Closed Caption data will appear in the stream in transport order. If B-frames are present the user data is re-ordered in the same way as the video frames.

Advanced TV Closed Captioning (ATVCC) channel packet data (cc_type 10 or 11) is not supported, because the input signal of the encoder is an analog video signal, which can carry only NTSC Closed Captions, but not ATV Closed Captions.

No additional user data on picture header level can be inserted if internal Closed Caption user data insertion compliant to the ATSC/NTSC standard is active.

7.3.8.4 *Internal Closed Caption user data insertion compliant to DVD standard*

Automatic insertion of Closed Caption data into the user data area on GOP header level compliant to the DVD standard can be selected via I²C-bus.

Closed Caption data, which is delivered from the video input processor (e.g. SAA7114) and captured in the video front-end will be inserted into the user data 1 area (GOP header level) of the video stream. Preconditions are appropriate settings of the video input processor and the VBI data extractor in the video front-end. The Closed Caption user data will be written for both fields. If no valid Closed Caption data for field 2 is available these data will be marked as invalid in the stream.

If extended data services (XDS data, line 21 field 2) are inserted, the insertion will be transparent. No modification of the CGMS-A copy information will be done.

The Closed Caption data will be inserted for each field of the GOP in display order. At SIF mode only field 1 Closed Captions can be inserted from the video input signal and dummy values (80H 80H) will be inserted for field 2.

The user data is delayed by one GOP period. The first GOP in the stream carries dummy data marked as invalid.

No additional user data on GOP header level can be inserted if internal Closed Caption user data insertion compliant to the DVD standard is active.

The amount of user data depends on the GOP size: 5 bytes header and 3 bytes/field are required. With the maximum GOP size of 19 this results in $5 + 19 \times 2 \times 3 = 119$ bytes, which is more than the available array of 64 bytes for GOP user data. Therefore the 64 byte array for picture user data is also used for GOP user data, if GOP sizes larger than 9 are selected. Then all 128 bytes, which are available for user data insertion on GOP and picture header level will be used for the insertion of CC data on GOP level. In this case no additional user data insertion on picture header level is possible.

7.3.9 MOTION ADAPTIVE NOISE REDUCTION

The gain and adaptivity can be controlled to optimize encoding efficiency in case of noisy input sequences, i.e. off-air reception.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.3.10 COMPRESSION BLOCK PARTITIONING

The video compression block, shown in Fig.4, contains the following sub-modules:

- **MacroBlock Processor (MBP).** Reads uncompressed video data from SDRAM and generates the compressed bitstream on MB level (without MB headers). Addresses for frame buffer (previous frame) access are generated by the MBP.
- **Core control.** Performs MB and slice header generation, base address generation for the current MB (uncompressed), motion vector candidate generation, and computation of encoding statistics required by the CPU for bit rate controlling.

- **Pre-packer** (part of packing unit). Since the MBP output words are not necessarily fully used (i.e. some output words may contain unused bits) the pre-packer packs the output of the MBP in such a way that all words contain valid bits. This reduces the amount of memory required for storing the MB data.
- **Packer** (part of packing unit). Merges header and MB headers.

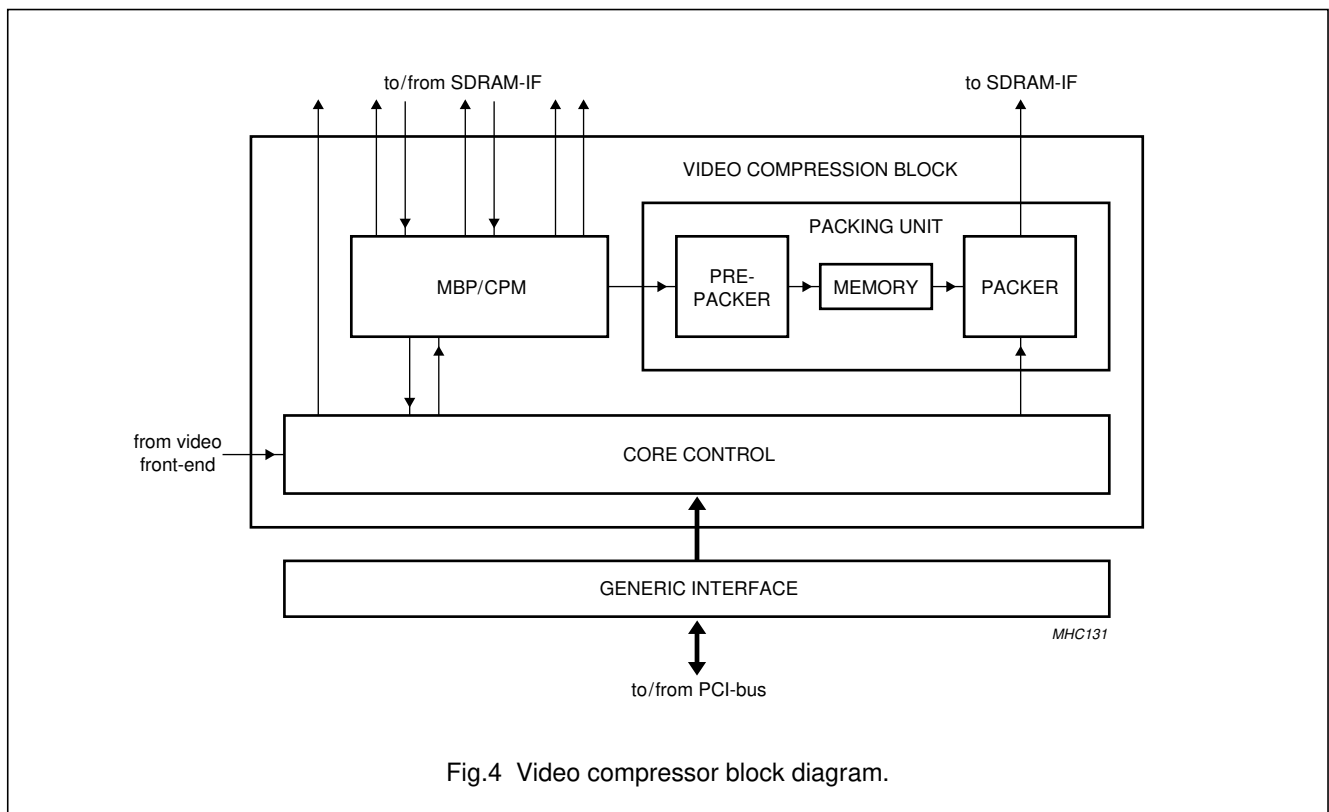


Fig.4 Video compressor block diagram.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.4 Digital audio input

7.4.1 GENERAL

The audio input interface (I²S) accepts serial digital audio data and supports master and slave mode. The interface is able to handle 16 to 20 bits audio data with left and right channel. Audio data with more than 20-bit word width is accepted as input, but the additional bits are ignored.

7.4.2 AUDIO PORT CONFIGURATION OPTIONS

The following configuration options can be selected from the host:

- **AUDIO INPUT PORT SELECTION.** Two digital audio input ports are selectable.
- **AUDIO INPUT FORMAT.** Various I²S and EIAJ formats can be selected.
- **AUDIO INPUT MODES.** Master or slave mode can be selected.
- **AUDIO CLOCK OUTPUT.** An audio clock output (256 × 48 kHz or 384 × 48 kHz) can be used for external analog-to-digital converter clocking.
- **AUDIO OUTPUT.** The second audio interface port can be configured as output in special applications e.g. concurrent encoding of audio and video without internal multiplexing of the two streams.

7.4.3 INPUT FORMATS

The digital audio input interface can select between two digital audio input ports via I²C-bus control and is able to input the following audio formats:

- I²S, see Fig.5
- EIAJ, see Fig.6
- EIAJ alternative format.

The alternative formats are defined as having the word select shifted by one clock cycle with respect to the data.

EIAJ and EIAJ alternative format are supported for 16, 18 and 20-bit resolution. I²S and I²S alternative format are supported for 16, 18, 20 and 24-bit resolution. Input data is truncated to 20 bits internally if 24-bit resolution is applied.

Each of the formats can be applied in master or slave mode.

When in master mode, the external audio analog-to-digital convertor must be clocked using the audio clock generated by the SAA6752HS. This can be set to 256 × 48 kHz or 384 × 48 kHz.

In slave mode an internal sample rate converter converts the input sample frequency to a video frame locked 48 kHz sample frequency.

If video is not present and/or the clock mode is set to mode 3, the audio clock frequency is locked to the fixed nominal system frequency (crystal or external). In all other cases the audio clock will be locked to the video frame frequency.

MPEG-2 video and MPEG-audio/AC-3
audio encoder with multiplexer

SAA6752HS

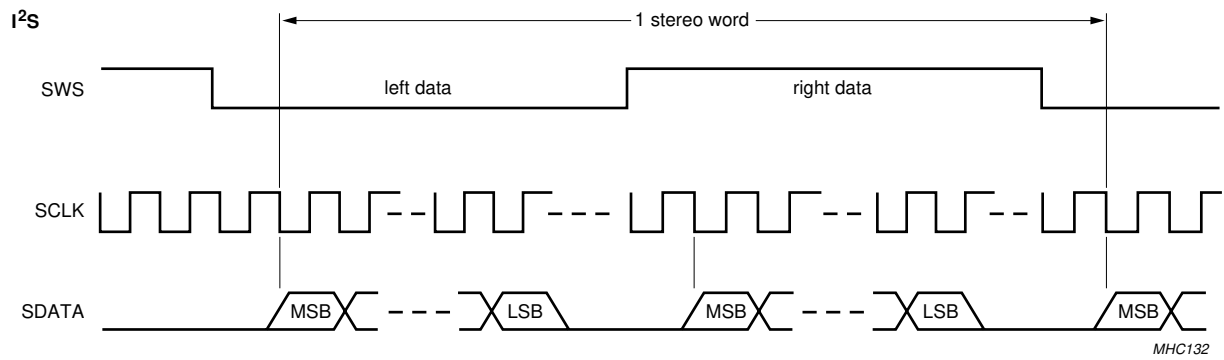


Fig.5 I²S mode format protocol.

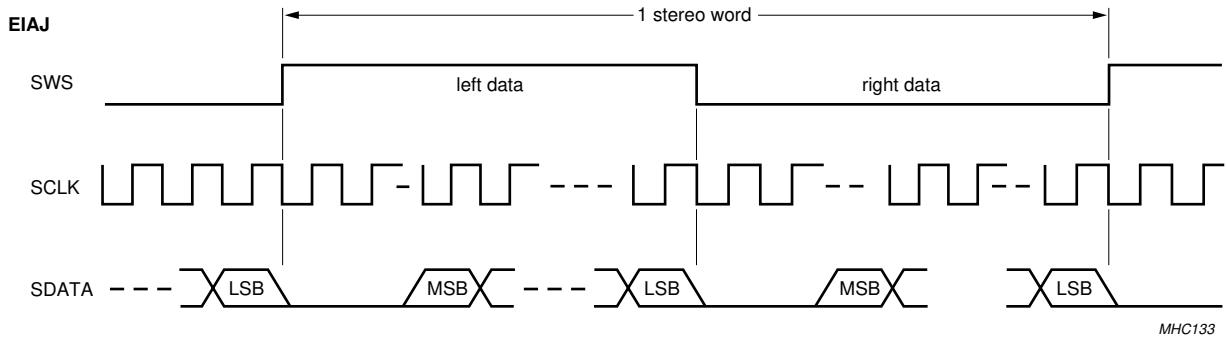


Fig.6 EIAJ mode format protocol.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

7.4.4 AUDIO INPUT PROCESSING

In order to be able to cope with analog and digital sources, the I²S input ports can be configured as master (analog) or slave (digital). For the slave mode however, a sample rate converter will be involved, except for DVD-compliant audio bypass. Table 4 reflects the different configuration possibilities.

Table 4 Audio input processing modes

PROCESSING MODE ⁽¹⁾	AUDIO CONTENT FORMAT	INPUT SAMPLE FREQUENCY (kHz)		NO. OF ENCODED BITS	ENCODED BIT RATE (kbit/s)
		MASTER ⁽²⁾	SLAVE ⁽³⁾⁽⁴⁾		
MPEG-1 L2 encoding	LPCM at 16, 18, 20 or 24 bits ⁽⁵⁾	48	32 kHz \pm 0.1% 44.1 kHz \pm 0.1% 48 kHz \pm 0.1%	20	256, 384
DDC encoding ⁽⁶⁾	LPCM at 16, 18, 20 or 24 bits ⁽⁵⁾	48	32 kHz \pm 0.1% 44.1 kHz \pm 0.1% 48 kHz \pm 0.1%	20	256, 384
LPCM bypass (uncompressed audio format) ⁽⁷⁾	LPCM at 16, 18, 20 or 24 bits ⁽⁵⁾	48	32 kHz \pm 0.1% 44.1 kHz \pm 0.1% 48 kHz \pm 0.1%	16	–
DVD-compliant audio bypass	16 bits ⁽⁸⁾	–	48 kHz ⁽⁹⁾	16	–

Notes

1. Processing modes can be changed when SAA6752HS is in Idle mode.
2. In master mode, the external audio source must use the SAA6752HS audio clock as a clock source.
3. A sample rate conversion process will convert incoming data to a nominal 48 kHz audio frequency that is locked to V-sync of the video input signal (if present). The sample rate converter is not enabled for DVD-compliant bypass mode.
4. The sample rate conversion input frequency range has been selected to be compatible with class 2 SPDIF receivers.
5. 24-bit input option only applies to I²S input formats, in this event it will be truncated to 20 bits internally in the SAA6752HS before processing. EIAJ formats are limited to 20 bits maximum.
6. Only for SAA6752HS/V103.
7. In systems that use 16 Mbit SDRAM due to system architecture constraints, LPCM bypass must be restricted to be used with I and IP video encoding only. There is no constraint if 64 Mbit SDRAM is used.
8. The IEC 60958 format defines 20 bits for an audio sample, plus 4 auxiliary bits, which can be used to extend the word length. IEC 61937 uses only 16 data bits of each IEC 60958 sub-frame. It depends on the settings of an external SPDIF to I²S converter if 16, 18, 20 or 24 bits are transferred to the SAA6752HS.
9. For DVD-compliant bypass mode the audio clock must be locked to the video clock externally.