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DATA SHEET

SAA7104E; SAA7105E
Digital video encoder

Product specification

2004 Mar 04

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- Supports Intel® Digital Video Out (DVO) low voltage interfacing to graphics controller
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 85 MHz at double edged clocking, synthesized on-chip or from external source
- Programmable assignment of clock edge to bytes (in double edged mode)
- Synthesizable pixel clock (PIXCLK) with minimized output jitter, can be used as reference clock for the VGC, as well)
- PIXCLK output and bi-phase PIXCLK input (VGC clock loop-through possible)
- Hot-plug detection through dedicated interrupt pin
- Supported VGA resolutions for PAL or NTSC legacy video output up to 1280 × 1024 graphics data at 60 or 50 Hz frame rate
- Supported VGA resolutions for HDTV output up to 1920 × 1080 interlaced graphics data at 60 or 50 Hz frame rate
- Three Digital-to-Analog Converters (DACs) for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) at 27 MHz sample rate (signals in parenthesis are optionally), all at 10-bit resolution
- Non-interlaced C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling
- Downscaling and upscaling from 50 to 400%
- Optional interlaced C_B-Y-C_R input of Digital Versatile Disk (DVD) signals
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode, maximum 85 MHz)
- 3 × 256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- HDTV up to 1920 × 1080 interlaced and 1280 × 720 progressive, including 3-level sync pulses
- Programmable border colour of underscan area
- Programmable 5 line anti-flicker filter
- On-chip 27 MHz crystal oscillator (3rd-harmonic or fundamental 27 MHz crystal)
- Fast I^2C-bus control port (400 kHz)
- Encoder can be master or slave
- Adjustable output levels for the DACs
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Optional support of various Vertical Blanking Interval (VBI) data insertion
- Macrovision™(1) Pay-per-View copy protection system rev. 7.01, rev. 6.1 and rev. 1.03 (525p) as option; this applies to the SAA7104E only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- Optional cross-colour reduction for PAL and NTSC CVBS outputs
- Power-save modes
- Joint Test Action Group (JTAG) boundary scan test
- Monolithic CMOS 3.3 V device, 5 V tolerant I/Os.

(1) Macrovision™ is a trademark of the Macrovision Corporation.

2 GENERAL DESCRIPTION

The SAA7104E; SAA7105E is an advanced next-generation video encoder which converts PC graphics data at maximum 1280 × 1024 resolution (optionally 1920 × 1080 interlaced) to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum 5 lines) ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 1280 × 1024 resolution/60 Hz (PIXCLK < 85 MHz). Alternatively this port can provide Y, P_B and P_R signals for HDTV monitors.

The device includes a sync/clock generator and on-chip DACs.

All inputs intended to interface to the host graphics controller are designed for low-voltage signals between down to 1.1 V and up to 3.6 V.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	3.15	3.3	3.45	V
V_{DDD}	digital supply voltage	3.15	3.3	3.45	V
I_{DDA}	analog supply current	1	110	115	mA
I_{DDD}	digital supply current	1	175	200	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog CVBS output signal voltage for a 100/100 colour bar at 75/2 Ω load (peak-to-peak value)	–	1.23	–	V
R_L	load resistance	–	37.5	–	Ω
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs	–	–	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs	–	–	±1	LSB
T_{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7104E	BGA156	plastic ball grid array package; 156 balls; body 15 × 15 × 1.15 mm	SOT472-1
SAA7105E			

5 BLOCK DIAGRAM

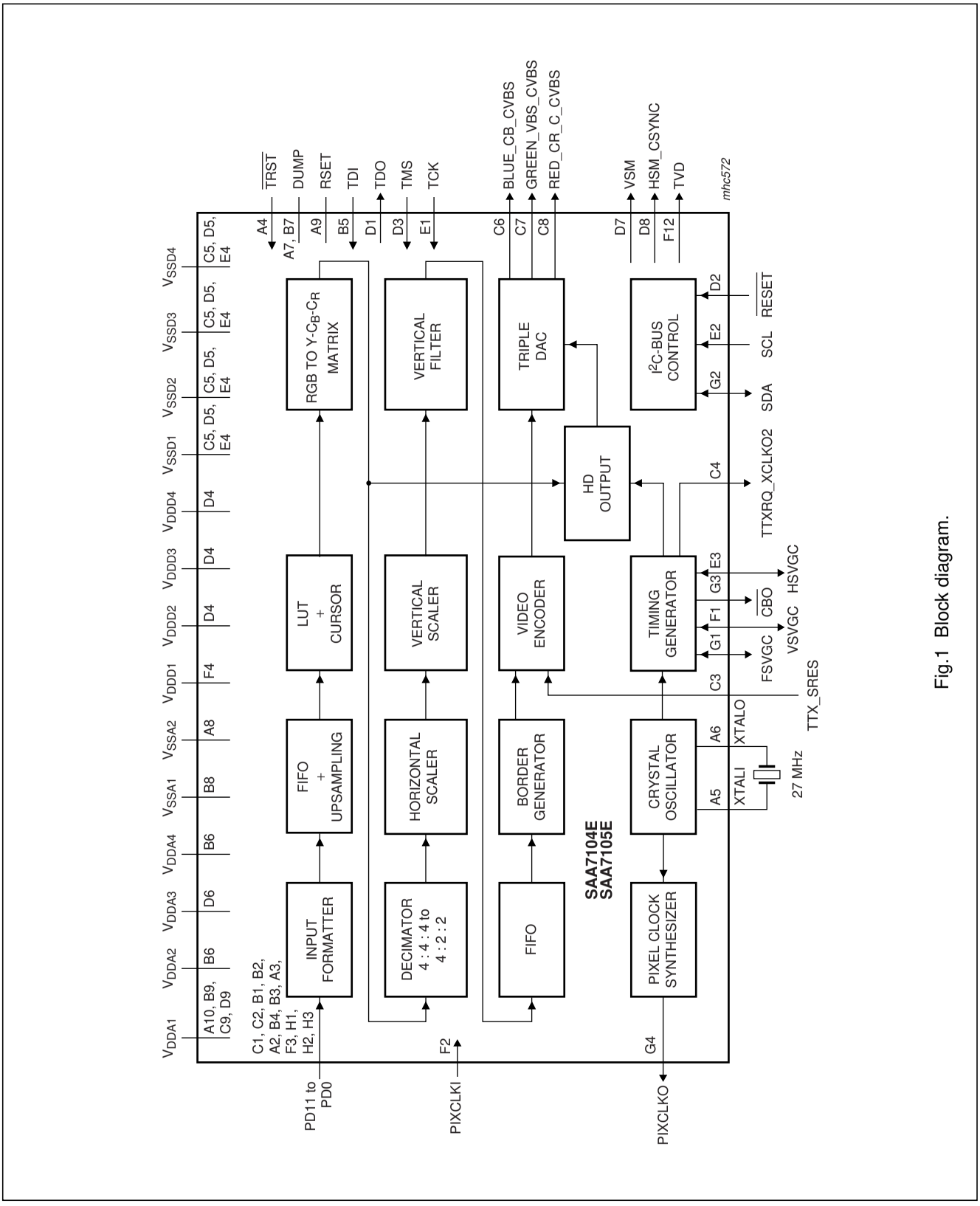

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
PD7	A2	I	MSB with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
PD4	A3	I	MSB – 3 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
$\overline{TRST}$	A4	I/pu	test reset input for BST; active LOW; notes 2, 3 and 4
XTALI	A5	I	crystal oscillator input
XTALO	A6	O	crystal oscillator output
DUMP	A7, B7	O	DAC reference pin; connected via 12 Ω resistor to analog ground
V_{SSA2}	A8	S	analog ground 2
RSET	A9	O	DAC reference pin; connected via 1 kΩ resistor to analog ground (do not use capacitor in parallel with 1 kΩ resistor)
V_{DDA1}	A10, B9, C9, D9	S	analog supply voltage 1 (3.3 V for DACs)
PD9	B1	I	see Tables 9 to 14 for pin assignment
PD8	B2	I	see Tables 9 to 14 for pin assignment
PD5	B3	I	MSB – 2 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
PD6	B4	I	MSB – 1 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
TDI	B5	I	test data input for BST; note 2
V_{DDA2}	B6	S	analog supply voltage 2 (3.3 V for DACs)
V_{DDA4}	B6	S	analog supply voltage 4 (3.3 V)
V_{SSA1}	B8	S	analog ground 1
PD11	C1	I	see Tables 9 to 14 for pin assignment
PD10	C2	I	see Tables 9 to 14 for pin assignment
TTX_SRES	C3	I	teletext input or sync reset input
TTXRQ_XCLKO2	C4	O	teletext request output or 13.5 MHz clock output of the crystal oscillator; note 5
V_{SSD1}	C5, D5, E4	S	digital ground 1
V_{SSD2}	C5, D5, E4	S	digital ground 2
V_{SSD3}	C5, D5, E4	S	digital ground 3
V_{SSD4}	C5, D5, E4	S	digital ground 4
BLUE_CB_CVBS	C6	O	analog output of BLUE or C_B or CVBS signal
GREEN_VBS_CVBS	C7	O	analog output of GREEN or VBS or CVBS signal
RED_CR_C_CVBS	C8	O	analog output of RED or C_R or C or CVBS signal
TDO	D1	O	test data output for BST; note 2
$\overline{RESET}$	D2	I	reset input; active LOW
TMS	D3	I/pu	test mode select input for Boundary Scan Test (BST); note 2
V_{DDD2}	D4	S	digital supply voltage 2 (3.3 V for I/Os)
V_{DDD3}	D4	S	digital supply voltage 3 (3.3 V for core)
V_{DDD4}	D4	S	digital supply voltage 4 (3.3 V for core)
V_{DDA3}	D6	S	analog supply voltage 3 (3.3 V for oscillator)

SYMBOL	PIN	TYPE(1)	DESCRIPTION
VSM	D7	O	vertical synchronization output to monitor (non-interlaced auxiliary RGB)
HSM_CSYNC	D8	O	horizontal synchronization output to monitor (non-interlaced auxiliary RGB) or composite sync for RGB-SCART
TCK	E1	I/pu	test clock input for BST; note 2
SCL	E2	I	I^2C-bus serial clock input
HSVGC	E3	I/O	horizontal synchronization output to VGC (optional input); note 5
reserved	E12	–	to be reserved for future applications
VSVGC	F1	I/O	vertical synchronization output to VGC (optional input); note 5
PIXCLKI	F2	I	pixel clock input (looped through)
PD3	F3	I	MSB – 4 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
V_{DDD1}	F4	S	digital supply voltage 1 for pins PD11 to PD0, PIXCLKI, PIXCLKO, FSVGC, VSVGC, HSVGC, $\overline{CBO}$ and TVD
TVD	F12	O	interrupt if TV is detected at DAC output
FSVGC	G1	I/O	frame synchronization output to Video Graphics Controller (VGC) (optional input); note 5
SDA	G2	I/O	I^2C-bus serial data input/output
$\overline{CBO}$	G3	I/O	composite blanking output to VGC; active LOW; note 5
PIXCLKO	G4	O	pixel clock output to VGC
PD2	H1	I	MSB – 5 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
PD1	H2	I	MSB – 6 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment
PD0	H3	I	MSB – 7 with C_B-Y-C_R 4 : 2 : 2; see Tables 9 to 14 for pin assignment

Notes

1. Pin type: I = input, O = output, S = supply, pu = pull-up.
2. In accordance with the *"IEEE1149.1"* standard the pins TDI, TMS, TCK and $\overline{TRST}$ are input pins with an internal pull-up resistor and TDO is a 3-state output pin.
3. For board design without boundary scan implementation connect $\overline{TRST}$ to ground.
4. This pin provides easy initialization of the Boundary Scan Test (BST) circuit. $\overline{TRST}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.
5. The pins FSVGC, VSVGC, $\overline{CBO}$, HSVGC and TTXRQ_XCLKO2 are used for bootstrapping; see Section 7.1.

Table 1 Pin assignment (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		PD7	PD4	$\overline{TRST}$	XTALI	XTALO	DUMP	V_{SSA2}	RSET	V_{DDA1}				
B	PD9	PD8	PD5	PD6	TDI	V_{DDA2} V_{DDA4}	DUMP	V_{SSA1}	V_{DDA1}					
C	PD11	PD10	TTX_ SRES	TTXRQ_ XCLKO2	V_{SSD1} V_{SSD2} V_{SSD3} V_{SSD4}	BLUE_ CB_ CVBS	GREEN_ VBS_ CVBS	RED_ CR_ C_ CVBS	V_{DDA1}					
D	TDO	$\overline{RESET}$	TMS	V_{DDD2} V_{DDD3} V_{DDD4}	V_{SSD1} V_{SSD2} V_{SSD3} V_{SSD4}	V_{DDA3}	VSM	HSM_ CSYNC	V_{DDA1}					
E	TCK	SCL	HSVGC	V_{SSD1} V_{SSD2} V_{SSD3} V_{SSD4}								reserved		
F	VSVGC	PIXCLKI	PD3	V_{DDD1}								TVD		
G	FSVGC	SDA	$\overline{CBO}$	PIXCLKO										
H	PD2	PD1	PD0											
J														
K														
L														
M														
N														
P														

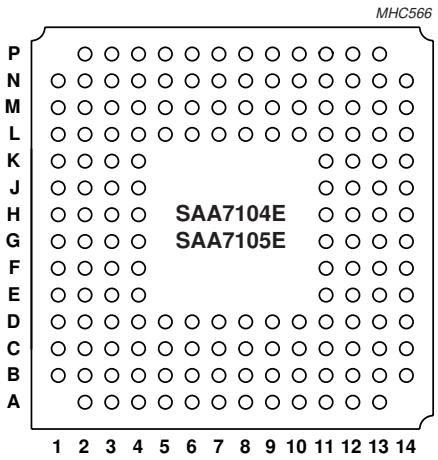

Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The digital video encoder encodes digital luminance and colour difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7104E; SAA7105E can be directly connected to a PC video graphics controller with a maximum resolution of 1280×1024 (progressive) or 1920×1080 (interlaced) at a 50 or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Tables 9 to 14.

A complete 3×256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port PD (Pixel Data) or via the I^2C-bus.

The SAA7104E; SAA7105E supports a $32 \times 32 \times 2$-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I^2C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7104E; SAA7105E can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/colour difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"ITU-R BT.470-3"*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figs 4 to 9. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *"ITU-R BT.656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in slave mode. For assignment of the input data to the rising or falling clock edge see Tables 9 to 14.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7104E; SAA7105E synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I²C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I²C-bus.

The IC also contains Closed Caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Fig.14). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

7.1 Reset conditions

To activate the reset a pulse at least of 2 crystal clocks duration is required.

During reset ($\overline{\text{RESET}}$ = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{\text{CBO}}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I²C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I²C-bus access redefines the corresponding registers; see Table 2.

Table 2 Strapping pins

PIN	TIED	PRESET
FSVGC	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{\text{CBO}}$	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal colour bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

7.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I²C-bus control bits SLOT and EDGE for correct operation.

If Y-C_B-C_R is being applied as a 27 Mbyte/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

The horizontal upscaling is supported via the input formatter. According to the programming of the pixel clock dividers (see Section 7.10), it will sample up the data stream to 1 ×, 2 × or 4 × the input data rate. An optional interpolation filter is available. The clock domain transition is handled by a 4 entries wide FIFO which gets initialized every field or explicitly at request. A bypass for the FIFO is available, especially for high input data rates.

7.3 RGB LUT

The three 256 byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed colour data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I^{2}C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 $\times$ 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

7.4 Cursor insertion

A 32 $\times$ 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I^{2}C-bus write access to specific registers or in the pixel data input through the PD port. In the latter case, the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I^{2}C-bus register as described in Table 5. Transparent means that the input pixels are passed through, the 'cursor colours' can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 3 Layout of a byte in the cursor bit map

D7	D6	D5	D4	D3	D2	D1	D0
pixel n + 3		pixel n + 2		pixel n + 1		pixel n	
D1	D0	D1	D0	D1	D0	D1	D0

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the 'hot spot', the other register controls the insertion position.

The hot spot is the 'tip' of the pointer arrow. It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 4 Cursor bit map

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
0	row 0 column 3		row 0 column 2		row 0 column 1		row 0 column 0	
1	row 0 column 7		row 0 column 6		row 0 column 5		row 0 column 4	
2	row 0 column 11		row 0 column 10		row 0 column 9		row 0 column 8	
...	...		...		...		...	
6	row 0 column 27		row 0 column 26		row 0 column 25		row 0 column 24	
7	row 0 column 31		row 0 column 30		row 0 column 29		row 0 column 28	
...	...		...		...		...	
254	row 31 column 27		row 31 column 26		row 31 column 25		row 31 column 24	
255	row 31 column 31		row 31 column 30		row 31 column 29		row 31 column 28	

Table 5 Cursor modes

CURSOR PATTERN	CURSOR MODE	
	CMODE = 0	CMODE = 1
00	second cursor colour	second cursor colour
01	first cursor colour	first cursor colour
10	transparent	transparent
11	inverted input	auxiliary cursor colour

7.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R colour space in this block. The colour difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

A gain adjust option corrects the level swing of the graphics world (black-to-white as 0 to 255) to the required range of 16 to 235.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

7.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the colour phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7104E; SAA7105E input data is in accordance with *"ITU-R BT.656"*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

7.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 86.

An additional, programmable vertical filter supports the anti-flicker function. This filter is not available at upscaling factors of more than 2.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

Due to the re-interlacing, the circuit can perform upscaling by a maximum factor of 2. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 7.20.

An additional upscaling mode allows to increase the upscaling factor to maximum 4 as it is required for the old VGA modes like 320 $\times$ 240.

7.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I^2C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor.

7.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true colour tint.

7.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd-harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I^2C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA or HDTV mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 40 and 85 MHz. Two programmable dividers provide the actual clock to be used externally and internally. The dividers can be programmed to factors of 1, 2, 4 and 8. For the internal pixel clock, a divider ratio of 8 makes no sense and is thus forbidden.

The internal clock can be switched completely to the pixel clock input. In this event, the input FIFO is useless and will be bypassed.

The entire pixel clock generation can be locked to the vertical frequency. Both pixel clock dividers get re-initialized every field. Optionally, the DTO can be cleared with each V-sync. At proper programming, this will make the pixel clock frequency a precise multiple of the vertical and horizontal frequencies. This is required for some graphic controllers.

7.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

7.12 Encoder

7.12.1 Video path

The encoder generates luminance and colour subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7104E only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 6 and 7. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be used for the Y and C output.

The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 4 and 5.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, colour is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

7.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig.14.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

7.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

7.12.4 Closed Caption encoder

Using this circuit, data in accordance with the specification of Closed Caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

7.12.5 ANTI-TAPING (SAA7104E ONLY)

For more information contact your nearest Philips Semiconductors sales office.

7.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. The transfer curves of luminance and colour difference components of RGB are illustrated in Figs 8 and 9.

7.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10-bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the Y, C and optional RGB or C_R-Y-C_B outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually 75 Ω) during a pre-defined output. A flag in the I²C-bus status byte reflects whether a load is applied or not. In addition, an automatic sense mode can be activated which indicates a 75 Ω load at any of the three outputs at the dedicated interrupt pin TVD.

If the SAA7104E; SAA7105E is required to drive a second (auxiliary) VGA monitor or an HDTV set, the DACs receive the signal coming from the HD data path. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

7.15 HD data path

This data path allows the SAA7104E; SAA7105E to be used with VGA or HDTV monitors. It receives its data directly from the cursor generator and supports RGB and Y-P_B-P_R output formats (RGB not with Y-P_B-P_R input formats). No scaling is done in this mode.

A gain adjustment either leads the full level swing to the digital-to-analog converters or reduces the amplitude by a factor of 0.69. This enables sync pulses to be added to the signal as it is required for display units expecting signals with sync pulses, either regular or 3-level syncs.

7.16 Timing generator

The synchronization of the SAA7104E; SAA7105E is able to operate in two modes; slave mode and master mode.

In slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT.656 data stream via PD7 to PD0.

Only vertical frequencies of 50 and 60 Hz are allowed with the SAA7104E; SAA7105E. In slave mode, it is not possible to lock the encoders colour carrier to the line frequency with the PHRES bits.

In the (more common) master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{CBO}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.

$\overline{CBO}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{CBO}$ goes active. This signal is programmable and it is possible to adjust the following (see Figs 12 and 13):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field.

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7104E; SAA7105E will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines. The additional request pulses will be suppressed with LUTL set to logic 0; see Table 109. The other vertical timings do not change in this case, so the first active line can be number 2, counted from 0.

7.17 Pattern generator for HD sync pulses

The pattern generator provides appropriate synchronization patterns for the video data path in auxiliary monitor or HDTV mode. It provides maximum flexibility in terms of raster generation for all interlaced and non-interlaced computer graphics or ATSC formats. The sync engine is capable of providing a combination of event-value pairs which can be used to insert certain values in the outgoing data stream at specified times. It can also be used to generate digital signals associated with time events. These can be used as digital horizontal and vertical synchronization signals on pins HSM_CSYNC and VSM.

The picture position is adjustable through the programmable relationship between the sync pulses and the video contents.

The generation of embedded analog sync pulses is bound to a number of events which can be defined for a line. Several of these line timing definitions can exist in parallel. For the final sync raster composition a certain sequence of lines with different sync event properties has to be defined.

The sequence specifies a series of line types and the number of occurrences of this specific line type. Once the sequence has been completed, it restarts from the beginning. All pulse shapes are filtered internally in order to avoid ringing after analog post filters.

The sequence of the generated pulse stream must fit precisely to the incoming data stream in terms of the total number of pixels per line and lines per frame.

The sync engines flexibility is achieved by using a sequence of linked lists carrying the properties for the image, the lines as well as fractions of lines. Figure 3 illustrates the context between the various tables.

The first table serves as an array to hold the correct sequence of lines that compose the synchronization raster; it can contain up to 16 entries. Each entry holds a 4-bit index to the next table and a 10-bit counter value which specifies how often this particular line is invoked. If the necessary line count for a particular line exceeds the 10 bits, it has to use two table entries.

The 4-bit index in the line count array points to the line type array. It holds up to 15 entries (index 0 is not used), index 1 points to the first entry, index 2 to the second entry of the line type array etc.

Each entry of the line type array can hold up to 8 index pointers to another table. These indices point to portions of a line pulse pattern: A line could be split up e.g. into a sync, a blank, and an active portion followed by another blank portion, occupying four entries in one table line.

Each index of this table points to a particular line of the next table in the linked list. This table is called the line pattern array and each of the up to seven entries stores up to four pairs of a duration in pixel clock cycles and an index to a value table. The table entries are used to define portions of a line representing a certain value for a certain number of clock cycles.

The value specified in this table is actually another 3-bit index into a value array which can hold up to eight 8-bit values. If bit 4 (MSB) of the index is logic 1, the value is inserted into the G or Y signal, only; if bit 4 = 0, the associated value is inserted into all three signals.

Two additional bits of the entries in the value array (LSBs of the second byte) determine if the associated events appear as a digital pulse on the HSM_CSYNC and/or VSM outputs.

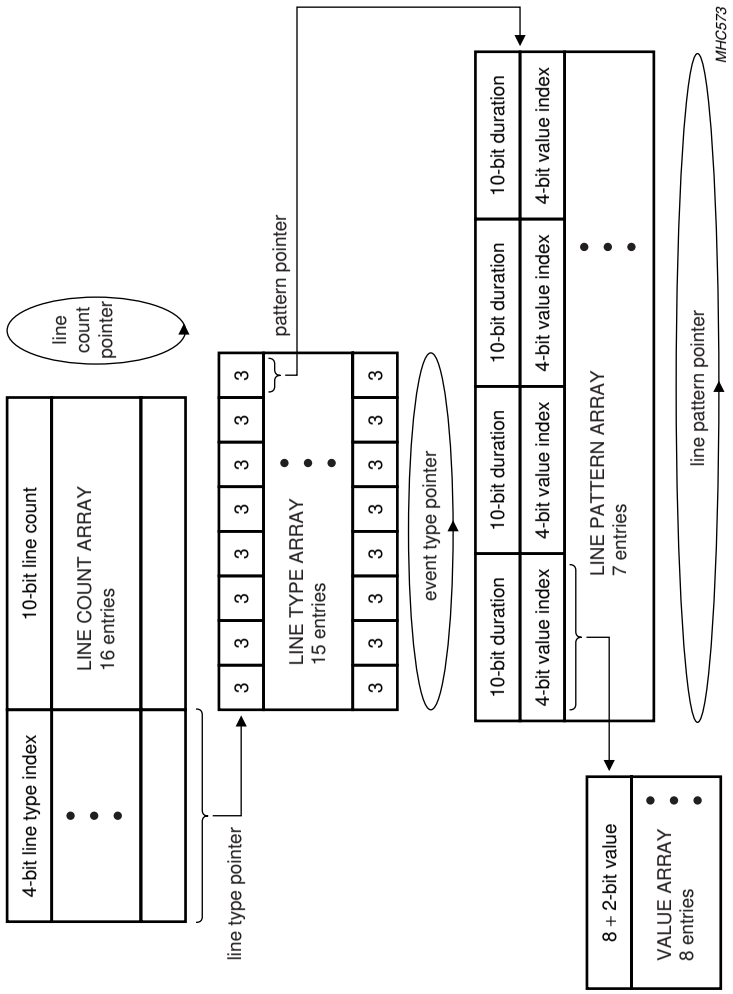

Fig.3 Context between the pattern generator tables for DH sync pulses.

To ease the trigger set-up for the sync generation module, a set of registers is provided to set up the screen raster which is defined as width and height. A trigger position can be specified as an x,y co-ordinate within the overall dimensions of the screen raster. If the x,y counter matches the specified co-ordinates, a trigger pulse is generated which pre-loads the tables with their initial values.

The listing in Table 6 outlines an example on how to set up the sync tables for a 1080i HD raster.

Important note:

Due to a problem in the programming interface, writing to the line pattern array (address D2) might destroy the data of the line type array (address D1). A work around is to write the line pattern array data before writing the line type array. Reading of the arrays is possible but all address pointers must be initialized before the next write operation.

Table 6 Example for set-up of the sync tables

SEQUENCE	COMMENT
Write to subaddress D0H	
00	points to first entry of line count array (index 0)
05 20	generate 5 lines of line type index 2 (this is the second entry of the line type array); will be the first vertical raster pulse
01 40	generate 1 line of line type index 4; will be sync-black-sync-black sequence after the first vertical pulse
0E 60	generate 14 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence
01 50	generate 1 line of line type index 5; will be the following line (line 563) with sync-black-sync-black-null sequence (null is equivalent to sync tip)
04 20	generate 4 lines of line type index 2; will be the second vertical raster pulse
01 30	generate 1 line of line type index 3; will be the following line with sync-null-sync-black sequence
0F 60	generate 15 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence; now, 1125 lines are defined
Write to subaddress D2H (insertion is done into all three analog output signals)	
00	points to first entry of line pattern array (index 1)
6F 33 2B 30 00 00 00 00	880 × value(3) + 44 × value(3); (subtract 1 from real duration)
6F 43 2B 30 00 00 00 00	880 × value(4) + 44 × value(3)
3B 30 BF 03 BF 03 2B 30	60 × value(3) + 960 × value(0) + 960 × value(0) + 44 × value(3)
2B 10 2B 20 57 30 00 00	44 × value(1) + 44 × value(2) + 88 × value(3)
3B 30 BF 33 BF 33 2B 30	60 × value(3) + 960 × value(3) + 960 × value(3) + 44 × value(3)
Write to subaddress D1H	
00	points to first entry of line type array (index 1)
34 00 00 00	use pattern entries 4 and 3 in this sequence (for sync and active video)
24 24 00 00	use pattern entries 4, 2, 4 and 2 in this sequence (for 2 × sync-black-null-black)
24 14 00 00	use pattern entries 4, 2, 4 and 1 in this sequence (for sync-black-null-black-null)
14 14 00 00	use pattern entries 4, 1, 4 and 1 in this sequence (for sync-black-sync-black)

SEQUENCE	COMMENT
14 24 00 00	use pattern entries 4, 1, 4 and 2 in this sequence (for sync-black-sync-black-null)
54 00 00 00	use pattern entries 4 and 5 in this sequence (for sync-black)
Write to subaddress D3H (no signals are directed to pins HSM_CSYNC and VSM)	
00	points to first entry of value array (index 0)
CC 00	black level, to be added during active video
80 00	sync level LOW (minimum output voltage)
0A 00	sync level HIGH (3-level sync)
CC 00	black level (needed elsewhere)
80 00	null (identical to sync level LOW)
Write to subaddress DCH	
0B	insertion is active, gain for signal is adapted accordingly

7.18 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.

The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data bytes following subaddress FFH. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.

The I²C-bus slave address is defined as 88H.

7.19 Power-down modes

In order to reduce the power consumption, the SAA7104E; SAA7105E supports 2 power-down modes, accessible via the I²C-bus. The analog power-down mode (DOWNA = 1) turns off the digital-to-analog converters and the pixel clock synthesizer. The digital power-down mode turns off all internal clocks and sets the digital outputs to LOW except the I²C-bus interface. The IC keeps its programming and can still be accessed in this mode, however not all registers can be read or written to. Reading or writing to the look-up tables, the cursor and the HD sync generator require a valid pixel clock. The typical supply current in full power-down is approximately 5 mA.

Because the analog power-down mode turns off the pixel clock synthesizer, there are limitations in some applications. If there is no pixel clock, the IC is not able to set its outputs to LOW. So, in most cases, DOWNA and DOWND should be set to logic 1 simultaneously. If the EIDIV bit is logic 1, it should be set to logic 0 before power-down.

7.20 Programming the SAA7104E; SAA7105E

The SAA7104E; SAA7105E needs to provide a continuous data stream at its analog outputs as well as receive a continuous stream of data from its data source. Because there is no frame memory isolating the data streams, restrictions apply to the input frame timings.

Input and output processing of the SAA7104E; SAA7105E are only coupled through the vertical frequencies. In master mode, the encoder provides a vertical sync and an odd/even pulse to the input processing. In slave mode, the encoder receives them.

The parameters of the input field are mainly given by the memory capacity of the SAA7104E; SAA7105E. The rule is that the scaler and thus the input processing needs to provide the video data in the same time frames as the encoder reads them. Therefore, the vertical active video times (and the vertical frequencies) need to be the same.

The second rule is that there has to be data in the buffer FIFO when the encoder enters the active video area. Therefore, the vertical offset in the input path needs to be a bit shorter than the offset of the encoder.

The following Sections give the set of equations required to program the IC for the most common application: A post processor in master mode with non-interlaced video input data.

Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- RiePclk: the ratio of internal to external pixel clock
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns).

7.20.1 TV DISPLAY WINDOW

At 60 Hz, the first visible pixel has the index 256, 710 pixels can be encoded; at 50 Hz, the index is 284, 702 pixels can be visible.

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 59.

ADWHS = 256 + 710 − OutPix (60 Hz);
ADWHS = 284 + 702 − OutPix (50 Hz);
ADWHE = ADWHS + OutPix × 2 (all frequencies)

For vertical, the procedure is the same. At 60 Hz, the first line with video information is number 19, 240 lines can be active. For 50 Hz, the numbers are 23 and 287; see Table 65.

$$FAL = 19 + \frac{240 - OutLin}{2} \text{ (60 Hz);}$$

$$FAL = 23 + \frac{287 - OutLin}{2} \text{ (50 Hz);}$$

LAL = FAL + OutLin (all frequencies)

Most TV sets use overscan, and not all pixels respectively lines are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is 10%, giving approximately 640 output pixels per line.

7.20.2 INPUT FRAME AND PIXEL CLOCK

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:

$$TPclk = \frac{262.5 \times 1716 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 262.5\right)} \text{ (60 Hz)}$$

$$TPclk = \frac{312.5 \times 1728 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 312.5\right)} \text{ (50 Hz)}$$

and for the pixel clock generator

$$PCL = \frac{TXclk}{TPclk} \times 2^{20 + PCLE} \text{ (all frequencies);}$$

see Tables 68, 70 and 71. The divider PCLE should be set according to Table 70. PCLI may be set to a lower or the same value. Setting a lower value means that the internal pixel clock is higher and the data get sampled up. The difference may be 1 at 640 × 480 pixels resolution and 2 at resolutions with 320 pixels per line as a rule of thumb. This allows horizontal upscaling by a maximum factor of 2 respectively 4 (this is the parameter RiePclk).

$$PCLI = PCLE - \frac{\log RiePclk}{\log 2} \text{ (all frequencies)}$$

The equations ensure that the last line of the field has the full number of clock cycles. Many graphic controllers require this. Note that the bit PCLSY needs to be set to ensure that there is not even a fraction of a clock left at the end of the field.

7.20.3 HORIZONTAL SCALER

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX ≤ HLEN is fulfilled. Values given by the VESA display timings are preferred.

HLEN = InPpl × RiePclk − 1

$$XPIX = \frac{InPix}{2} \times RiePclk$$

$$XINC = \frac{OutPix}{InPix} \times \frac{4096}{RiePclk}$$

XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1.

7.20.4 VERTICAL SCALER

The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:

$$YOFS = \frac{FAL \times 1716 \times TXclk}{InPpl \times TPclk} - 2.5 \quad (60\ Hz)$$

$$YOFS = \frac{FAL \times 1728 \times TXclk}{InPpl \times TPclk} - 2.5 \quad (50\ Hz)$$

In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

YPIX = InLin

YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth. Note that the maximum value for YINC is 4095. It might be necessary to reduce the value of YSKIP to fulfil this requirement.

$$YINC = \frac{OutLin}{InLin + 2} \times \left(1 + \frac{YSKIP}{4095}\right) \times 4096$$

$$YIWGTO = \frac{YINC}{2} + 2048$$

$$YIWGTE = \frac{YINC - YSKIP}{2}$$

When YINC = 0 it sets the scaler to scaling factor 1. The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.

It should be noted that these equations assume that the input is non-interlaced but the output is interlaced. If the input is interlaced, the initial weighting factors need to be adapted to obtain the proper phase offsets in the output frame.

If vertical upscaling beyond the upper capabilities is required, the parameter YUPSC may be set to logic 1. This extends the maximum vertical scaling factor by a factor of 2. Only the parameter YINC is affected, it needs to be divided by two to get the same effect.

There are restrictions in this mode:

- The vertical filter YFILT is not available in this mode; the circuit will ignore this value
- The horizontal blanking needs to be long enough to transfer an output line between 2 memory locations. This is 710 internal pixel clocks.

  Or the upscaling factor needs to be limited to 1.5 and the horizontal upscaling factor is also limited to less than ~1.5. In this case a normal blanking length is sufficient.

7.21 Input levels and formats

The SAA7104E; SAA7105E accepts digital Y, C_B, C_R or RGB data with levels (digital codes) in accordance with *"ITU-R BT.601"*. An optional gain adjustment also allows to accept data with the full level swing of 0 to 255.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features an individual gain setting for luminance (GY) and colour difference signals (GCD). Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

The SAA7104E; SAA7105E has special input cells for the VGC port. They operate at a wider supply voltage range and have a strict input threshold at $^1/_2V_{DDD}$. To achieve full speed of these cells, the EIDIV bit needs to be set to logic 1. Note that the impedance of these cells is approximately 6 kΩ. This may cause trouble with the bootstrapping pins of some graphic chips. So the power-on reset forces the bit to logic 0, the input impedance is regular in this mode.

Table 7 *"ITU-R BT.601"* signal component levels

COLOUR	SIGNALS[1]					
	Y	C_B	C_R	R	G	B
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

Note

1. Transformation:
   a) $R = Y + 1.3707 \times (C_R - 128)$
   b) $G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$
   c) $B = Y + 1.7324 \times (C_B - 128)$.

Table 8 Usage of bits SLOT and EDGE

DATA SLOT CONTROL (EXAMPLE FOR FORMAT 0)			
SLOT	**EDGE**	**1st DATA**	**2nd DATA**
0	0	at rising edge G3/Y3	at falling edge R7/C_R7
0	**1**	**at falling edge G3/Y3**	**at rising edge R7/C_R7**
1	0	at rising edge R7/C_R7	at falling edge G3/Y3
1	1	at falling edge R7/C_R7	at rising edge G3/Y3

Table 9 Pin assignment for input format 0

8 + 8 + 8-BIT 4 : 4 : 4 NON-INTERLACED RGB/C_B-Y-C_R		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD11	G3/Y3	R7/C_R7
PD10	G2/Y2	R6/C_R6
PD9	G1/Y1	R5/C_R5
PD8	G0/Y0	R4/C_R4
PD7	B7/C_B7	R3/C_R3
PD6	B6/C_B6	R2/C_R2
PD5	B5/C_B5	R1/C_R1
PD4	B4/C_B4	R0/C_R0
PD3	B3/C_B3	G7/Y7
PD2	B2/C_B2	G6/Y6
PD1	B1/C_B1	G5/Y5
PD0	B0/C_B0	G4/Y4

Table 10 Pin assignment for input format 1

5 + 5 + 5-BIT 4 : 4 : 4 NON-INTERLACED RGB		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD7	G2	X
PD6	G1	R4
PD5	G0	R3
PD4	B4	R2
PD3	B3	R1
PD2	B2	R0
PD1	B1	G4
PD0	B0	G3

Table 11 Pin assignment for input format 2

5 + 6 + 5-BIT 4 : 4 : 4 NON-INTERLACED RGB		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD7	G2	R4
PD6	G1	R3
PD5	G0	R2
PD4	B4	R1
PD3	B3	R0
PD2	B2	G5
PD1	B1	G4
PD0	B0	G3

Table 12 Pin assignment for input format 3

8 + 8 + 8-BIT 4 : 2 : 2 NON-INTERLACED C_B-Y-C_R				
PIN	**FALLING CLOCK EDGE n**	**RISING CLOCK EDGE n**	**FALLING CLOCK EDGE n + 1**	**RISING CLOCK EDGE n + 1**
PD7	C_B7(0)	Y7(0)	C_R7(0)	Y7(1)
PD6	C_B6(0)	Y6(0)	C_R6(0)	Y6(1)
PD5	C_B5(0)	Y5(0)	C_R5(0)	Y5(1)
PD4	C_B4(0)	Y4(0)	C_R4(0)	Y4(1)
PD3	C_B3(0)	Y3(0)	C_R3(0)	Y3(1)
PD2	C_B2(0)	Y2(0)	C_R2(0)	Y2(1)
PD1	C_B1(0)	Y1(0)	C_R1(0)	Y1(1)
PD0	C_B0(0)	Y0(0)	C_R0(0)	Y0(1)

Table 13 Pin assignment for input format 4

8 + 8 + 8-BIT 4 : 2 : 2 INTERLACED C_B-Y-C_R (ITU-R BT.656, 27 MHz CLOCK)				
PIN	**RISING CLOCK EDGE n**	**RISING CLOCK EDGE n + 1**	**RISING CLOCK EDGE n + 2**	**RISING CLOCK EDGE n + 3**
PD7	C_B7(0)	Y7(0)	C_R7(0)	Y7(1)
PD6	C_B6(0)	Y6(0)	C_R6(0)	Y6(1)
PD5	C_B5(0)	Y5(0)	C_R5(0)	Y5(1)
PD4	C_B4(0)	Y4(0)	C_R4(0)	Y4(1)
PD3	C_B3(0)	Y3(0)	C_R3(0)	Y3(1)
PD2	C_B2(0)	Y2(0)	C_R2(0)	Y2(1)
PD1	C_B1(0)	Y1(0)	C_R1(0)	Y1(1)
PD0	C_B0(0)	Y0(0)	C_R0(0)	Y0(1)

Table 14 Pin assignment for input format 5; note 1

8-BIT NON-INTERLACED INDEX COLOUR		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD11	X	X
PD10	X	X
PD9	X	X
PD8	X	X
PD7	INDEX7	X
PD6	INDEX6	X
PD5	INDEX5	X
PD4	INDEX4	X
PD3	INDEX3	X
PD2	INDEX2	X
PD1	INDEX1	X
PD0	INDEX0	X

Note

1. X = don’t care.

Table 15 Pin assignment for input format 6

8 + 8 + 8-BIT 4 : 4 : 4 NON-INTERLACED RGB/C_B-Y-C_R		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD11	G4/Y4	R7/C_R7
PD10	G3/Y3	R6/C_R6
PD9	G2/Y2	R5/C_R5
PD8	B7/C_B7	R4/C_R4
PD7	B6/C_B6	R3/C_R3
PD6	B5/C_B5	G7/Y7
PD5	B4/C_B4	G6/Y6
PD4	B3/C_B3	G5/Y5
PD3	G0/Y0	R2/C_R2
PD2	B2/C_B2	R1/C_R1
PD1	B1/C_B1	R0/C_R0
PD0	B0/C_B0	G1/Y1

7.22 Bit allocation map

Table 16 Slave receiver (slave address 88H)

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Status byte (read only)	00	VER2	VER1	VER0	CCRDO	CCRDE	(1)	FSEQ	O_E
Null	01 to 15	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Common DAC adjust fine	16	(1)	(1)	(1)	(1)	DACF3	DACF2	DACF1	DACF0
R DAC adjust coarse	17	(1)	(1)	(1)	RDACC4	RDACC3	RDACC2	RDACC1	RDACC0
G DAC adjust coarse	18	(1)	(1)	(1)	GDACC4	GDACC3	GDACC2	GDACC1	GDACC0
B DAC adjust coarse	19	(1)	(1)	(1)	BDACC4	BDACC3	BDACC2	BDACC1	BDACC0
MSM threshold	1A	MSMT7	MSMT6	MSMT5	MSMT4	MSMT3	MSMT2	MSMT1	MSMT0
Monitor sense mode	1B	MSM	MSA	MSOE	(1)	(1)	RCOMP	GCOMP	BCOMP
Chip ID (02B or 03B, read only)	1C	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	(1)	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28	(1)	(1)	BS5	BS4	BS3	BS2	BS1	BS0
Sync reset enable, burst end	29	SRES	(1)	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2A	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2B	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2C	CGEN	(1)	(1)	(1)	CG19	CG18	CG17	CG16
Output port control	2D	VBSEN	CVBSEN1	CVBSEN0	CEN	ENCOFF	CLK2EN	CVBSEN2	(1)
Null	2E to 36	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Input path control	37	(1)	YUPSC	YFIL1	YFIL0	(1)	CZOOM	IGAIN	XINT
Gain luminance for RGB	38	(1)	(1)	(1)	GY4	GY3	GY2	GY1	GY0
Gain colour difference for RGB	39	(1)	(1)	(1)	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3A	CBENB	(1)	SYNTV	SYMP	DEMOFF	CSYNC	Y2C	UV2C
VPS enable, input control 2	54	VPSEN	(1)	GPVAL	GPEN	(1)	(1)	EDGE	SLOT
VPS byte 5	55	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	(1)	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	(1)	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Standard control	61	DOWND	DOWNA	INPI	YGS	(1)	SCBW	PAL	FISE
Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Null	6B	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	NVTRIG	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLC0
Closed Caption, teletext enable	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
Active display window horizontal start	70	ADWHS7	ADWHS6	ADWHS5	ADWHS4	ADWHS3	ADWHS2	ADWHS1	ADWHS0
Active display window horizontal end	71	ADWHE7	ADWHE6	ADWHE5	ADWHE4	ADWHE3	ADWHE2	ADWHE1	ADWHE0
MSBs ADWH	72	(1)	ADWHE10	ADWHE9	ADWHE8	(1)	ADWHS10	ADWHS9	ADWHS8
TTX request horizontal start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request horizontal delay	74	(1)	(1)	(1)	(1)	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance	75	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	(1)	(1)	(1)
TTX odd request vertical start	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request vertical start	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
TTX even request vertical end	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7C	TTX60	LAL8	TTXO	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Disable TTX line	7E	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7F	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13
FIFO status (read only)	80	(1)	(1)	(1)	(1)	IFERR	BFERR	OVFL	UDFL
Pixel clock 0	81	PCL07	PCL06	PCL05	PCL04	PCL03	PCL02	PCL01	PCL00
Pixel clock 1	82	PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL09	PCL08
Pixel clock 2	83	PCL23	PCL22	PCL21	PCL20	PCL19	PCL18	PCL17	PCL16
Pixel clock control	84	DCLK	PCLSY	IFRA	IFBP	PCLE1	PCLE0	PCLI1	PCLI0
FIFO control	85	EIDIV	(1)	(1)	(1)	FILI3	FILI2	FILI1	FILI0
Null	86 to 8F	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Horizontal offset	90	XOFS7	XOFS6	XOFS5	XOFS4	XOFS3	XOFS2	XOFS1	XOFS0
Pixel number	91	XPIX7	XPIX6	XPIX5	XPIX4	XPIX3	XPIX2	XPIX1	XPIX0
Vertical offset odd	92	YOFSO7	YOFSO6	YOFSO5	YOFSO4	YOFSO3	YOFSO2	YOFSO1	YOFSO0
Vertical offset even	93	YOFSE7	YOFSE6	YOFSE5	YOFSE4	YOFSE3	YOFSE2	YOFSE1	YOFSE0
MSBs	94	YOFSE9	YOFSE8	YOFSO9	YOFSO8	XPIX9	XPIX8	XOFS9	XOFS8
Line number	95	YPIX7	YPIX6	YPIX5	YPIX4	YPIX3	YPIX2	YPIX1	YPIX0
Scaler CTRL, MCB YPIX	96	EFS	PCBN	SLAVE	ILC	YFIL	(1)	YPIX9	YPIX8
Sync control	97	HFS	VFS	OFS	PFS	OVS	PVS	OHS	PHS
Line length	98	HLEN7	HLEN6	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0
Input delay, MSB line length	99	IDEL3	IDEL2	IDEL1	IDEL0	HLEN11	HLEN10	HLEN9	HLEN8
Horizontal increment	9A	XINC7	XINC6	XINC5	XINC4	XINC3	XINC2	XINC1	XINC0
Vertical increment	9B	YINC7	YINC6	YINC5	YINC4	YINC3	YINC2	YINC1	YINC0
MSBs vertical and horizontal increment	9C	YINC11	YINC10	YINC9	YINC8	XINC11	XINC10	XINC9	XINC8
Weighting factor odd	9D	YIWGTO7	YIWGTO6	YIWGTO5	YIWGTO4	YIWGTO3	YIWGTO2	YIWGTO1	YIWGTO0
Weighting factor even	9E	YIWGTE7	YIWGTE6	YIWGTE5	YIWGTE4	YIWGTE3	YIWGTE2	YIWGTE1	YIWGTE0
Weighting factor MSB	9F	YIWGTE11	YIWGTE10	YIWGTE9	YIWGTE8	YIWGTO11	YIWGTO10	YIWGTO9	YIWGTO8
Vertical line skip	A0	YSKIP7	YSKIP6	YSKIP5	YSKIP4	YSKIP3	YSKIP2	YSKIP1	YSKIP0