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SAA7108AE; SAA7109AE

HD-CODEC

Rev. 03 — 6 February 2007 Product data sheet

1. General description

The SAA7108AE; SAA7109AE is a new multistandard video decoder and encoder chip, offering high quality video input and TV output processing as required by PC-99 specifications. It enables hardware manufacturers to implement versatile video functions on a significantly reduced printed-circuit board area at very competitive costs.

Separate pins for supply voltages as well as for I^{2}C-bus control and boundary scan test have been provided for the video encoder and decoder sections to ensure both flexible handling and optimized noise behavior.

The **video encoder** is used to encode PC graphics data at maximum 1280 × 1024 resolution (optionally 1920 × 1080 interlaced) to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum 5 lines) ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 1280 × 1024 resolution/60 Hz (PIXCLK < 85 MHz). Alternatively this port can provide Y, P_B and P_R signals for HDTV monitors.

The encoder section includes a sync/clock generator and on-chip DACs.

All inputs intended to interface to the host graphics controller are designed for low-voltage signals down to 1.1 V and up to 3.45 V.

The **video decoder**, a 9-bit video input processor, is a combination of a 2-channel analog pre-processing circuit including source selection, anti-aliasing filter and Analog-to-Digital Converter (ADC), automatic clamp and gain control, a Clock Generation Circuit (CGC), and a digital multistandard decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM).

The decoder includes a brightness, contrast and saturation control circuit, a multistandard VBI data slicer and a 27 MHz VBI data bypass. The pure 3.3 V (5 V compatible) CMOS circuit SAA7108AE; SAA7109AE, consisting of an analog front-end and digital video decoder, a digital video encoder and analog back-end, is a highly integrated circuit especially designed for desktop video applications.

The decoder is based on the principle of line-locked clock decoding and is able to decode the color of PAL, SECAM and NTSC signals into ITU-R BT.601 compatible color component values.

The encoder can operate fully independently at its own variable pixel clock, transporting graphics input data, and at the line-locked, single crystal-stable video encoding clock.

As an option, it is possible to slave the video PAL/NTSC encoding to the video decoder clock with the encoder FIFO acting as a buffer to decouple the line-locked decoder clock from the crystal-stable encoder clock.

2. Features

2.1 Video decoder

- Six analog inputs, internal analog source selectors, e.g. 6 × CVBS or (2 × Y/C and 2 × CVBS) or (1 × Y/C and 4 × CVBS)
- Two analog preprocessing channels in differential CMOS style for best S/N performance
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 9-bit video CMOS Analog-to-Digital Converters (ADCs), digitized CVBS or Y/C signals are available on the Image Port Data (IPD) port under I^2C-bus control
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal sync processing and clock generation, horizontal and vertical sync detection
- Requires only one crystal (either 24.576 MHz or 32.11 MHz) for all standards
- Automatic detection of 50 Hz and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, combination PAL N, PAL M, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM
- User programmable luminance peaking or aperture correction
- Cross-color reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Brightness Contrast Saturation (BCS) and hue control on-chip
- Two multifunctional real-time output pins controlled by the I^2C-bus
- Multistandard VBI data slicer decoding World Standard Teletext (WST), North-American Broadcast Text System (NABTS), Closed Caption (CC), Wide Screen Signalling (WSS), Video Programming System (VPS), Vertical Interval Time Code (VITC) variants (EBU/SMPTE) etc.
- Standard ITU 656 Y-C_B-C_R 4 : 2 : 2 format (8-bit) on IPD output bus
- Enhanced ITU 656 output format on IPD output bus containing:
  - Active video
  - Raw CVBS data for INTERCAST applications (27 MHz data rate)
  - Decoded VBI data
- Detection of copy protected input signals according to the Macrovision standard. Can be used to prevent unauthorized recording of pay-TV or video tape signals

2.2 Video scaler

- Both up and downscaling
- Conversion to square pixel format
- NTSC to 288 lines (video phone)
- Phase accuracy better than $^1/_{64}$ pixel or line, horizontally or vertically
- Independent scaling definitions for odd and even fields
- Anti-alias filter for horizontal scaling
- Provides output as:
  - Scaled active video
  - Raw CVBS data for INTERCAST, WAVE-PHORE, POPCON applications or general VBI data decoding (27 MHz or sample rate converted)
- Local video output for Y-C_B-C_R 4 : 2 : 2 format (VMI, VIP and ZV)

2.3 Video encoder

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- Supports Intel Digital Video Out (DVO) low-voltage interfacing to graphics controller
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 85 MHz at double edged clocking, synthesized on-chip or from external source
- Programmable assignment of clock edge to bytes (in double edged mode)
- Synthesizable pixel clock (PIXCLK) with minimized output jitter, can be used as reference clock for the VGC, as well
- PIXCLK output and bi-phase PIXCLK input (VGC clock loop-through possible)
- Hot-plug detection through dedicated interrupt pin
- Supported VGA resolutions for PAL or NTSC legacy video output up to 1280 × 1024 graphics data at 60 Hz or 50 Hz frame rate
- Supported VGA resolutions for HDTV output up to 1920 × 1080 interlaced graphics data at 60 Hz or 50 Hz frame rate
- Three Digital-to-Analog Converters (DACs) for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) at 27 MHz sample rate (signals in parenthesis are optionally selected), all at 10-bit resolution
- Non-interlaced C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling
- Downscaling and upscaling from 50 % to 400 %
- Optional interlaced C_B-Y-C_R input of Digital Versatile Disk (DVD) signals
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode, maximum 85 MHz)
- 3 × 256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- HDTV up to 1920 × 1080 interlaced and 1280 × 720 progressive, including 3-level sync pulses
- Programmable border color of underscan area
- Programmable 5-line anti-flicker filter
- On-chip 27 MHz crystal oscillator (3rd harmonic or fundamental 27 MHz crystal)
- Fast I^2C-bus control port (400 kHz)

- Encoder can be master or slave
- Adjustable output levels for the DACs
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Color Bar Generator (CBG)
- Optional support of various Vertical Blanking Interval (VBI) data insertion
- Macrovision Pay-per-View copy protection system rev. 7.01, rev. 6.1 and rev. 1.03 (525p) as option; this applies to the SAA7108AE only.

2.4 Common features

- 5 V tolerant digital inputs and I/O ports
- I^2C-bus controlled (full read-back ability by an external controller, bit rate up to 400 kbit/s)
- Versatile Power-save modes
- Boundary scan test circuit complies with the *"IEEE Std. 1149.b1-1994"* (separate ID codes for decoder and encoder)
- LBGA156 package
- Moisture Sensitive Level (MSL): e3

3. Applications

- Notebook (low-power consumption)
- PCMCIA card application
- AGP based graphics cards
- PC editing
- Image processing
- Video phone applications
- INTERCAST and PC teletext applications
- Security applications
- Hybrid satellite set-top boxes

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDD}	digital supply voltage			3.15	3.3	3.45	V
V_{DDA}	analog supply voltage			3.15	3.3	3.45	V
T_{amb}	ambient temperature			0	-	70	°C
P_{A+D}	analog and digital power dissipation		[1]	-	-	1.7	W

[1] Power dissipation is extremely dependent on programming and selected application.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SAA7108AE	LBGA156	plastic low profile ball grid array package; 156 balls; body 15 × 15 × 1.05 mm	SOT700-1
SAA7109AE			

6. Block diagram

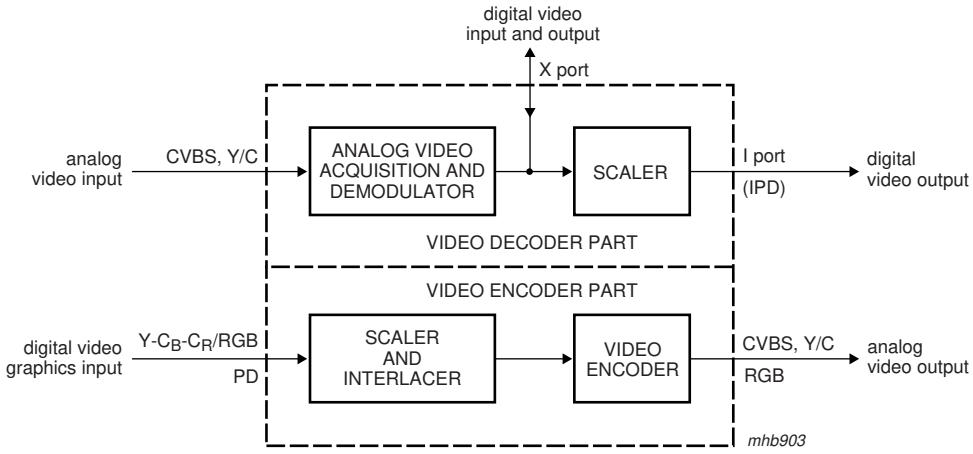


Fig 1. Simplified block diagram

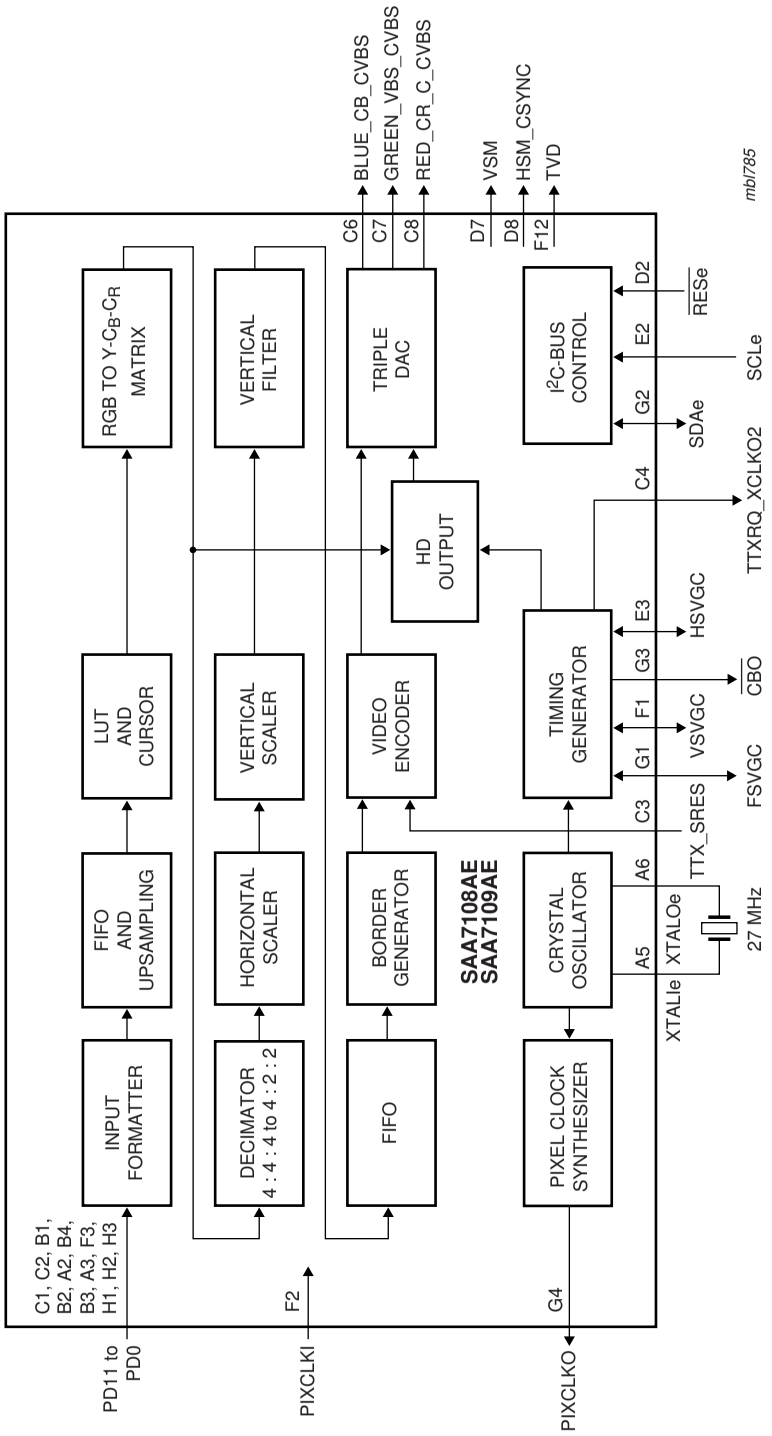
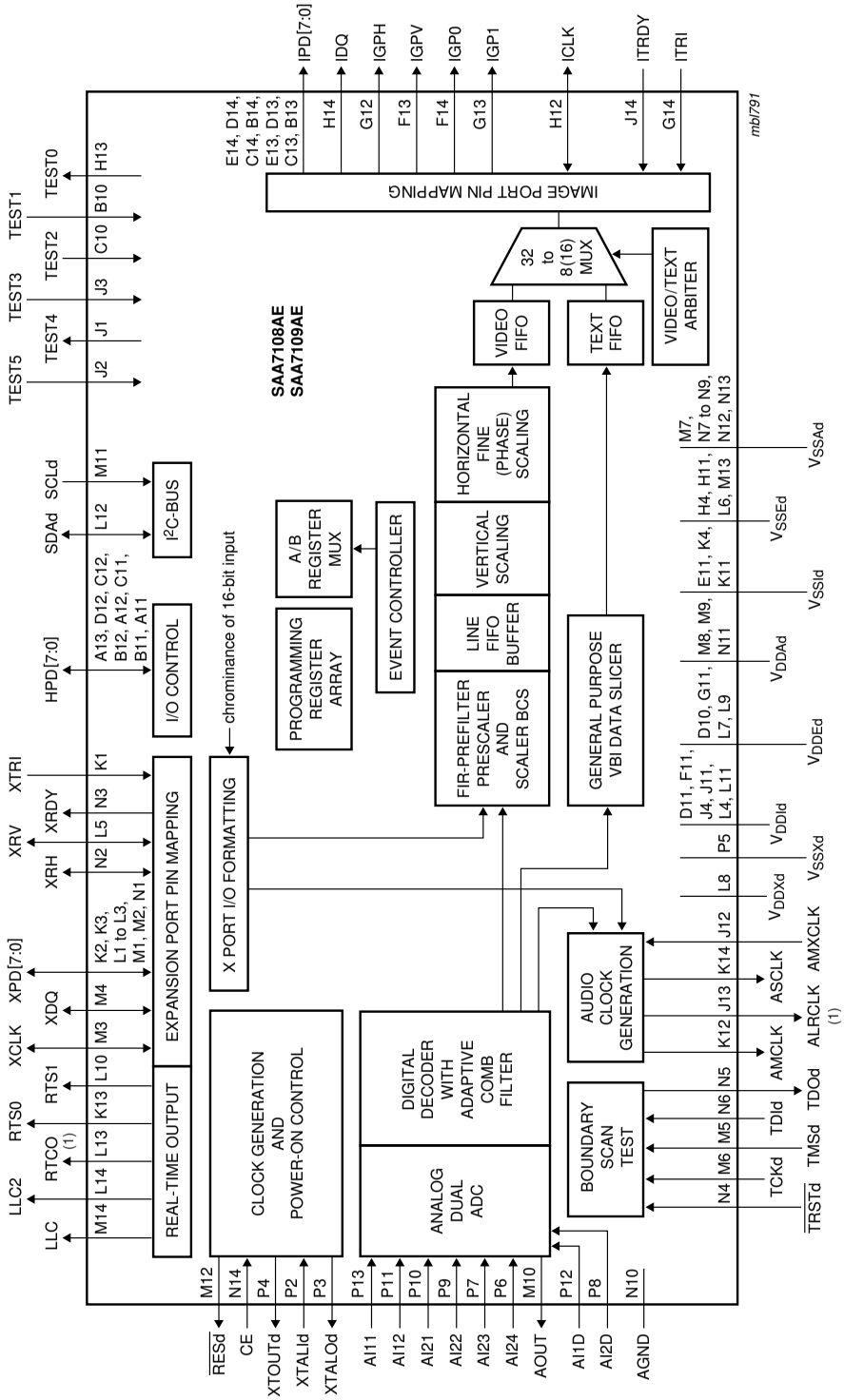


Fig 2. Block diagram (video encoder part)



(1) The pins RTCO and ALRCLK are used for configuration of the I²C-bus interface and the definition of the crystal oscillator frequency at RESET (pin strapping).

Fig 3. Block diagram (video decoder part)

7. Pinning information

7.1 Pinning

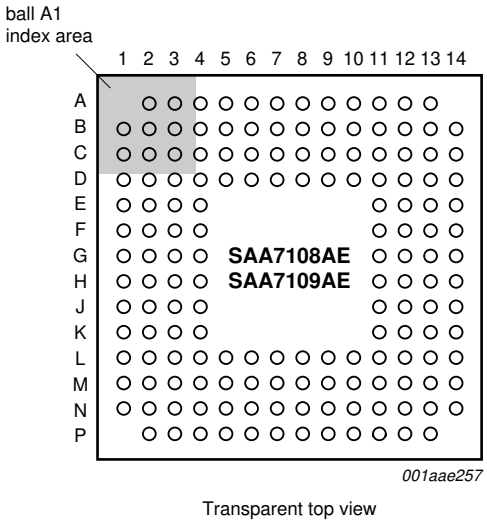


Fig 4. Pin configuration (LBGA156)

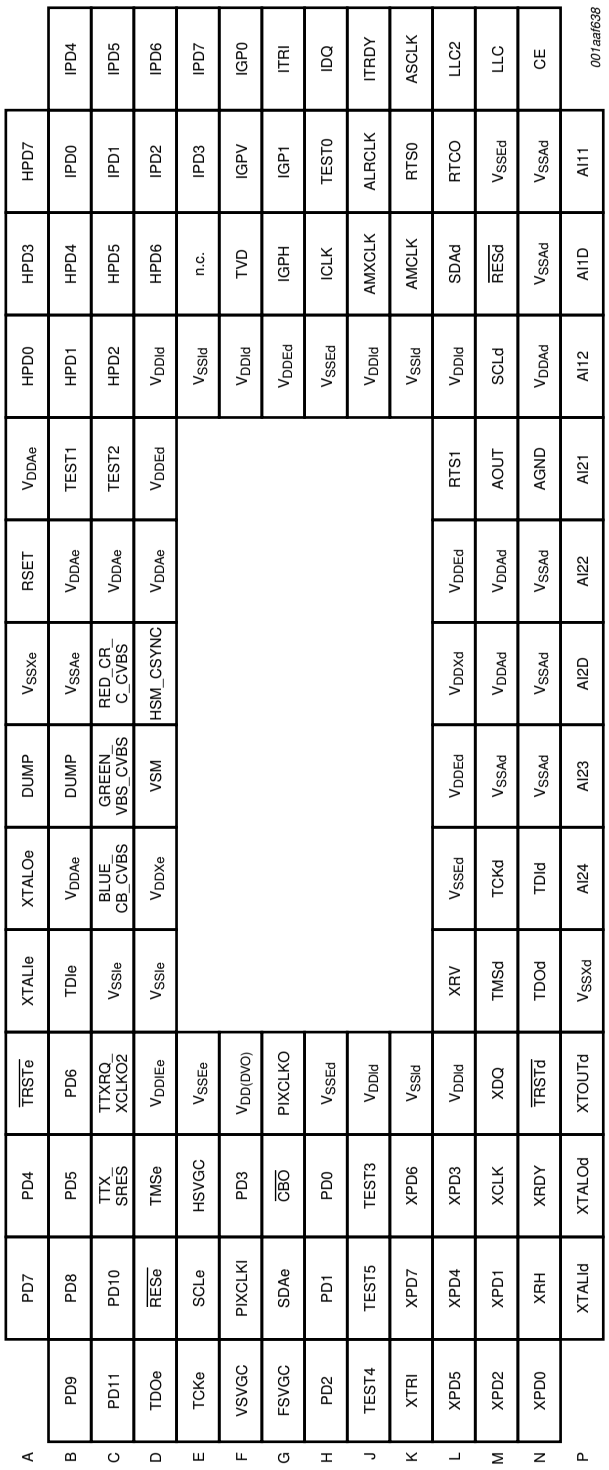


Fig 5. Pin configuration (LBGA156 top view)

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A2	PD7	A3	PD4	A4	$\overline{TRSTe}$	A5	XTALIe
A6	XTALOe	A7	DUMP	A8	V_{SSXe}	A9	RSET
A10	V_{DDAe}	A11	HPD0	A12	HPD3	A13	HPD7
B1	PD9	B2	PD8	B3	PD5	B4	PD6
B5	TDIe	B6	V_{DDAe}	B7	DUMP	B8	V_{SSAe}
B9	V_{DDAe}	B10	TEST1	B11	HPD1	B12	HPD4
B13	IPD0	B14	IPD4				
C1	PD11	C2	PD10	C3	TTX_SRES	C4	TTXRQ_XCLKO2
C5	V_{SSIe}	C6	BLUE_CB_CVBS	C7	GREEN_VBS_CVBS	C8	RED_CR_C_CVBS
C9	V_{DDAe}	C10	TEST2	C11	HPD2	C12	HPD5
C13	IPD1	C14	IPD5				
D1	TDOe	D2	$\overline{RESe}$	D3	TMSe	D4	V_{DDIEe}
D5	V_{SSIe}	D6	V_{DDXe}	D7	VSM	D8	HSM_CSYNC
D9	V_{DDAe}	D10	V_{DDEd}	D11	V_{DDId}	D12	HPD6
D13	IPD2	D14	IPD6				
E1	TCKe	E2	SCLe	E3	HSVGC	E4	V_{SSEe}
E11	V_{SSId}	E12	n.c.	E13	IPD3	E14	IPD7
F1	VSVGC	F2	PIXCLKI	F3	PD3	F4	$V_{DD(DVO)}$
F11	V_{DDId}	F12	TVD	F13	IGPV	F14	IGP0
G1	FSVGC	G2	SDAe	G3	$\overline{CBO}$	G4	PIXCLKO
G11	V_{DDEd}	G12	IGPH	G13	IGP1	G14	ITRI
H1	PD2	H2	PD1	H3	PD0	H4	V_{SSEd}
H11	V_{SSEd}	H12	ICLK	H13	TEST0	H14	IDQ
J1	TEST4	J2	TEST5	J3	TEST3	J4	V_{DDId}
J11	V_{DDId}	J12	AMXCLK	J13	ALRCLK	J14	ITRDY
K1	XTRI	K2	XPD7	K3	XPD6	K4	V_{SSId}
K11	V_{SSId}	K12	AMCLK	K13	RTS0	K14	ASCLK
L1	XPD5	L2	XPD4	L3	XPD3	L4	V_{DDId}
L5	XRV	L6	V_{SSEd}	L7	V_{DDEd}	L8	V_{DDXd}
L9	V_{DDEd}	L10	RTS1	L11	V_{DDId}	L12	SDAd
L13	RTCO	L14	LLC2				
M1	XPD2	M2	XPD1	M3	XCLK	M4	XDQ
M5	TMSd	M6	TCKd	M7	V_{SSAd}	M8	V_{DDAd}
M9	V_{DDAd}	M10	AOUT	M11	SCLd	M12	$\overline{RESd}$
M13	V_{SSEd}	M14	LLC				
N1	XPD0	N2	XRH	N3	XRDY	N4	$\overline{TRSTd}$
N5	TDOd	N6	TDId	N7	V_{SSAd}	N8	V_{SSAd}
N9	V_{SSAd}	N10	AGND	N11	V_{DDAd}	N12	V_{SSAd}
N13	V_{SSAd}	N14	CE				

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
P2	XTALId	P3	XTALOd	P4	XTOUTd	P5	V_{SSXd}
P6	AI24	P7	AI23	P8	AI2D	P9	AI22
P10	AI21	P11	AI12	P12	AI1D	P13	AI11

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
PD7	A2	I	MSB of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD4	A3	I	MSB – 3 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
$\overline{TRSTe}$	A4	I/pu	test reset input for Boundary Scan Test (BST) (encoder); active LOW; with internal pull-up[2][3]
XTALIe	A5	I	27 MHz crystal input (encoder)
XTALOe	A6	O	27 MHz crystal output (encoder)
DUMP	A7	O	DAC reference pin (encoder); 12 Ω resistor connected to V_{SSAe}
V_{SSXe}	A8	S	ground for oscillator (encoder)
RSET	A9	O	DAC reference pin (encoder); 1 kΩ resistor connected to V_{SSAe}
V_{DDAe}	A10	S	3.3 V analog supply voltage (encoder)
HPD0	A11	I/O	MSB – 7 of Host Port Data (HPD) output bus
HPD3	A12	I/O	MSB – 4 of HPD output bus
HPD7	A13	I/O	MSB of HPD output bus
PD9	B1	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats
PD8	B2	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats
PD5	B3	I	MSB – 2 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD6	B4	I	MSB – 1 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
TDIe	B5	I/pu	test data input for BST (encoder)[4]
V_{DDAe}	B6	S	3.3 V analog supply voltage (encoder)
DUMP	B7	O	DAC reference pin (encoder); connected to A7
V_{SSAe}	B8	S	analog ground (encoder)
V_{DDAe}	B9	S	3.3 V analog supply voltage (encoder)
TEST1	B10	I	scan test input 1; do not connect
HPD1	B11	I/O	MSB – 6 of HPD output bus
HPD4	B12	I/O	MSB – 3 of HPD output bus
IPD0	B13	O	MSB – 7 of IPD output bus
IPD4	B14	O	MSB – 3 of Image Port Data (IPD) output bus
PD11	C1	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
PD10	C2	I	see Table 12, Table 17 and Table 18 for pin assignment with different encoder input formats
TTX_SRES	C3	I	teletext input or sync reset input (encoder)
TTXRQ_XCLKO2	C4	O	teletext request output or 13.5 MHz clock output of the crystal oscillator (encoder)
V_{SSIe}	C5	S	digital ground core (encoder)
BLUE_CB_CVBS	C6	O	BLUE or C_B or CVBS output
GREEN_VBS_CVBS	C7	O	GREEN or VBS or CVBS output
RED_CR_C_CVBS	C8	O	RED or C_R or C or CVBS output
V_{DDAe}	C9	S	3.3 V analog supply voltage (encoder)
TEST2	C10	I	scan test input 2; do not connect
HPD2	C11	I/O	MSB – 5 of HPD output bus
HPD5	C12	I/O	MSB – 2 of HPD output bus
IPD1	C13	O	MSB – 6 of IPD output bus
IPD5	C14	O	MSB – 2 of IPD output bus
TDOe	D1	O	test data output for BST (encoder)[4]
$\overline{RESe}$	D2	I	reset input (encoder); active LOW
TMSe	D3	I/pu	test mode select input for BST (encoder)[4]
V_{DDIEe}	D4	S	3.3 V digital supply voltage for core and peripheral cells (encoder)
V_{SSIe}	D5	S	digital ground core (encoder)
V_{DDXe}	D6	S	3.3 V supply voltage for oscillator (encoder)
VSM	D7	O	vertical synchronization output to VGA monitor (non-interlaced)
HSM_CSYNC	D8	O	horizontal synchronization output to VGA monitor (non-interlaced) or composite sync for RGB-SCART
V_{DDAe}	D9	S	3.3 V analog supply voltage (encoder)
V_{DDEd}	D10	S	3.3 V digital supply voltage for peripheral cells (decoder)
V_{DDId}	D11	S	3.3 V digital supply voltage for core (decoder)
HPD6	D12	I/O	MSB – 1 of HPD output bus
IPD2	D13	O	MSB – 5 of IPD output bus
IPD6	D14	O	MSB – 1 of IPD output bus
TCKe	E1	I/pu	test clock input for BST (encoder)[4]
SCLe	E2	I(/O)	serial clock input (I^2C-bus encoder) with inactive output path
HSVGC	E3	I/O	horizontal synchronization output to Video Graphics Controller (VGC) (optional input)
V_{SSEe}	E4	S	digital ground peripheral cells (encoder)
V_{SSId}	E11	S	digital ground core (decoder)
n.c.	E12	-	not connected
IPD3	E13	O	MSB – 4 of IPD output bus
IPD7	E14	O	MSB of IPD output bus
VSVGC	F1	I/O	vertical synchronization output to VGC (optional input)
PIXCLKI	F2	I	pixel clock input (looped through)

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
PD3	F3	I	MSB – 4 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
$V_{DD(DVO)}$	F4	S	digital supply voltage for DVO cells
V_{DDId}	F11	S	3.3 V digital supply voltage for core (decoder)
TVD	F12	O	TV detector; hot-plug interrupt pin; HIGH if TV is connected
IGPV	F13	O	multi-purpose vertical reference output with IPD output bus
IGP0	F14	O	general purpose output signal 0 with IPD output bus
FSVGC	G1	I/O	frame synchronization output to VGC (optional input)
SDAe	G2	I/O	serial data input/output (I^2C-bus encoder)
$\overline{CBO}$	G3	O	composite blanking output to VGC; active LOW
PIXCLKO	G4	O	pixel clock output to VGC
V_{DDEd}	G11	S	3.3 V digital supply voltage for peripheral cells (decoder)
IGPH	G12	O	multi-purpose horizontal reference output with IPD output bus
IGP1	G13	O	general purpose output signal 1 with IPD output bus
ITRI	G14	I(/O)	programmable control signals for IPD output bus
PD2	H1	I	MSB – 5 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD1	H2	I	MSB – 6 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
PD0	H3	I	MSB – 7 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Table 12 to Table 18 for pin assignment
V_{SSEd}	H4	S	digital ground for peripheral cells (decoder)
V_{SSEd}	H11	S	digital ground for peripheral cells (decoder)
ICLK	H12	I/O	clock for IPD output bus (optional clock input)
TEST0	H13	O	scan test output; do not connect
IDQ	H14	O	data qualifier for IPD output bus
TEST4	J1	O	scan test output; do not connect
TEST5	J2	I	scan test input; do not connect
TEST3	J3	I	scan test input; do not connect
V_{DDId}	J4	S	3.3 V digital supply voltage for core (decoder)
V_{DDId}	J11	S	3.3 V digital supply voltage for core (decoder)
AMXCLK	J12	I	audio master external clock input
ALRCLK	J13	(I/)O	audio left/right clock output; can be strapped[5][6] to supply via a 3.3 kΩ resistor to indicate that the default 24.576 MHz crystal (pin ALRCLK = LOW; internal pull-down) has been replaced by a 32.110 MHz crystal (pin ALRCLK = HIGH)
ITRDY	J14	I	target ready input for IPD output bus
XTRI	K1	I	control signal for all X port pins
XPD7	K2	I/O	MSB of XPD bus
XPD6	K3	I/O	MSB – 1 of XPD bus
V_{SSId}	K4	S	digital ground core (decoder)
V_{SSId}	K11	S	digital ground core (decoder)
AMCLK	K12	O	audio master clock output, must be less than 50 % of crystal clock

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
RTS0	K13	O	real-time status or sync information line 0
ASCLK	K14	O	audio serial clock output
XPD5	L1	I/O	MSB – 2 of XPD bus
XPD4	L2	I/O	MSB – 3 of XPD bus
XPD3	L3	I/O	MSB – 4 of XPD bus
V_{DDId}	L4	S	3.3 V digital supply voltage for core (decoder)
XRV	L5	I/O	vertical reference for XPD bus
V_{SSEd}	L6	S	digital ground for peripheral cells (decoder)
V_{DDEd}	L7	S	3.3 V digital supply voltage for peripheral cells (decoder)
V_{DDXd}	L8	S	3.3 V supply voltage for oscillator (decoder)
V_{DDEd}	L9	S	3.3 V digital supply voltage for peripheral cells (decoder)
RTS1	L10	O	real-time status or sync information line 1
V_{DDId}	L11	S	3.3 V digital supply voltage for core (decoder)
SDAd	L12	I/O	serial data input/output (I^2C-bus decoder)
RTCO	L13	(I/)O	real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see external document *"How to use Real Time Control (RTC)"*, available on request); the RTCO pin[5][7] is enabled via I^2C-bus bit RTCE; see Table 162
LLC2	L14	O	line-locked ½ clock output (13.5 MHz nominal)
XPD2	M1	I/O	MSB – 5 of XPD bus
XPD1	M2	I/O	MSB – 6 of XPD bus
XCLK	M3	I/O	clock for XPD bus
XDQ	M4	I/O	data qualifier for XPD bus
TMSd	M5	I/pu	test mode select input for BST (decoder)[4]
TCKd	M6	I/pu	test clock input for BST (decoder)[4]
V_{SSAd}	M7	S	analog ground (decoder)
V_{DDAd}	M8	S	3.3 V analog supply voltage (decoder)
V_{DDAd}	M9	S	3.3 V analog supply voltage (decoder)
AOUT	M10	O	do not connect; analog test output
SCLd	M11	I(/O)	serial clock input (I^2C-bus decoder) with inactive output path
$\overline{RESd}$	M12	O	reset output signal; active LOW (decoder)
V_{SSEd}	M13	S	digital ground for peripheral cells (decoder)
LLC	M14	O	line-locked clock output (27 MHz nominal)
XPD0	N1	I/O	MSB – 7 of XPD bus
XRH	N2	I/O	horizontal reference for XPD bus
XRDY	N3	O	data input ready for XPD bus
$\overline{TRSTd}$	N4	I/pu	test reset input for BST (decoder); active LOW; with internal pull-up[2][3]
TDOd	N5	O	test data output for BST (decoder)[4]
TDId	N6	I/pu	test data input for BST (decoder)[4]
V_{SSAd}	N7	S	analog ground (decoder)
V_{SSAd}	N8	S	analog ground (decoder)

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
V_{SSAd}	N9	S	analog ground (decoder)
AGND	N10	S	analog ground (decoder) connected to substrate
V_{DDAd}	N11	S	3.3 V analog supply voltage (decoder)
V_{SSAd}	N12	S	analog ground (decoder)
V_{SSAd}	N13	S	analog ground (decoder)
CE	N14	I	chip enable or reset input (with internal pull-up)
XTALId	P2	I	27 MHz crystal input (decoder)
XTALOd	P3	O	27 MHz crystal output (decoder)
XTOUTd	P4	O	crystal oscillator output signal (decoder); auxiliary signal
V_{SSXd}	P5	S	ground for crystal oscillator (decoder)
AI24	P6	I	analog input 24
AI23	P7	I	analog input 23
AI2D	P8	I	differential analog input for channel 2; connect to ground via a capacitor
AI22	P9	I	analog input 22
AI21	P10	I	analog input 21
AI12	P11	I	analog input 12
AI1D	P12	I	differential analog input for channel 1; connect to ground via a capacitor
AI11	P13	I	analog input 11

[1] Pin type: I = input, O = output, S = supply, pu = pull-up.

[2] For board design without boundary scan implementation connect $\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$ to ground.

[3] This pin provides easy initialization of the Boundary Scan Test (BST) circuit. $\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

[4] In accordance with the *"IEEE1149.1"* standard the pins TDIe (TDId), TMSe (TMSd), TCKe (TCKd) and $\overline{\text{TRSTe}}$ ($\overline{\text{TRSTd}}$) are input pins with an internal pull-up resistor and TDOe (TDOd) is a 3-state output pin.

[5] Pin strapping is done by connecting the pin to supply via a 3.3 kΩ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull-down).

[6] Pin ALRCLK = LOW for 24.576 MHz crystal (default); pin ALRCLK = HIGH for 32.110 MHz crystal.

[7] Pin RTCO operates as I^2C-bus slave address pin; pin RTCO = LOW for slave address 42h/43h (default); pin RTCO = HIGH for slave address 40h/41h.

8. Functional description of digital video encoder part

The digital video encoder part encodes digital luminance and color difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7108AE; SAA7109AE can be directly connected to a PC video graphics controller with a maximum resolution of 1280 × 1024 (progressive) or 1920 × 1080 (interlaced) at a 50 Hz or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Table 12 to Table 18.

A complete 3 bytes × 256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port Pixel Data (PD) or via the I²C-bus.

The SAA7108AE; SAA7109AE supports a 32-bit × 32-bit × 2-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I²C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7108AE; SAA7109AE can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, color modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/color difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *'RS-170-A'* and *'ITU-R BT.470-3'*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figure 6 to Figure 11. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *'ITU-R BT.656'* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in Slave mode. For assignment of the input data to the rising or falling clock edge see Table 12 to Table 18.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7108AE; SAA7109AE synthesizes all necessary internal signals, color subcarrier frequency and synchronization signals from that clock.

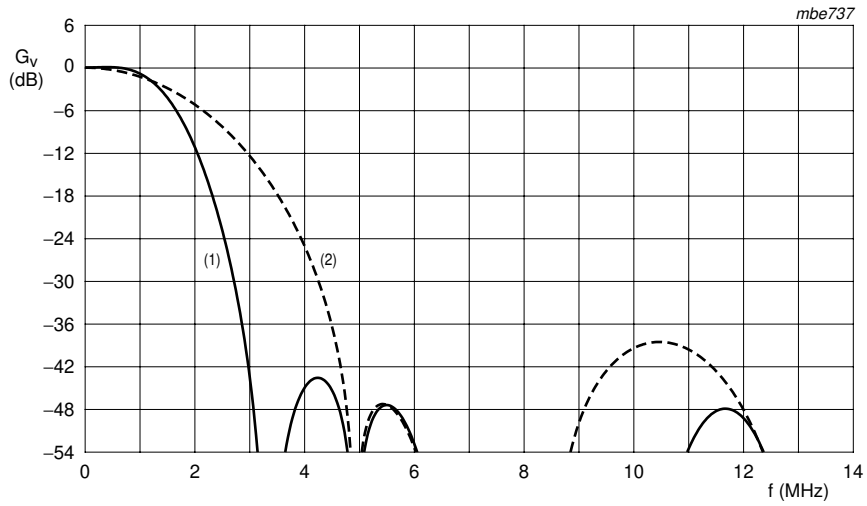
Wide screen signalling data can be loaded via the I²C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I²C-bus.

The IC also contains closed caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Figure 66). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

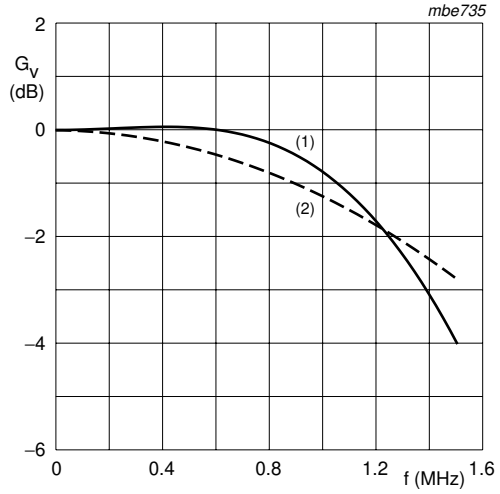
- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude etc.



(1) SCBW = 1.

(2) SCBW = 0.

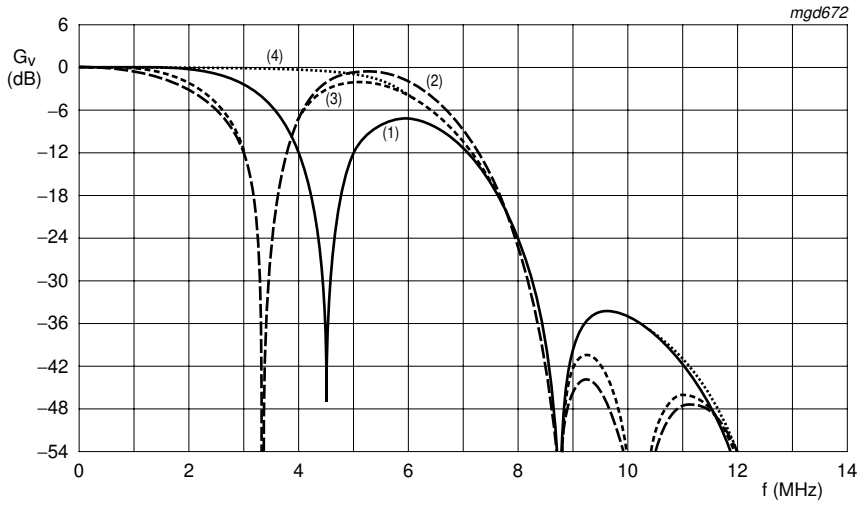
Fig 6. Chrominance transfer characteristic



(1) SCBW = 1.

(2) SCBW = 0.

Fig 7. Chrominance transfer characteristic (enlargement of Figure 6)



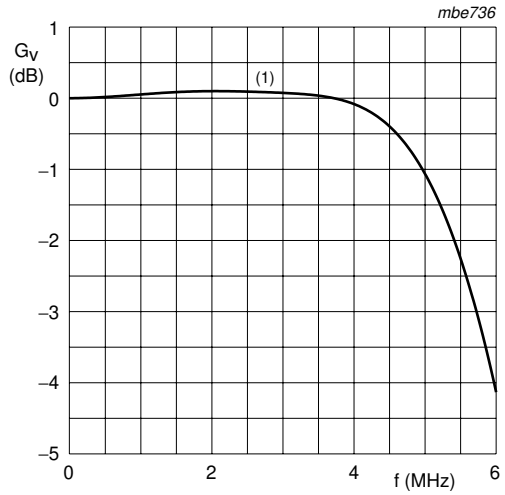
(1) CCRS[1:0] = 01.

(2) CCRS[1:0] = 10.

(3) CCRS[1:0] = 11.

(4) CCRS[1:0] = 00.

Fig 8. Luminance transfer characteristic (excluding scaler)



(1) CCRS[1:0] = 00.

Fig 9. Luminance transfer characteristic (excluding scaler) (enlargement of Figure 8)

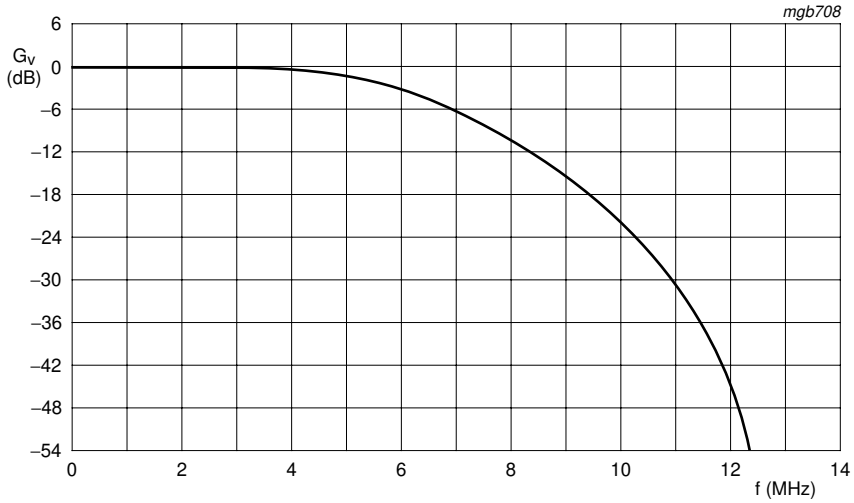


Fig 10. Luminance transfer characteristic in RGB (excluding scaler)

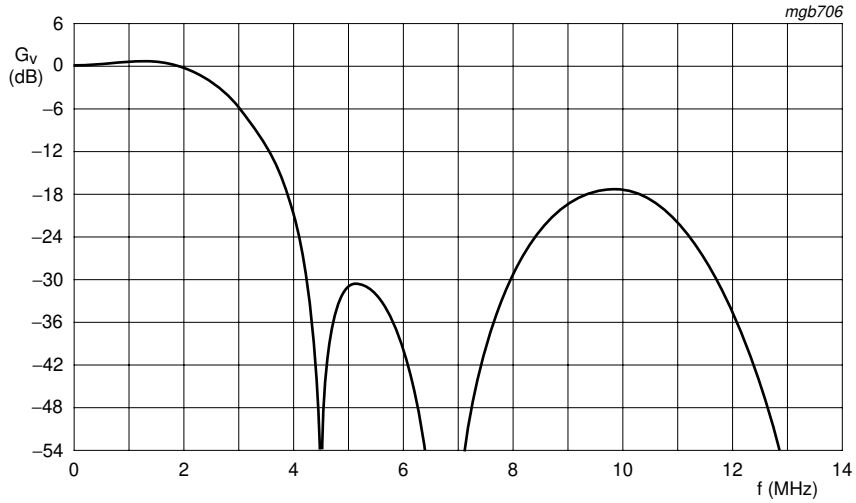


Fig 11. Color difference transfer characteristic in RGB (excluding scaler)

8.1 Reset conditions

To activate the reset, a pulse of at least 2 crystal clocks duration is required.

During reset ($\overline{\text{RES}}$e = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{\text{CBO}}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I²C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I²C-bus access redefines the corresponding registers; see Table 5.

Table 5. Strapping pins

Pin	Tied	Preset
FSVGC (pin G1)	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC (pin F1)	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{\text{CBO}}$ (pin G3)	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC (pin E3)	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2 (pin C4)	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal color bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

8.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I²C-bus control bits SLOT and EDGE for correct operation.

If Y-C_B-C_R is being applied as a 27 MB/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

The horizontal upscaling is supported via the input formatter. According to the programming of the pixel clock dividers (see Section 8.10), it will sample up the data stream to 1 ×, 2 × or 4 × the input data rate. An optional interpolation filter is available. The clock domain transition is handled by a 4 entries wide FIFO which gets initialized every field or explicitly at request. A bypass for the FIFO is available, especially for high input data rates.

8.3 RGB LUT

The three 256-byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed color data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I²C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 bytes × 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

8.4 Cursor insertion

A 32 dots × 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I²C-bus write access to specific registers or in the pixel data input through the PD port. In the latter case, the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I²C-bus register as described in Table 8. Transparent means that the input pixels are passed through, the ‘cursor colors’ can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 6. Layout of a byte in the cursor bit map

D7		D6		D5		D4		D3		D2		D1		D0	
pixel n + 3				pixel n + 2				pixel n + 1				pixel n			
D1		D0		D1		D0		D1		D0		D1		D0	

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the 'hot spot', the other register controls the insertion position. The hot spot is the 'tip' of the pointer arrow. It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border, this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 7. Cursor bit map

Byte	D7 D6	D5 D4	D3 D2	D1 D0
0	row 0 column 3	row 0 column 2	row 0 column 1	row 0 column 0
1	row 0 column 7	row 0 column 6	row 0 column 5	row 0 column 4
2	row 0 column 11	row 0 column 10	row 0 column 9	row 0 column 8
...	...	...	...	...
6	row 0 column 27	row 0 column 26	row 0 column 25	row 0 column 24
7	row 0 column 31	row 0 column 30	row 0 column 29	row 0 column 28
...	...	...	...	...
254	row 31 column 27	row 31 column 26	row 31 column 25	row 31 column 24
255	row 31 column 31	row 31 column 30	row 31 column 29	row 31 column 28

Table 8. Cursor modes

Cursor pattern	Cursor mode	
	CMODE = 0	CMODE = 1
00	second cursor color	second cursor color
01	first cursor color	first cursor color
10	transparent	transparent
11	inverted input	auxiliary cursor color

8.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R color space in this block. The color difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

A gain adjust option corrects the level swing of the graphics world (black-to-white as 0 to 255) to the required range of 16 to 235.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

8.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the color phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7108AE; SAA7109AE input data is in accordance with *'ITU-R BT.656'*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

8.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 107.

An additional, programmable vertical filter supports the anti-flicker function. This filter is not available at upscaling factors of more than 2.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

Due to the re-interlacing, the circuit can perform upscaling by a maximum factor of 2. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 8.20.

An additional upscaling mode allows to increase the upscaling factor to maximum 4 as it is required for the old VGA modes like 320 $\times$ 240.

8.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I^2C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor.

8.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true color tint.

8.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I^2C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 40 MHz and 85 MHz. Two programmable dividers provide the actual clock to be used externally and internally. The dividers can be programmed to factors of 1, 2, 4 and 8. For the internal pixel clock, a divider ratio of 8 makes no sense and is thus forbidden.

The internal clock can be switched completely to the pixel clock input. In this event, the input FIFO is useless and will be bypassed.

The entire pixel clock generation can be locked to the vertical frequency. Both pixel clock dividers get re-initialized every field. Optionally, the DTO can be cleared with each V-sync. At proper programming, this will make the pixel clock frequency a precise multiple of the vertical and horizontal frequencies. This is required for some graphic controllers.

8.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

8.12 Encoder

8.12.1 Video path

The encoder generates luminance and color subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7108AE only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figure 8 and Figure 9. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher color bandwidth, which can be used for the Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figure 6 and Figure 7.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, color is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

8.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Figure 66.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

8.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

8.12.4 Closed caption encoder

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

8.12.5 Anti-taping (SAA7108AE only)

For more information contact your nearest NXP Semiconductors sales office.