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DATA SHEET

SAA7108E; SAA7109E
PC-CODEC

Product specification
2004 Mar 16
Supersedes data of 2001 Dec 12

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

1.1 Video decoder

- Six analog inputs, internal analog source selectors, e.g. 6 × CVBS or (2 × Y/C and 2 × CVBS) or (1 × Y/C and 4 × CVBS)
- Two analog preprocessing channels in differential CMOS style for best S/N-performance
- Fully programmable static gain or Automatic Gain Control (AGC) for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 9-bit video CMOS Analog-To-Digital Converters (ADCs), digitized CVBS or Y/C signals are available on the IPD (Image Port Data) port under I²C-bus control
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal sync processing and clock generation, horizontal and vertical sync detection
- Requires only one crystal (either 24.576 MHz or 32.11 MHz) for all standards
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, combination PAL N, PAL M, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Brightness Contrast Saturation (BCS) and hue control on-chip
- Two multi functional real-time output pins controlled by I²C-bus
- Multi-standard VBI data slicer decoding World Standard Teletext (WST), North-American Broadcast Text System (NABTS), Closed Caption (CC), Wide Screen Signalling (WSS), Video Programming System (VPS), Vertical Interval Time Code (VITC) variants (EBU/SMPTE) etc.
- Standard ITU 656 Y-C_B-C_R 4 : 2 : 2 format (8-bit) on IPD output bus
- Enhanced ITU 656 output format on IPD output bus containing:
  - active video
  - raw CVBS data for INTERCAST applications (27 MHz data rate)
  - decoded VBI data
- Detection of copy protected input signals according to the macrovision standard. Can be used to prevent unauthorized recording of pay-TV or video tape signals.

1.2 Video scaler

- Both up and downscaling
- Conversion to square pixel format
- NTSC to 288 lines (video phone)
- Phase accuracy better than $^1/_{64}$ pixel or line, horizontally or vertically
- Independent scaling definitions for odd and even fields
- Anti-alias filter for horizontal scaling
- Provides output as
  - scaled active video
  - raw CVBS data for INTERCAST, WAVE-PHORE, POPCON applications or general VBI data decoding (27 MHz or sample rate converted)
- Local video output for Y-C_B-C_R 4 : 2 : 2 format (VMI, VIP, ZV).

1.3 Video encoder

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 45 MHz at double edged clocking, synthesized on-chip or from external source
- Up to 800 × 600 graphics data at 60 Hz or 50 Hz with programmable underscan range
- Three Digital-to-Analog Converters (DACs) at 27 MHz sample rate for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) (signals in parenthesis are optional); all at 10-bit resolution

- Selectable cross-colour reduction to improve CVBS output
- Non-interlaced C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling
- Downscaling from 1 : 1 to 1 : 2 and up to 20% upscaling
- Optional interlaced C_B-Y-C_R input Digital Versatile Disk (DVD)
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode, maximum 45 MHz)
- 3×256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- Programmable border colour of underscan area
- On-chip 27 MHz crystal oscillator (3rd-harmonic or fundamental 27 MHz crystal)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Optional support of various VBI data insertion as
  - WST-625, WSS, VPS
  - WST-525, NABTS
  - Closed Caption, Copy Generation Management System (CGMS)
- Macrovision Pay-per-View copy protection system rev. 7.01 and rev. 6.1 as option; this applies to SAA7108E only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.

1.4 Common features

- 5 V tolerant digital I/O ports
- I^2C-bus controlled (full read-back ability by an external controller, bit rate up to 400 kbits/s)
- Versatile power-save modes
- Boundary scan test circuit complies with the *"IEEE Std. 1149.b1-1994"* (separate ID codes for decoder and encoder)
- Monolithic CMOS 3.3 V device
- BGA156 package
- Moisture Sensitive Level (MSL): e3.

2 APPLICATIONS

- Notebook (low-power consumption)
- PCMCIA card application
- AGP based graphics cards
- PC editing
- Image processing
- Video phone applications
- INTERCAST and PC teletext applications
- Security applications
- Hybrid satellite set-top boxes.

3 GENERAL DESCRIPTION

The SAA7108E; SAA7109E is a new multi-standard video decoder and encoder chip, offering high quality video input and TV output processing as required by PC-99 specifications. It enables hardware manufacturers to implement versatile video functions on a significantly reduced printed-circuit board area at very competitive costs.

Separate pins for supply voltages as well as for I^2C-bus control and boundary scan test have been provided for the video encoder and decoder sections to ensure both flexible handling and optimized noise behaviour.

The **video encoder** is used to encode PC graphics data at maximum 800 × 600 resolution to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and interlacer ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 800 × 600 resolution/60 Hz (PIXCLK < 45 MHz).

The **video decoder**, a 9-bit video input processor, is a combination of a 2-channel analog pre-processing circuit including source selection, anti-aliasing filter and Analog-to-Digital Converter (ADC), automatic clamp and gain control, a Clock Generation Circuit (CGC), and a digital multi-standard decoder (PAL BGHI, PAL M, PAL N, combination PAL N, NTSC M, NTSC-Japan, NTSC N, NTSC 4.43 and SECAM).

The decoder includes a brightness, contrast and saturation control circuit, a multi-standard VBI data slicer and a 27 MHz VBI data bypass. The pure 3.3 V (5 V compatible) CMOS circuit SAA7108E; SAA7109E, consisting of an analog front-end and digital video decoder, a digital video encoder and analog back-end, is a highly integrated circuit especially designed for desktop video applications.

The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU-R BT.601 compatible colour component values.

The encoder can operate fully independently at its own variable pixel clock, transporting graphics input data, and at the line-locked, single crystal-stable video encoding clock.

As an option, it is possible to slave the video PAL/NTSC encoding to the video decoder clock with the encoder FIFO acting as a buffer to decouple the line-locked decoder clock from the crystal-stable encoder clock.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
T_{amb}	ambient temperature		0	–	70	°C
P_{A+D}	analog and digital power dissipation	note 1	–	–	1.4	W

Note

1. Power dissipation is extremely dependent on programming and selected application.

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7108E	BGA156	plastic ball grid array package; 156 balls; body 15 × 15 × 1.15 mm	SOT472-1
SAA7109E			

6 BLOCK DIAGRAMS

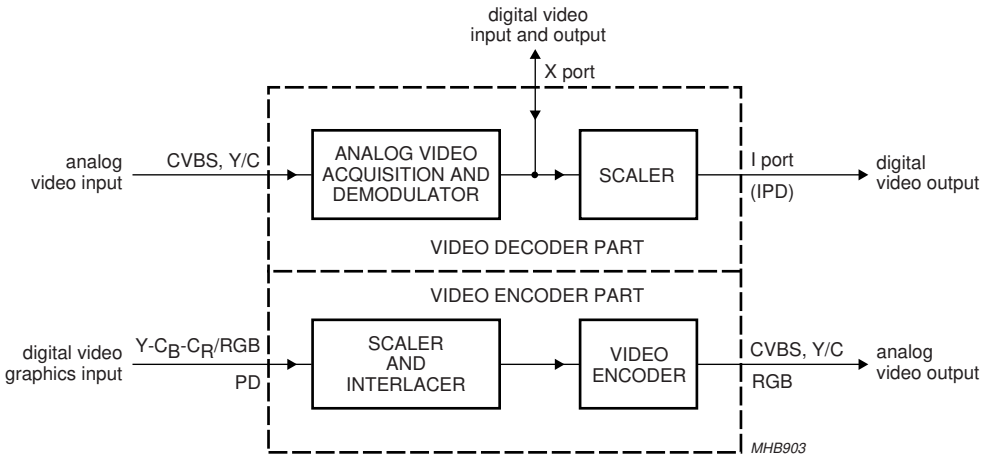


Fig.1 Simplified block diagram.

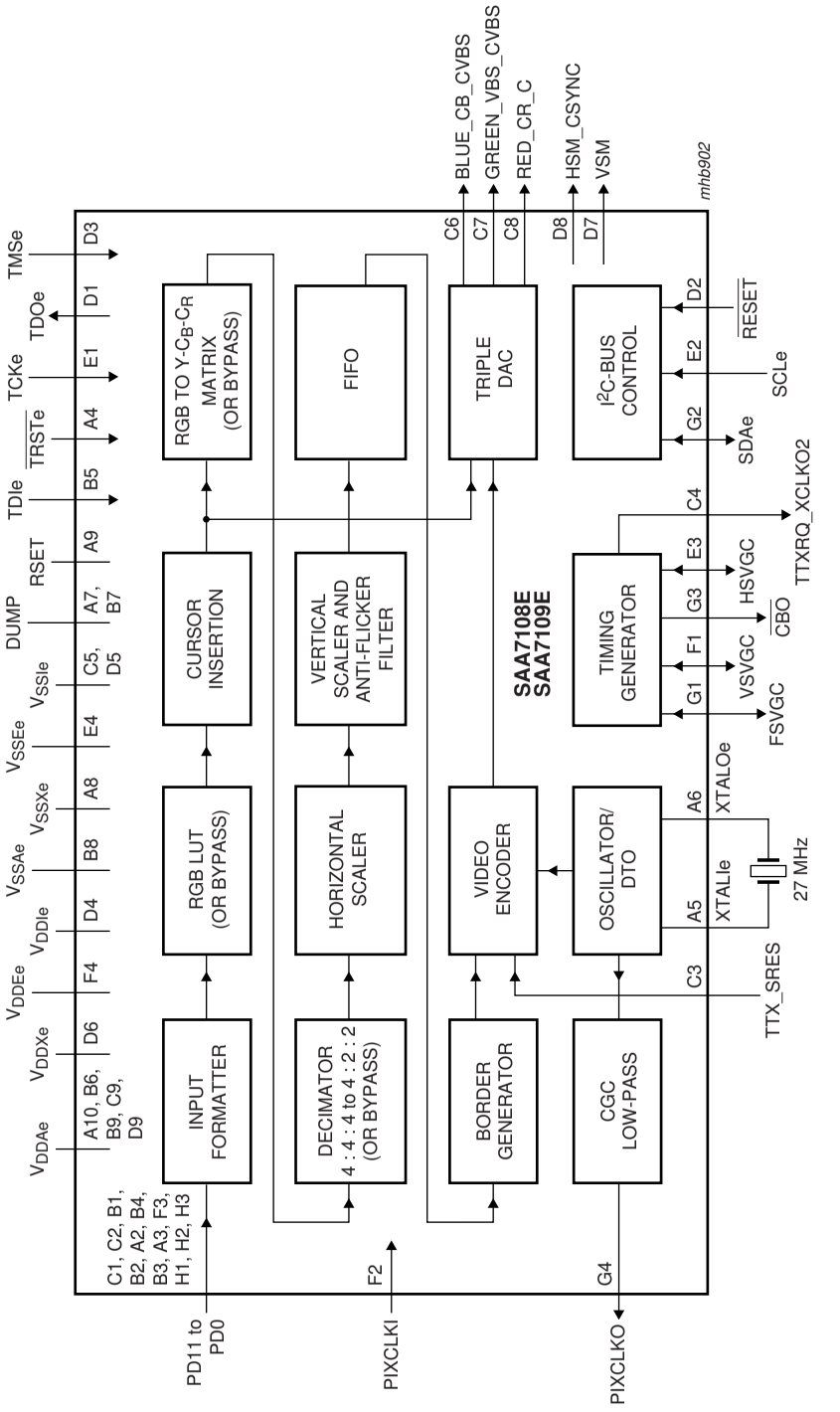


Fig.2 Block diagram (video encoder part).

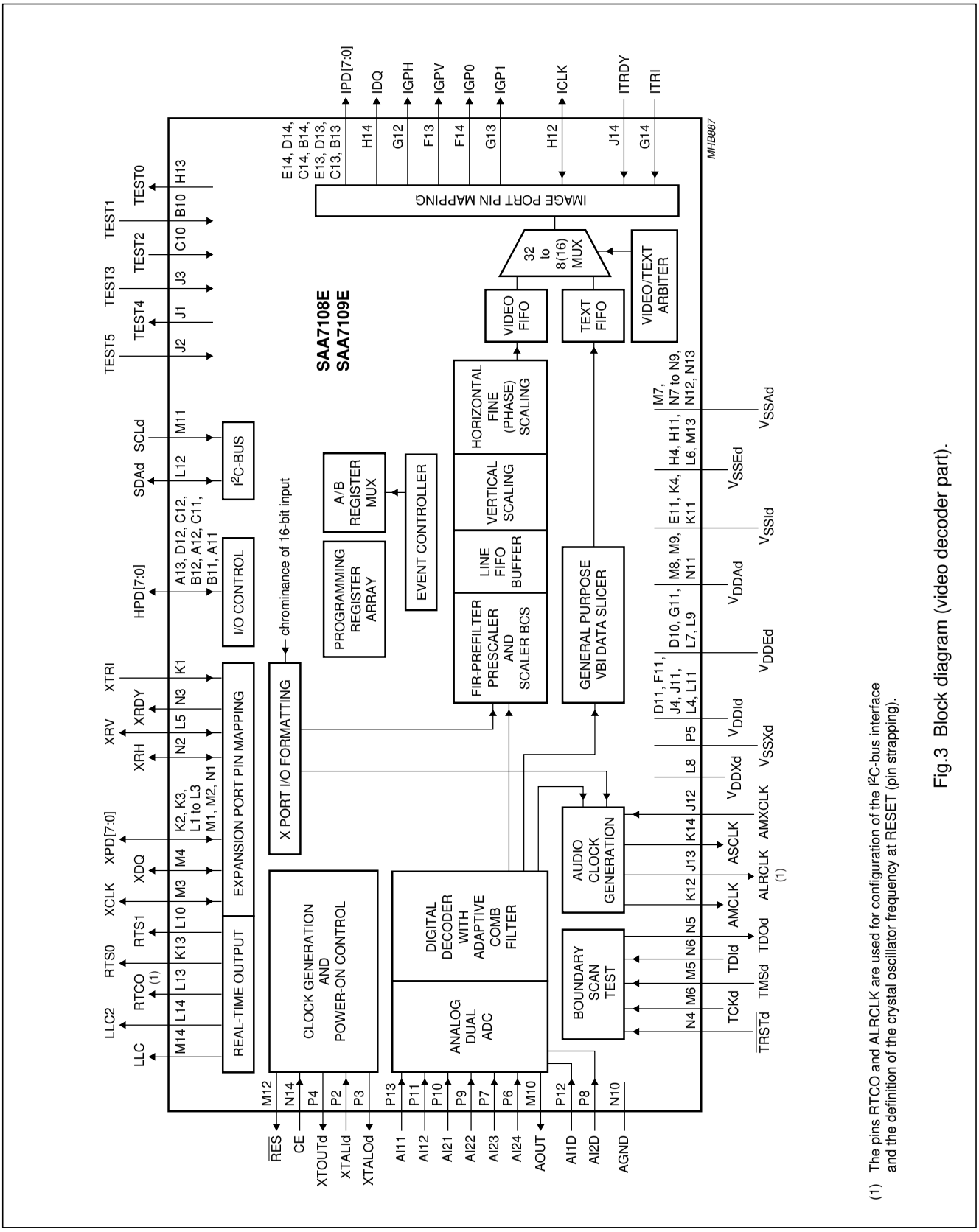


Fig.3 Block diagram (video decoder part).

(1) The pins RTCO and ALRCLK are used for configuration of the I²C-bus interface and the definition of the crystal oscillator frequency at RESET (pin strapping).

7 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
PD7	A2	I	MSB of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
PD4	A3	I	MSB – 3 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
$\overline{\text{TRSTe}}$	A4	I/pu	test reset input for Boundary Scan Test (BST) (encoder); active LOW; with internal pull-up; notes 2 and 3
XTALIe	A5	I	27 MHz crystal input (encoder)
XTALOe	A6	O	27 MHz crystal output (encoder)
DUMP	A7	O	DAC reference pin (encoder), 12 Ω resistor connected to V_{SSAe}
V_{SSXe}	A8	S	ground for oscillator (encoder)
RSET	A9	O	DAC reference pin (encoder), 1 kΩ resistor connected to V_{SSAe}
V_{DDAe}	A10	S	3.3 V analog supply voltage (encoder)
HPD0	A11	I/O	MSB – 7 of Host Port Data (HPD) output bus
HPD3	A12	I/O	MSB – 4 of HPD output bus
HPD7	A13	I/O	MSB of HPD output bus
PD9	B1	I	see Tables 25, 30 and 31 for pin assignment with different encoder input formats
PD8	B2	I	see Tables 25, 30 and 31 for pin assignment with different encoder input formats
PD5	B3	I	MSB – 2 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
PD6	B4	I	MSB – 1 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
TDIe	B5	I/pu	test data input for BST (encoder); note 4
V_{DDAe}	B6	S	3.3 V analog supply voltage (encoder)
DUMP	B7	O	DAC reference pin (encoder); connected to A7
V_{SSAe}	B8	S	analog ground (encoder)
V_{DDAe}	B9	S	3.3 V analog supply voltage (encoder)
TEST1	B10	I	scan test input 1, do not connect
HPD1	B11	I/O	MSB – 6 of HPD output bus
HPD4	B12	I/O	MSB – 3 of HPD output bus
IPD0	B13	O	MSB – 7 of IPD output bus
IPD4	B14	O	MSB – 3 of Image Port Data (IPD) output bus
PD11	C1	I	see Tables 25, 30 and 31 for pin assignment with different encoder input formats
PD10	C2	I	see Tables 25, 30 and 31 for pin assignment with different encoder input formats
TTX_SRES	C3	I	teletext input or sync reset input (encoder)
TTXRQ_XCLKO2	C4	O	teletext request output or 13.5 MHz clock output of the crystal oscillator (encoder)
V_{SSIe}	C5	S	digital ground core (encoder)
BLUE_CB_CVBS	C6	O	BLUE or C_B or CVBS output

SYMBOL	PIN	TYPE[1]	DESCRIPTION
GREEN_VBS_CVBS	C7	O	GREEN or VBS or CVBS output
RED_CR_C	C8	O	RED or C_R or C output
V_{DDAe}	C9	S	3.3 V analog supply voltage (encoder)
TEST2	C10	I	scan test input 2, do not connect
HPD2	C11	I/O	MSB – 5 of HPD output bus
HPD5	C12	I/O	MSB – 2 of HPD output bus
IPD1	C13	O	MSB – 6 of IPD output bus
IPD5	C14	O	MSB – 2 of IPD output bus
TDOe	D1	O	test data output for BST (encoder); note 4
$\overline{\text{RESET}}$	D2	I	reset input (encoder); active LOW
TMSe	D3	I/pu	test mode select input for BST (encoder); note 4
V_{DDIe}	D4	S	3.3 V digital supply voltage for core (encoder)
V_{SSIe}	D5	S	digital ground core (encoder)
V_{DDXe}	D6	S	3.3 V supply voltage for oscillator (encoder)
VSM	D7	O	vertical synchronization output to VGA monitor (non-interlaced)
HSM_CSYNC	D8	O	horizontal synchronization output to VGA monitor (non-interlaced) or composite sync for RGB-SCART
V_{DDAe}	D9	S	3.3 V analog supply voltage (encoder)
V_{DDEd}	D10	S	3.3 V digital supply voltage for peripheral cells (decoder)
V_{DDId}	D11	S	3.3 V digital supply voltage for core (decoder)
HPD6	D12	I/O	MSB – 1 of HPD output bus
IPD2	D13	O	MSB – 5 of IPD output bus
IPD6	D14	O	MSB – 1 of IPD output bus
TCKe	E1	I/pu	test clock input for BST (encoder); note 4
SCLe	E2	I	I^2C-bus serial clock input (encoder)
HSVGC	E3	I/O	horizontal synchronization output to Video Graphics Controller (VGC) (optional input)
V_{SSEe}	E4	S	digital ground peripheral cells (encoder)
V_{SSId}	E11	S	digital ground core (decoder)
n.c.	E12	–	not connected
IPD3	E13	O	MSB – 4 of IPD output bus
IPD7	E14	O	MSB of IPD output bus
VSVGC	F1	I/O	vertical synchronization output to VGC (optional input)
PIXCLKI	F2	I	pixel clock input (looped through)
PD3	F3	I	MSB – 4 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
V_{DDEe}	F4	S	3.3 V digital supply voltage for peripheral cells (encoder)
V_{DDId}	F11	S	3.3 V digital supply voltage for core (decoder)
n.c.	F12	–	not connected
IGPV	F13	O	multi-purpose vertical reference output with IPD output bus
IGP0	F14	O	general purpose output signal 0 with IPD output bus

SYMBOL	PIN	TYPE(1)	DESCRIPTION
FSVGC	G1	I/O	frame synchronization output to VGC (optional input)
SDAe	G2	I/O	I^2C-bus serial data input/output (encoder)
$\overline{CBO}$	G3	O	composite blanking output to VGC; active LOW
PIXCLKO	G4	O	pixel clock output to VGC
V_{DDEd}	G11	S	3.3 V digital supply voltage for peripheral cells (decoder)
IGPH	G12	O	multi-purpose horizontal reference output with IPD output bus
IGP1	G13	O	general purpose output signal 1 with IPD output bus
ITRI	G14	I/(O)	programmable control signals for IPD output bus
PD2	H1	I	MSB – 5 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
PD1	H2	I	MSB – 6 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
PD0	H3	I	MSB – 7 of encoder input bus with C_B-Y-C_R 4 : 2 : 2; see Tables 25 to 31 for pin assignment
V_{SSEd}	H4	S	digital ground for peripheral cells (decoder)
V_{SSEd}	H11	S	digital ground for peripheral cells (decoder)
ICLK	H12	I/O	clock for IPD output bus (optional clock input)
TEST0	H13	O	scan test output, do not connect
IDQ	H14	O	data qualifier for IPD output bus
TEST4	J1	O	scan test output, do not connect
TEST5	J2	I	scan test input, do not connect
TEST3	J3	I	scan test input, do not connect
V_{DDId}	J4	S	3.3 V digital supply voltage for core (decoder)
V_{DDId}	J11	S	3.3 V digital supply voltage for core (decoder)
AMXCLK	J12	I	audio master external clock input
ALRCLK	J13	(I/)O	audio left/right clock output; can be strapped to supply via a 3.3 kΩ resistor to indicate that the default 24.576 MHz crystal (ALRCLK = 0; internal pull-down) has been replaced by a 32.110 MHz crystal (ALRCLK = 1); notes 5 and 6
ITRDY	J14	I	target ready input for IPD output bus
XTRI	K1	I	control signal for all X port pins
XPD7	K2	I/O	MSB of XPD bus
XPD6	K3	I/O	MSB – 1 of XPD bus
V_{SSId}	K4	S	digital ground core (decoder)
V_{SSId}	K11	S	digital ground core (decoder)
AMCLK	K12	O	audio master clock output, must be less than 50% of crystal clock
RTS0	K13	O	real-time status or sync information line 0
ASCLK	K14	O	audio serial clock output
XPD5	L1	I/O	MSB – 2 of XPD bus
XPD4	L2	I/O	MSB – 3 of XPD bus
XPD3	L3	I/O	MSB – 4 of XPD bus
V_{DDId}	L4	S	3.3 V digital supply voltage for core (decoder)
XRV	L5	I/O	vertical reference for XPD bus

SYMBOL	PIN	TYPE[1]	DESCRIPTION
V_{SSEd}	L6	S	digital ground for peripheral cells (decoder)
V_{DDEd}	L7	S	3.3 V digital supply voltage for peripheral cells (decoder)
V_{DDXd}	L8	S	3.3 V supply voltage for oscillator (decoder)
V_{DDEd}	L9	S	3.3 V digital supply voltage for peripheral cells (decoder)
RTS1	L10	O	real-time status or sync information line 1
V_{DDId}	L11	S	3.3 V digital supply voltage for core (decoder)
SDAd	L12	I/O	I²C-bus serial data input/output (decoder)
RTCO	L13	(I/)O	real-time control output; contains information about actual system clock frequency, field rate, odd/even sequence, decoder status, subcarrier frequency and phase and PAL sequence (see external document *"RTC Functional Description"*, available on request); the RTCO pin is enabled via I²C-bus bit RTCE; see notes 5 and 7 and Table 146
LLC2	L14	O	line-locked ½ clock output (13.5 MHz nominal)
XPD2	M1	I/O	MSB – 5 of XPD bus
XPD1	M2	I/O	MSB – 6 of XPD bus
XCLK	M3	I/O	clock for XPD bus
XDQ	M4	I/O	data qualifier for XPD bus
TMSd	M5	I/pu	test mode select input for BST (decoder); note 4
TCKd	M6	I/pu	test clock input for BST (decoder); note 4
V_{SSAd}	M7	S	analog ground (decoder)
V_{DDAd}	M8	S	3.3 V analog supply voltage (decoder)
V_{DDAd}	M9	S	3.3 V analog supply voltage (decoder)
AOUT	M10	O	analog test output (do not connect)
SCLd	M11	I	I²C-bus serial clock input (decoder)
$\overline{RES}$	M12	O	reset output signal; active LOW (decoder)
V_{SSEd}	M13	S	digital ground for peripheral cells (decoder)
LLC	M14	O	line-locked clock output (27 MHz nominal)
XPD0	N1	I/O	MSB – 7 of XPD bus
XRH	N2	I/O	horizontal reference for XPD bus
XRDY	N3	O	data input ready for XPD bus
$\overline{TRSTd}$	N4	I/pu	test reset input for BST (decoder); active LOW; with internal pull-up; notes 2 and 3
TDOd	N5	O	test data output for BST (decoder); note 4
TDId	N6	I/pu	test data input for BST (decoder); note 4
V_{SSAd}	N7	S	analog ground (decoder)
V_{SSAd}	N8	S	analog ground (decoder)
V_{SSAd}	N9	S	analog ground (decoder)
AGND	N10	S	analog ground (decoder) connected to substrate
V_{DDAd}	N11	S	3.3 V analog supply voltage (decoder)
V_{SSAd}	N12	S	analog ground (decoder)
V_{SSAd}	N13	S	analog ground (decoder)
CE	N14	I	chip enable or reset input (with internal pull-up)

SYMBOL	PIN	TYPE(1)	DESCRIPTION
XTALId	P2	I	27 MHz crystal input (decoder)
XTALOd	P3	O	27 MHz crystal output (decoder)
XTOUTd	P4	O	crystal oscillator output signal (decoder); auxiliary signal
V_{SSXd}	P5	S	ground for crystal oscillator (decoder)
AI24	P6	I	analog input 24
AI23	P7	I	analog input 23
AI2D	P8	I	differential analog input for channel 2; connect to ground via a capacitor
AI22	P9	I	analog input 22
AI21	P10	I	analog input 21
AI12	P11	I	analog input 12
AI1D	P12	I	differential analog input for channel 1; connect to ground via a capacitor
AI11	P13	I	analog input 11

Notes

1. Pin type: I = input, O = output, S = supply, pu = pull-up.
2. For board design without boundary scan implementation connect $\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$ to ground.
3. This pin provides easy initialization of the Boundary Scan Test (BST) circuit. $\overline{\text{TRSTe}}$ and $\overline{\text{TRSTd}}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.
4. In accordance with the *"IEEE1149.1"* standard the pads TDIe (TDId), TMSe (TMSd), TCKe (TCKd) and $\overline{\text{TRSTe}}$ ($\overline{\text{TRSTd}}$) are input pads with an internal pull-up resistor and TDOe (TDOd) is a 3-state output pad.
5. Pin strapping is done by connecting the pin to supply via a 3.3 kΩ resistor. During the power-up reset sequence the corresponding pins are switched to input mode to read the strapping level. For the default setting no strapping resistor is necessary (internal pull-down).
6. Pin ALRCLK: 0 = 24.576 MHz crystal (default); 1 = 32.110 MHz crystal.
7. Pin RTCO: operates as I^2C-bus slave address pin; RTCO = 0 slave address 42H/43H (default); RTCO = 1 slave address 40H/41H.

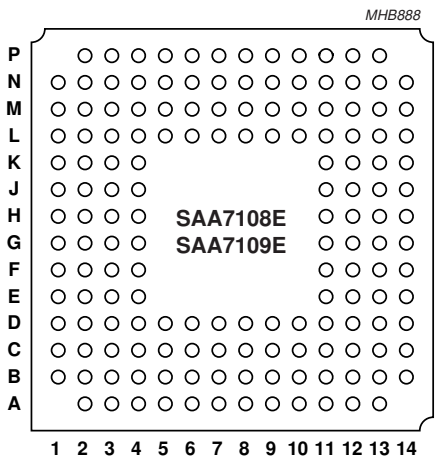


Fig.4 Pin configuration.

Table 1 Pin assignment (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		PD7	PD4	$\overline{\text{TRSTe}}$	XTALIe	XTALOe	DUMP	V_{SSXe}	RSET	V_{DDAe}	HPD0	HPD3	HPD7	
B	PD9	PD8	PD5	PD6	TDIe	V_{DDAe}	DUMP	V_{SSAe}	V_{DDAe}	TEST1	HPD1	HPD4	IPD0	IPD4
C	PD11	PD10	TTX_ SRES	TTXRQ_ XCLKO2	V_{SSIe}	BLUE_ CB_CVBS	GREEN_ VBS_CVBS	RED_CR_C	V_{DDAe}	TEST2	HPD2	HPD5	IPD1	IPD5
D	TDOe	$\overline{\text{RESET}}$	TMSe	V_{DDIe}	V_{SSIe}	V_{DDXe}	VSM	HSM_CSYNC	V_{DDAe}	V_{DDEd}	V_{DDId}	HPD6	IPD2	IPD6
E	TCKe	SCLe	HSVGC	V_{SSEe}							V_{SSId}	n.c.	IPD3	IPD7
F	VSVGC	PIXCLKI	PD3	V_{DDEe}							V_{DDId}	n.c.	IGPV	IGP0
G	FSVGC	SDAe	$\overline{\text{CBO}}$	PIXCLKO							V_{DDEd}	IGPH	IGP1	ITRI
H	PD2	PD1	PD0	V_{SSEd}							V_{SSEd}	ICLK	TEST0	IDQ
J	TEST4	TEST5	TEST3	V_{DDId}							V_{DDId}	AMXCLK	ALRCLK	ITRDY
K	XTRI	XPD7	XPD6	V_{SSId}							V_{SSId}	AMCLK	RTS0	ASCLK
L	XPD5	XPD4	XPD3	V_{DDId}	XRV	V_{SSEd}	V_{DDEd}	V_{DDXd}	V_{DDEd}	RTS1	V_{DDId}	SDAd	RTCO	LLC2
M	XPD2	XPD1	XCLK	XDQ	TMSd	TCKd	V_{SSAd}	V_{DDAd}	V_{DDAd}	AOUT	SCLd	$\overline{\text{RES}}$	V_{SSEd}	LLC
N	XPD0	XRH	XRDY	$\overline{\text{TRSTd}}$	TDOd	TDId	V_{SSAd}	V_{SSAd}	V_{SSAd}	AGND	V_{DDAd}	V_{SSAd}	V_{SSAd}	CE
P		XTALId	XTALOd	XTOUTd	V_{SSXd}	AI24	AI23	AI2D	AI22	AI21	AI12	AI1D	AI11	

8 FUNCTIONAL DESCRIPTION OF DIGITAL VIDEO ENCODER PART

The digital video encoder encodes digital luminance and colour difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7108E; SAA7109E can be directly connected to a PC video graphics controller with a maximum resolution of 800×600 at a 50 or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Tables 25 to 31.

A complete 3×256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port PD (Pixel Data) or via the I^{2}C-bus.

The SAA7108E; SAA7109E supports a $32 \times 32 \times 2$-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I^{2}C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7108E; SAA7109E can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/colour difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"ITU-R BT.470-3"*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figs 5 to 10. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *"ITU-R BT.656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in slave mode. For assignment of the input data to the rising or falling clock edge see Tables 25 to 31.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7108E; SAA7109E synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.

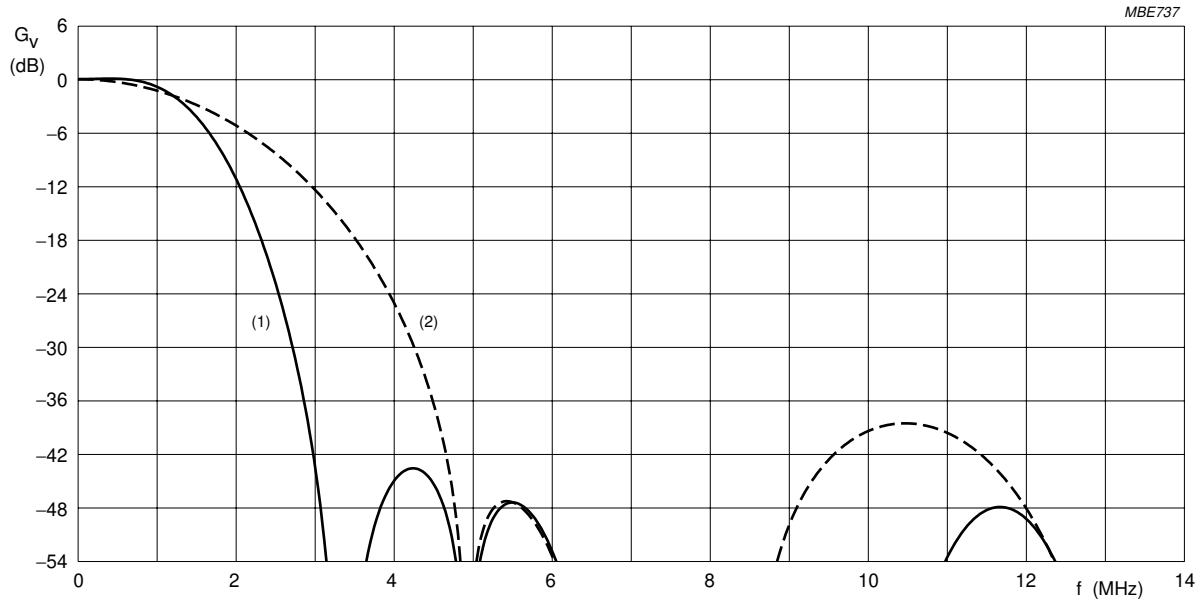
Wide screen signalling data can be loaded via the I^{2}C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I^{2}C-bus.

The IC also contains Closed Caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Fig.50). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

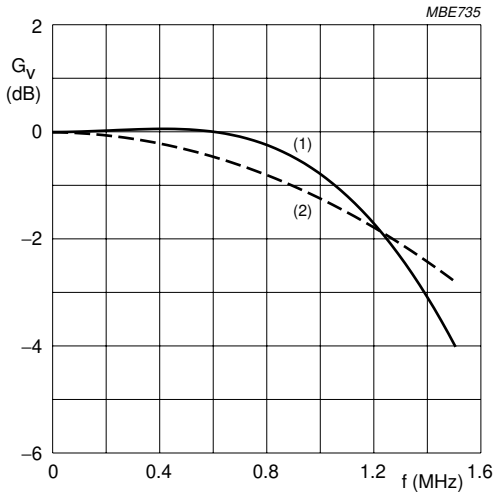
A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.



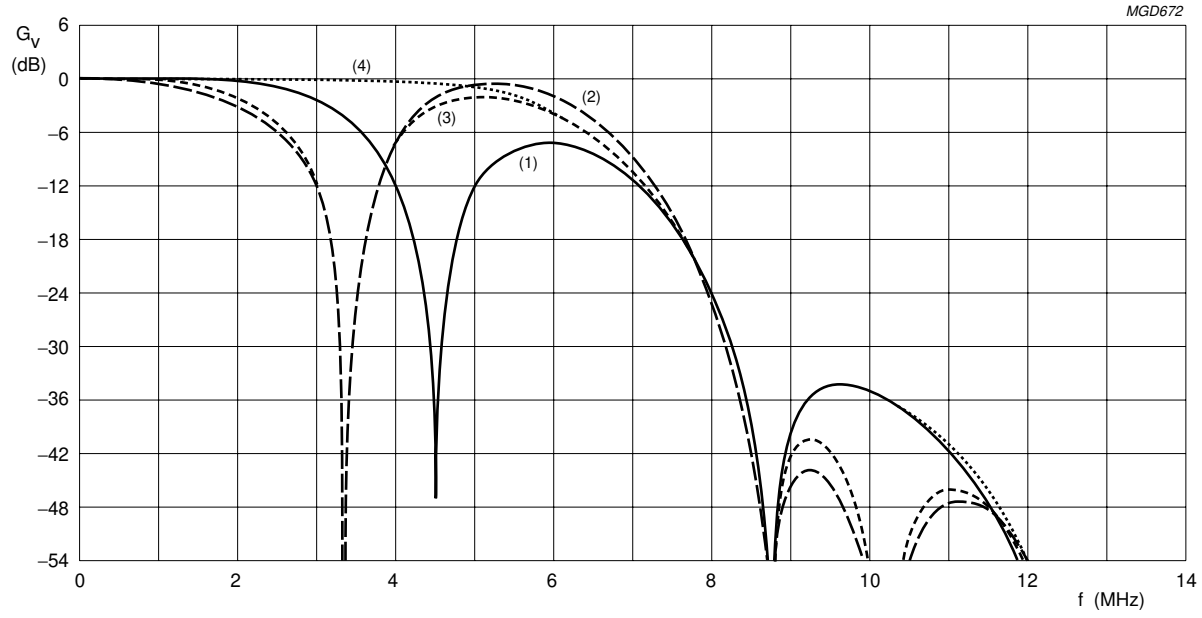
(1) SCBW = 1.
(2) SCBW = 0.

Fig.5 Chrominance transfer characteristic 1.



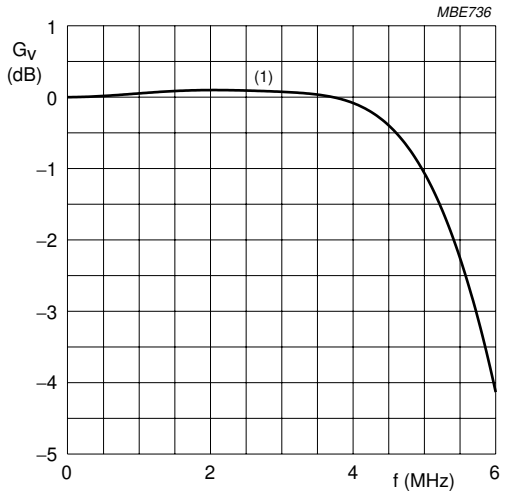
(1) SCBW = 1.
(2) SCBW = 0.

Fig.6 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.7 Luminance transfer characteristic 1 (excluding scaler).



(1) CCRS1 = 0; CCRS0 = 0.

Fig.8 Luminance transfer characteristic 2 (excluding scaler).

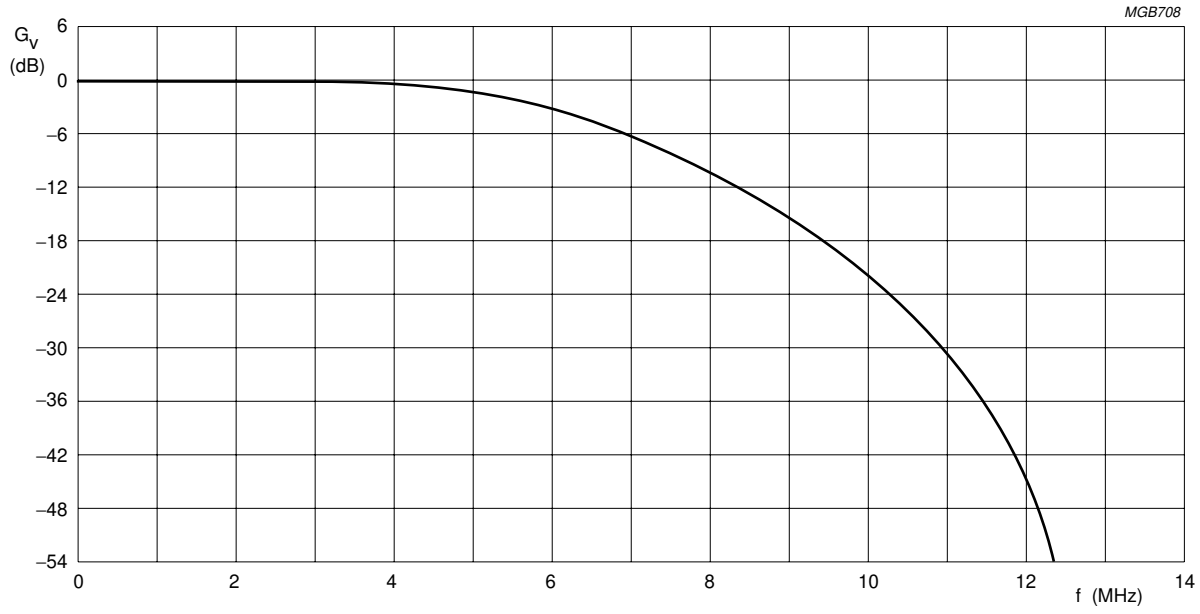


Fig.9 Luminance transfer characteristic in RGB (excluding scaler).

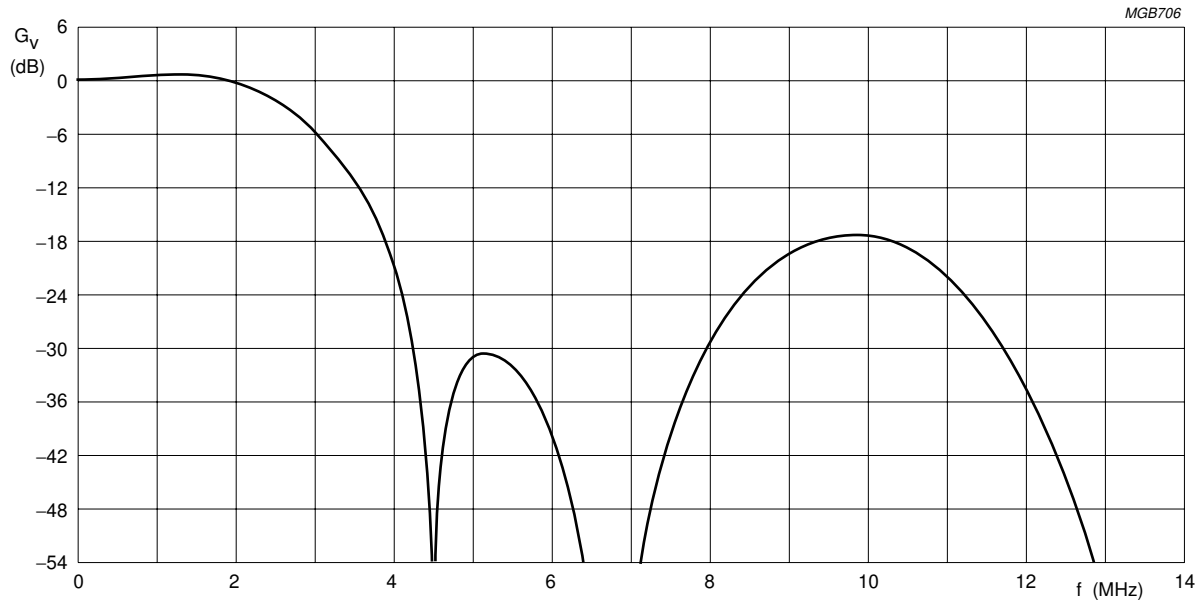


Fig.10 Colour difference transfer characteristic in RGB (excluding scaler).

8.1 Reset conditions

To activate the reset a pulse at least of 2 crystal clocks duration is required.

During reset ($\overline{RESET}$ = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{CBO}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I²C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I²C-bus access redefines the corresponding registers; see Table 2.

Table 2 Strapping pins

PIN	TIED	PRESET
FSVGC (pin G1)	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC (pin F1)	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{CBO}$ (pin G3)	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC (pin E3)	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2 (pin C4)	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal colour bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

8.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I²C-bus control bits EDGE1 and EDGE2 for correct operation.

If Y-C_B-C_R is being applied as a 27 Mbyte/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

8.3 RGB LUT

The three 256-byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed colour data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I²C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 × 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

8.4 Cursor insertion

A 32 × 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I²C-bus write access to specific registers or in the pixel data input via the PD port. In the latter case the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I²C-bus register as described in Table 5. Transparent means that the input pixels are passed through, the ‘cursor colours’ can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 3 Layout of a byte in the cursor bit map

D7	D6	D5	D4	D3	D2	D1	D0
pixel n + 3		pixel n + 2		pixel n + 1		pixel n	
D1	D0	D1	D0	D1	D0	D1	D0

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the ‘hot spot’, the other register controls the insertion position. The hot spot is the ‘tip’ of the pointer arrow.

It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 4 Cursor bit map

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
0	row 0 column 3		row 0 column 2		row 0 column 1		row 0 column 0	
1	row 0 column 7		row 0 column 6		row 0 column 5		row 0 column 4	
2	row 0 column 11		row 0 column 10		row 0 column 9		row 0 column 8	
...	...		...		...		...	
6	row 0 column 27		row 0 column 26		row 0 column 25		row 0 column 24	
7	row 0 column 31		row 0 column 30		row 0 column 29		row 0 column 28	
...	...		...		...		...	
254	row 31 column 27		row 31 column 26		row 31 column 25		row 31 column 24	
255	row 31 column 31		row 31 column 30		row 31 column 29		row 31 column 28	

Table 5 Cursor modes

CURSOR PATTERN	CURSOR MODE	
	CMODE = 0	CMODE = 1
00	second cursor colour	second cursor colour
01	first cursor colour	first cursor colour
10	transparent	transparent
11	inverted input	auxiliary cursor colour

8.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R colour space in this block. The colour difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

8.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the colour phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7108E; SAA7109E input data is in accordance with *"ITU-R BT.656"*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

8.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 129.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

Due to the re-interlacing, the circuit can perform upscaling. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 8.17.

8.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I²C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor. It is suggested to refer to Tables 6 to 23 for some representative combinations.

8.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true colour tint.

8.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd-harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I²C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 18 and 44 MHz.

8.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

8.12 Encoder

8.12.1 Video path

The encoder generates luminance and colour subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7108E only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 7 and 8. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be used for the Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 5 and 6.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, colour is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

8.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig.50.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

8.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

8.12.4 Closed Caption encoder

Using this circuit, data in accordance with the specification of Closed Caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

8.12.5 Anti-taping (SAA7108E only)

For more information contact your nearest Philips Semiconductors sales office.

8.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed.

The transfer curves of luminance and colour difference components of RGB are illustrated in Figs 9 and 10.

8.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10-bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the Y, C and optional RGB or C_R-Y-C_B outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually 75 Ω) during a pre-defined output. A flag in the I^2C-bus status byte reflects whether a load is applied or not.

If the SAA7108E; SAA7109E is required to drive a second (auxiliary) VGA monitor, the DACs receive the signal directly from the cursor insertion block. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

8.15 Timing generator

The synchronization of the SAA7108E; SAA7109E is able to operate in two modes; slave mode and master mode.

In slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT.656 data stream via PD7 to PD0.

Only vertical frequencies of 50 and 60 Hz are allowed with the SAA7108E; SAA7109E. In slave mode, it is not possible to lock the encoders colour carrier to the line frequency with the PHRES bits.

In the (more common) master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{\text{CBO}}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.

$\overline{\text{CBO}}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{\text{CBO}}$ goes active. This signal is programmable and it is possible to adjust the following (see Figs 48 and 49):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field.

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7108E; SAA7109E will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines. The additional request pulses will be suppressed with LUTL set to logic 0; see Table 139. The other vertical timings do not change in this case, so the first active line can be number 2, counted from 0.

8.16 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.

The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data bytes following subaddress FFH. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.

The I²C-bus slave address is defined as 88H.

8.17 Programming the graphics acquisition scaler of the video encoder

In order to program the graphics acquisition scaler it is first necessary to determine the input and output field timings. The timings are controlled by decoding binary counters that index the position in the current line and field respectively. In both cases, 0 means the start of the sync pulse.

At 60 Hz, the first visible pixel has the index 256, 710 pixels can be encoded; at 50 Hz, the index is 284, 702 pixels can be visible. Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns).

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 106.

ADWHS = 256 + 710 − OutPix (60 Hz);
ADWHS = 284 + 702 − OutPix (50 Hz);
ADWHE = ADWHS + OutPix × 2 (all frequencies)

For vertical, the procedure is the same. At 60 Hz, the first line with video information is number 19, 240 lines can be active. For 50 Hz, the numbers are 23 and 287; see Table 112.

$$FAL = 19 + \frac{240 - OutLin}{2} \text{ (60 Hz);}$$

$$FAL = 23 + \frac{287 - OutLin}{2} \text{ (50 Hz);}$$

LAL = FAL + OutLin (all frequencies)

Most TV sets use overscan, and not all pixels respectively lines are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is 10%, giving approximately 640 output pixels per line.

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:

$$TPclk = \frac{262.5 \times 1716 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 262.5\right)} \text{ (60 Hz)}$$

$$TPclk = \frac{312.5 \times 1728 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 312.5\right)} \text{ (50 Hz)}$$

and for the pixel clock generator $PCL = \frac{TXclk}{TPclk} \times 2^{21}$

(all frequencies); see Table 115.

The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:

$$YOFS = \frac{FAL \times 1716 \times TXclk}{InPpl \times TPclk} - 2 \text{ (60 Hz)}$$

$$YOFS = \frac{FAL \times 1728 \times TXclk}{InPpl \times TPclk} - 2 \text{ (50 Hz)}$$

In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

Once the timings are known the scaler can be programmed.

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX ≤ HLEN is fulfilled. Values given by the VESA display timings are preferred.

$$HLEN = InPpl - 1 \quad XPIX = \frac{InPix}{2} \quad XINC = \frac{OutPix}{InPix} \times 4096$$

XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1.

YPIX = InLin

YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth.

$$YINC = \frac{OutLin}{InLin + 2} \times \left(1 + \frac{YSKIP}{4095}\right) \times 4096$$

$$YIWGTO = \frac{YINC}{2} + 2048$$

$$YIWGTE = \frac{YINC - YSKIP}{2}$$

When YINC = 0 it sets the scaler to scaling factor 1. The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.

Due to the limited amount of memory it is not possible to get valid vertical scaler settings only from the formulae above. In some cases it is necessary to adjust the vertical offsets or the scaler increment to get valid settings. Tables 6 to 23 show verified settings. They are organised in the following way: The tables are separate for the standard to be encoded, the input resolution and three different anti-flicker filter settings. Each table contains 5 vertical sizes with 5 different offsets. They are intended to be selected according to the current TV set. The corresponding horizontal resolutions of 640 pixels give proper aspect ratios. They can be adjusted according to the formulae above. The next line gives a minimum size intended to fit on the screen under all circumstances. The corresponding horizontal resolution is 620 pixels. Overscan is only possible with an input resolution of 800 × 600 pixels. Where possible, the corresponding settings are given on the last lines of the tables.

8.18 Input levels and formats

The SAA7108E; SAA7109E accepts digital Y, C_B, C_R or RGB data with levels (digital codes) in accordance with *"ITU-R BT.601"*; see Table 24.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features an individual gain setting for luminance (GY) and colour difference signals (GCD). Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 6 Y scaler programming at NTSC, input frame size: 640 × 400, full anti-flicker filter

TV LINE	OFFSET	FAL	LAL	PCL	YINC	YSKIP	YOFSO	YOFSE	YIWGTO	YIWGTE
Regular size (horizontal TV size: 640 pixels, offset ±10 pixels)										
212	–4	29	241	1851099	2163	0	52	52	3128	1080
212	–2	31	243	1851099	2163	0	56	56	3128	1080
212	0	33	245	1851099	2163	0	60	60	3128	1080
212	2	35	247	1851099	2163	0	63	63	3128	1080
212	4	37	249	1851099	2163	0	67	67	3128	1080
214	–4	28	242	1836201	2181	0	50	50	3138	1090
214	–2	30	244	1836201	2181	0	54	54	3138	1090
214	0	32	246	1836201	2181	0	57	57	3138	1090
214	2	34	248	1836201	2181	0	61	61	3138	1090
214	4	36	250	1836201	2181	0	65	65	3138	1090
216	–4	27	243	1817578	2202	0	47	47	3148	1100
216	–2	29	245	1817578	2202	0	51	51	3148	1100
216	0	31	247	1817578	2202	0	55	55	3148	1100
216	2	33	249	1817578	2202	0	58	58	3148	1100
216	4	35	251	1817578	2202	0	62	62	3148	1100
218	–4	26	244	1802680	2222	0	45	45	3158	1110
218	–2	28	246	1802680	2222	0	49	49	3158	1110
218	0	30	248	1802680	2222	0	53	53	3158	1110
218	2	32	250	1802680	2222	0	56	56	3158	1110
218	4	34	252	1802680	2222	0	60	60	3158	1110
220	–4	25	245	1784057	2245	0	43	43	3168	1120
220	–2	27	247	1784057	2245	0	46	46	3168	1120
220	0	29	249	1784057	2245	0	50	50	3168	1120
220	2	31	251	1784057	2245	0	54	54	3168	1120
220	4	33	253	1784057	2245	0	57	57	3168	1120
Overscan (horizontal size: 710 pixels)										
241	0	0	0	0	0	0	0	0	0	0
Small size (horizontal size: 620 pixels)										
204	0	37	241	1925590	2079	0	70	70	3087	1039