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DATA SHEET

SAA7111A
Enhanced Video Input Processor (EVIP)

Product specification
Supersedes data of 1997 May 26
File under Integrated Circuits, IC22

1998 May 15

Philips
Semiconductors

PHILIPS

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Enhanced Video Input Processor (EVIP) SAA7111A

1 FEATURES

- Four analog inputs, internal analog source selectors, e.g. 4 × CVBS or 2 × Y/C or (1 × Y/C and 2 × CVBS)
- Two analog preprocessing channels
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 8-bit video CMOS analog-to-digital converters
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal-sync processing and clock generation
- Requires only one crystal (24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43, NTSC-Japan and SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Brightness Contrast Saturation (BCS) control on-chip
- The YUV (CCIR-601) bus supports a data rate of:
  - 864 × f_H = 13.5 MHz for 625 line sources
  - 858 × f_H = 13.5 MHz for 525 line sources.
- Data output streams for 16, 12 or 8-bit width with the following formats:
  - YUV 4 : 1 : 1 (12-bit)
  - YUV 4 : 2 : 2 (16-bit)
  - YUV 4 : 2 : 2 (CCIR-656) (8-bit)
  - RGB (5, 6, and 5) (16-bit) with dither
  - RGB (8, 8, and 8) (24-bit) with special application.
- Odd/even field identification by a non interlace CVBS input signal
- Fix level for RGB output format during horizontal blanking
- 720 active samples per line on the YUV bus
- One user programmable general purpose switch on an output pin
- Built-in line-21 text slicer
- A 27 MHz Vertical Blanking Interval (VBI) data bypass programmable by I²C-bus for INTERCAST applications
- Power-on control
- Two via I²C-bus switchable outputs for the digitized CVBS or Y/C input signals AD1 (7 to 0) and AD2 (7 to 0)
- Chip enable function (reset for the clock generator and power save mode up from chip version 3)
- Compatible with memory-based features (line-locked clock)
- Boundary scan test circuit complies with the *'IEEE Std. 1149.1 – 1990'* (ID-Code = 0 F111 02 B)
- I²C-bus controlled (full read-back ability by an external controller)
- Low power (<0.5 W), low voltage (3.3 V), small package (LQFP64)
- 5 V tolerant digital I/O ports.

2 APPLICATIONS

- Desktop/Notebook (PCMCIA) video
- Multimedia
- Digital television
- Image processing
- Video phone
- Intercast.

3 GENERAL DESCRIPTION

The Enhanced Video Input Processor (EVIP) is a combination of a two-channel analog preprocessing circuit including source selection, anti-aliasing filter and ADC, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a digital multi-standard decoder (PAL BGHI, PAL M, PAL N, NTSC M, NTSC-Japan NTSC N and SECAM), a brightness/contrast/saturation control circuit, a colour space matrix (see Fig.1) and a 27 MHz VBI-data bypass.

The pure 3.3 V CMOS circuit SAA7111A, analog front-end and digital video decoder, is a highly integrated circuit for desktop video applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into CCIR-601 compatible colour component values. The SAA7111A accepts as analog inputs CVBS or S-video (Y/C) from TV or VTR sources. The circuit is I^2C-bus controlled. The SAA7111A then supports several text features as Line 21 data slicing and a high-speed VBI data bypass for Intercast.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
T_{amb}	operating ambient temperature	0	25	70	°C
P_{A+D}	analog and digital power	–	0.5	–	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7111AHZ	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm	SOT314-2
SAA7111AH	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm	SOT393-1

6 BLOCK DIAGRAM

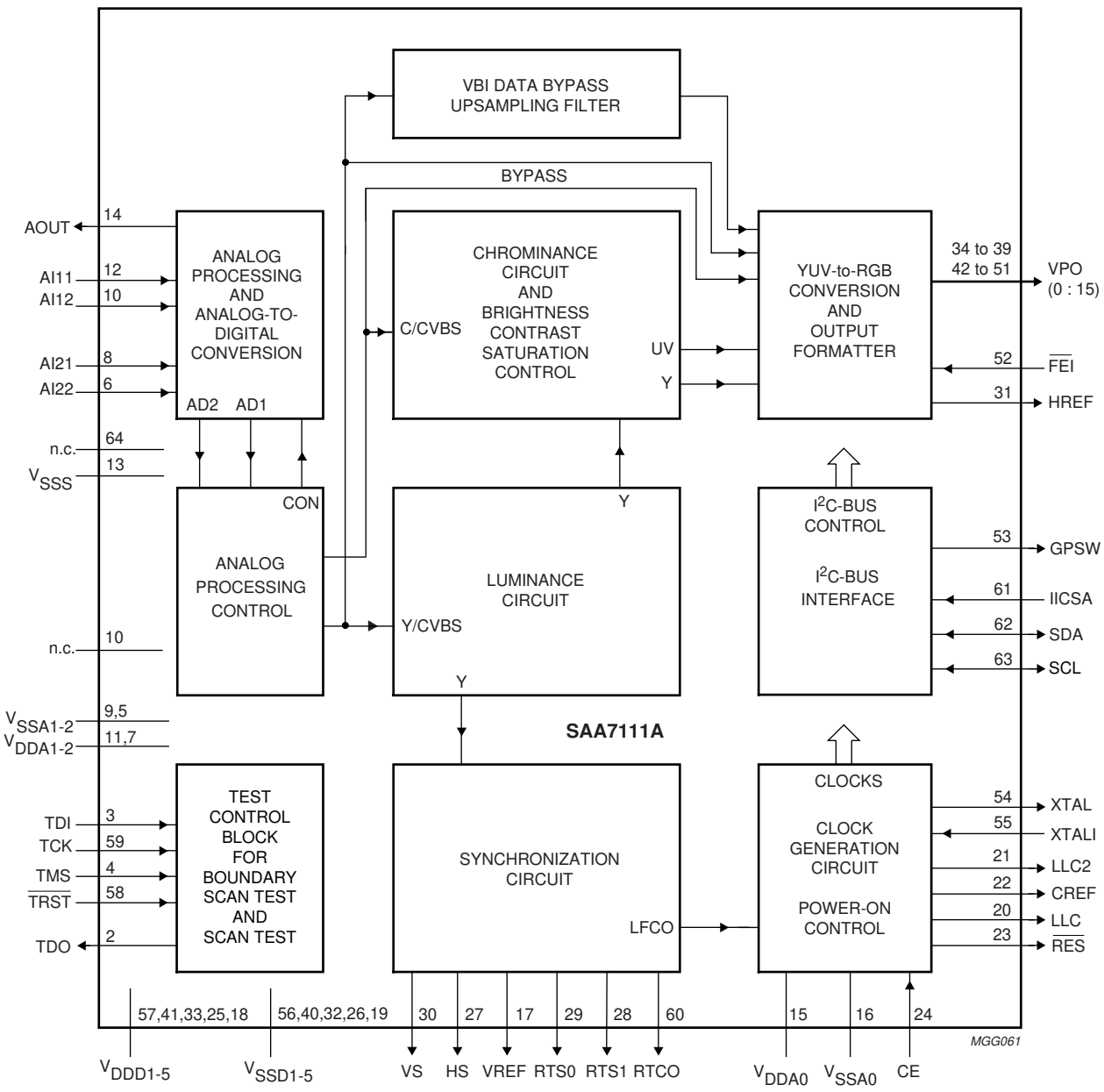


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN (L)QFP64	I/O/P	DESCRIPTION
n.c.	1	–	Do not connect.
TDO	2	O	Test data output for boundary scan test; note 1.
TDI	3	I	Test data input for boundary scan test; note 1.
TMS	4	I	Test mode select input for boundary scan test or scan test; note 1.
V_{SSA2}	5	P	Ground for analog supply voltage channel 2.
AI22	6	I	Analog input 22.
V_{DDA2}	7	P	Positive supply voltage for analog channel 2 (+3.3 V).
AI21	8	I	Analog input 21.
V_{SSA1}	9	P	Ground for analog supply voltage channel 1.
AI12	10	I	Analog input 12.
V_{DDA1}	11	P	Positive supply voltage for analog channel 1 (+3.3 V).
AI11	12	I	Analog input 11.
V_{SSS}	13	P	Substrate ground connection.
AOUT	14	O	Analog test output; for testing the analog input channels.
V_{DDA0}	15	P	Positive supply voltage for internal Clock Generator Circuit (CGC) (+3.3 V).
V_{SSA0}	16	P	Ground for internal CGC.
VREF	17	O	Vertical reference output signal (I^2C-bit COMPO = 0) or inverse composite blanking signal (I^2C-bit COMPO = 1) (enabled via I^2C-bus bit OEHV).
V_{DDD5}	18	P	Digital supply voltage 5 (+3.3 V).
V_{SSD5}	19	P	Ground for digital supply voltage 5.
LLC	20	O	Line-locked system clock output (27 MHz).
LLC2	21	O	Line-locked clock ½ output (13.5 MHz).
CREF	22	O	Clock reference output: this is a clock qualifier signal distributed by the internal CGC for a data rate of LLC2. Using CREF all interfaces on the VPO bus are able to generate a bus timing with identical phase. If CCIR 656 format is selected (OFTS0 = 1 and OFTS1 = 1) an inverse composite blanking signal (pixel qualifier) is provided on this pin.
$\overline{RES}$	23	O	Reset output (active LOW); sets the device into a defined state. All data outputs are in high impedance state. The I^2C-bus is reset (waiting for start condition).
CE	24	I	Chip enable; connection to ground forces a reset, up from version 3 power save function additionally available.
V_{DDD4}	25	P	Digital supply voltage input 4 (+3.3 V).
V_{SSD4}	26	P	Ground for digital supply voltage input 4.
HS	27	O	Horizontal sync output signal (programmable); the positions of the positive and negative slopes are programmable in 8 LLC increments over a complete line (equals 64 μs) via I^2C-bus bytes HSB and HSS. Fine position adjustment in 2 LLC increments can be performed via I^2C-bus bits HDEL1 and HDEL0.
RTS1	28	O	Two functions output; controlled by I^2C-bus bit RTSE1. RTSE1 = 0: PAL line identifier (LOW = PAL line); indicates the inverted and non-inverted R – Y component for PAL signals. RTSE1 = 1: H-PLL locked indicator; a high state indicates that the internal horizontal PLL has locked.

SYMBOL	PIN (L)QFP64	I/O/P	DESCRIPTION
RTS0	29	O	Two functions output; controlled by I²C-bus bit RTSE0. RTSE0 = 0: odd/even field identification (HIGH = odd field). RTSE0 = 1: vertical locked indicator; a HIGH state indicates that the internal Vertical Noise Limiter (VNL) has locked.
VS	30	O	Vertical sync signal (enabled via I²C-bus bit OEHV); this signal indicates the vertical sync with respect to the YUV output. The HIGH period of this signal is approximately six lines if the VNL function is active. The positive slope contains the phase information for a deflection controller.
HREF	31	O	Horizontal reference output signal (enabled via I²C-bus bit OEHV); this signal is used to indicate data on the digital YUV bus. The positive slope marks the beginning of a new active line. The HIGH period of HREF is 720 Y samples long. HREF can be used to synchronize data multiplexer/demultiplexer. HREF is also present during the vertical blanking interval.
V_{SSD3}	32	P	Ground for digital supply voltage input 3.
V_{DDD3}	33	P	Digital supply voltage 3 (+3.3 V).
VPO (15 to 10)	34 to 39	O	Digital VPO-bus (Video Port Out) signal; higher bits of the 16-bit VPO-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing scheme of the VPO-bus are controlled via I²C-bus bits OFTS0 and OFTS1. If I²C-bus bit VIPB = 1 the six MSBs of the digitized input signal are connected to these outputs, configured by the I²C-bus 'MODE' bits (see Figs 33 to 40): LUMA → VPO15 to VPO8, CHROMA → VPO7 to VPO0.
V_{SSD2}	40	P	Ground for digital supply voltage input 2.
V_{DDD2}	41	P	Digital supply voltage 2 (+3.3 V).
VPO (9 to 0)	42 to 51	O	Digital VPO-bus output signal; lower bits of the 16-bit YUV-bus or the 16-bit RGB-bus output signal. The output data rate, the format and multiplexing schema of the VPO-bus are controlled via I²C-bus bits OFTS0 and OFTS1. If I²C-bus bit VIPB = 1 the digitized input signal are connected to these outputs, configured by the I²C-bus 'MODE' bits (see Figs 33 to 40): LUMA → VPO15 to VPO8, CHROMA → VPO7 to VPO0.
$\overline{FEI}$	52	I	Fast enable input signal (active LOW); this signal is used to control fast switching on the digital YUV-bus. A HIGH at this input forces the IC to set its Y and UV outputs to the high impedance state.
GPSW	53	O	General purpose switch output; the state of this signal is set via I²C-bus control and the levels are TTL compatible.
XTAL	54	O	Second terminal of crystal oscillator; not connected if external clock signal is used.
XTALI	55	I	Input terminal for 24.576 MHz crystal oscillator or connection of external oscillator with CMOS compatible square wave clock signal.
V_{SSD1}	56	P	Ground for digital supply voltage input 1.
V_{DDD1}	57	P	Digital supply voltage input 1 (+3.3 V).
$\overline{TRST}$	58	I	Test reset input not (active LOW), for boundary scan test; notes 1, 2 and 3.
TCK	59	I	Test clock for boundary scan test; note 1.
RTCO	60	O	Real time control output: contains information about actual system clock frequency, subcarrier frequency and phase and PAL sequence.

SYMBOL	PIN (L)QFP64	I/O/P	DESCRIPTION
IICSA	61	I	I^2C-bus slave address select; 0 = 48H for write, 49H for read 1 = 4AH for write, 4BH for read.
SDA	62	I/O	Serial data input/output (I^2C-bus).
SCL	63	I/O	Serial clock input/output (I^2C-bus).
n.c.	64	–	Not connect.

Notes

1. In accordance with the '*IEEE1149.1*' standard the pads TCK, TDI, TMS and $\overline{\text{TRST}}$ are input pads with an internal pull-up transistor and TDO a 3-state output pad.
2. This pin provides easy initialization of BST circuit. $\overline{\text{TRST}}$ can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once.
3. For board design without boundary scan implementation (pin compatibility with the SAA7110) connect the $\overline{\text{TRST}}$ pin to ground.

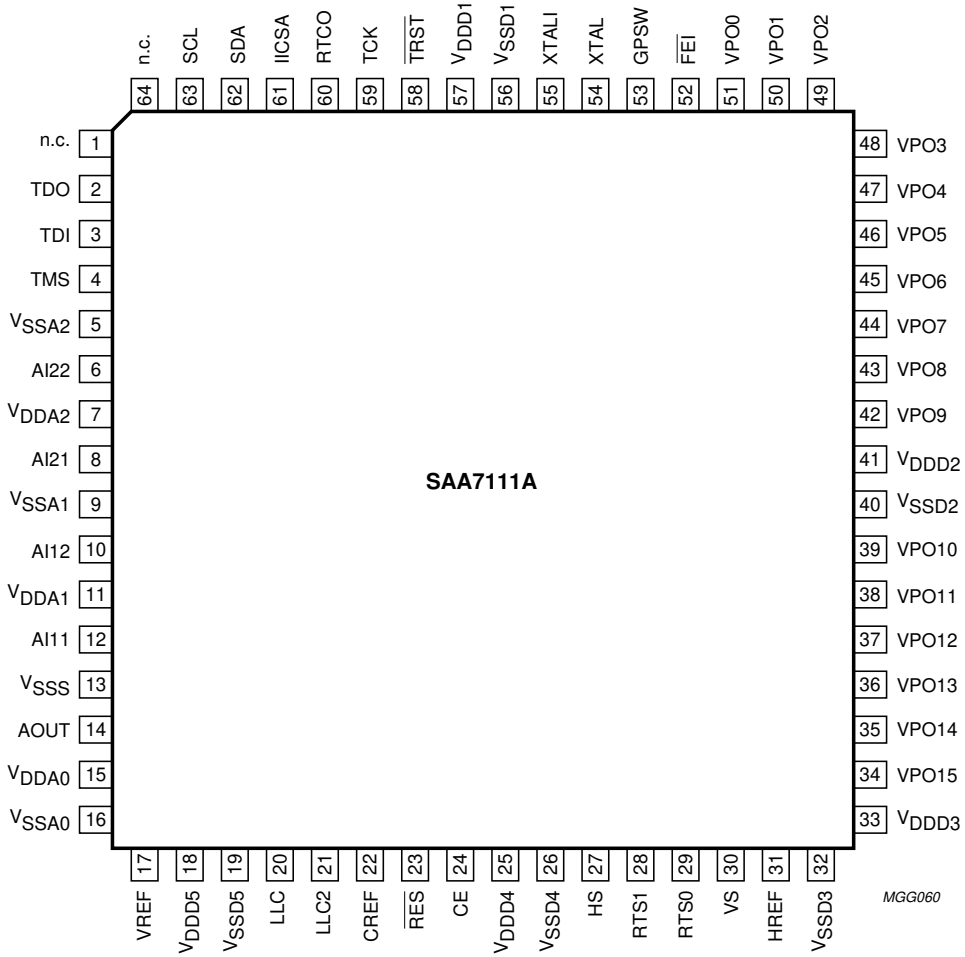


Fig.2 Pin configuration (LQFP64/QFP64).

8 FUNCTIONAL DESCRIPTION

8.1 Analog input processing

The SAA7111A offers four analog signal inputs, two analog main channels with source switch, clamp circuit, analog amplifier, anti-alias filter and video CMOS ADC (see Fig.5).

8.2 Analog control circuits

The anti-alias filters are adapted to the line-locked clock frequency via a filter control circuit. During the vertical blanking time, gain and clamping control are frozen.

8.2.1 CLAMPING

The clamp control circuit controls the correct clamping of the analog input signals. The coupling capacitor is also used to store and filter the clamping voltage. An internal digital clamp comparator generates the information with respect to clamp-up or clamp-down. The clamping levels for the two ADC channels are fixed for luminance (60) and chrominance (128). Clamping time in normal use is set with the HCL pulse at the back porch of the video signal.

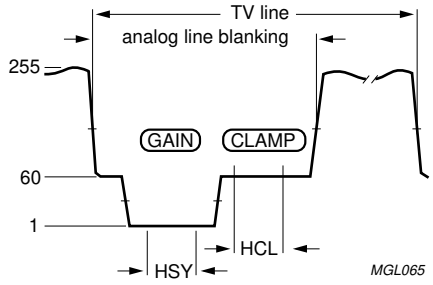


Fig.3 Analog line with clamp (HCL) and gain range (HSY).

8.2.2 GAIN CONTROL

Signal (white) peak control limits the gain at signal overshoots. The flow charts (see Figs 13 and 14) show more details of the AGC. The influence of supply voltage variation within the specified range is automatically eliminated by clamp and automatic gain control.

The gain control circuit receives (via the I^2C-bus) the static gain levels for the two analog amplifiers or controls one of these amplifiers automatically via a built-in automatic gain control (AGC) as part of the Analog Input Control (AICO).

The AGC (automatic gain control for luminance) is used to amplify a CVBS or Y signal to the required signal amplitude, matched to the ADCs input voltage range. The AGC active time is the sync bottom of the video signal.

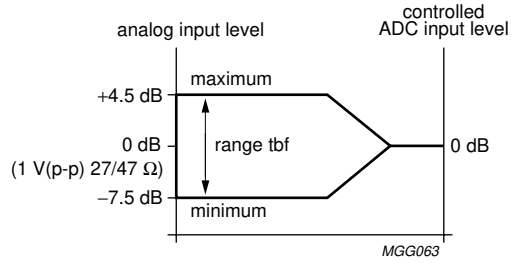


Fig.4 Automatic gain range.

8.3 Chrominance processing

The 8-bit chrominance signal is fed to the multiplication inputs of a quadrature demodulator, where two subcarrier signals from the local oscillator DTO1 are applied (0 and 90° phase relationship to the demodulator axis). The frequency is dependent on the present colour standard. The output signals of the multipliers are low-pass filtered (four programmable characteristics) to achieve the desired bandwidth for the colour difference signals (PAL and NTSC) or the 0 and 90° FM-signals (SECAM).

The colour difference signals are fed to the Brightness/Contrast/Saturation block (BCS), which includes the following five functions:

- AGC (Automatic Gain Control for chrominance PAL and NTSC)
- Chrominance amplitude matching (different gain factors for R – Y and B – Y to achieve CCIR-601 levels Cr and Cb for all standards)
- Chrominance saturation control
- Luminance contrast and brightness
- Limiting YUV to the values 1 (min.) and 254 (max.) to fulfil CCIR-601 requirements.

The SECAM-processing contains the following blocks:

- Baseband 'bell' filters to reconstruct the amplitude and phase equalized 0 and 90° FM-signals
- Phase demodulator and differentiator (FM-demodulation)
- De-emphasis filter to compensate the pre-emphasised input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM-switch signal).

The burst processing block provides the feedback loop of the chroma PLL and contains;

- Burst gate accumulator
- Colour identification and killer
- Comparison nominal/actual burst amplitude (PAL/NTSC standards only)
- Loop filter chrominance gain control (PAL/NTSC standards only)
- Loop filter chrominance PLL (only active for PAL/NTSC standards)
- PAL/SECAM sequence detection, H/2-switch generation
- Increment generation for DTO1 with divider to generate stable subcarrier for non-standard signals.

The chrominance comb filter block eliminates crosstalk between the chrominance channels in accordance with the PAL standard requirements. For NTSC colour standards the chrominance comb filter can be used to eliminate crosstalk from luminance to chrominance (cross-colour) for vertical structures. The comb filter can be switched off if desired. The embedded line delay is also used for SECAM recombination (cross-over switches).

The resulting signals are fed to the variable Y-delay compensation, RGB matrix, dithering circuit and output interface, which contains the VPO output formatter and the output control logic (see Fig.6).

8.4 Luminance processing

The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f_0 = 4.43 or 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-video (S-VHS and HI8) signals.

The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I^2C-bus) in two band-pass filters with selectable transfer characteristic. This signal is then added to the original (unpeaked) signal. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the BCS control located in the chrominance processing block (see Fig.7).

8.5 RGB matrix

Y, Cr and Cb data are converted after interpolation into RGB data in accordance with CCIR-601 recommendations. The realized matrix equations consider the digital quantization:

$R = Y + 1.371\ Cr$

$G = Y - 0.336\ Cb - 0.698\ Cr$

$B = Y + 1.732\ Cb.$

After dithering (noise shaping) the RGB data is fed to the output interface within the VPO-bus output formatter.

8.6 VBI-data bypass

For a 27 MHz VBI-data bypass the offset binary CVBS signal is upsampled behind the ADCs. Upsampling of the CVBS signal from 13.5 to 27 MHz is possible, because the ADCs deliver high performance at 13.5 MHz sample clock. Suppressing of the back folded CVBS frequency components after upsampling is achieved by an interpolation filter (see Fig.42).

The TUF block on the digital top level performs the upsampling and interpolation for the bypassed CVBS signal (see Fig.6).

For bypass details see Figs 8 to 10.

8.7 VPO-bus (digital outputs)

The 16-bit VPO-bus transfers digital data from the output interfaces to a feature box or a field memory, a digital colour space converter (SAA7192 DCSC), a video enhancement and digital-to-analog processor (SAA7165 VEDA2) or a colour graphics board (Targa-format) as a graphical user interface.

The output data formats are controlled via the I²C-bus bits OFTS0, OFTS1 and RGB888. Timing for the data stream formats, YUV (4 : 1 : 1) (12-bit), YUV (4 : 2 : 2) (16-bit), RGB (5, 6 and 5) (16-bit) and RGB (8, 8 and 8) (24-bit) with an LLC2 data rate, is achieved by marking each second positive rising edge of the clock LLC in conjunction with CREF (clock reference) (except RGB (8, 8 and 8), see special application in Fig.32). The higher output signals VPO15 to VPO8 in the YUV format perform the digital luminance signal. The lower output signals VPO7 to VPO0 in the YUV format are the bits of the multiplexed colour difference signals (B – Y) and (R – Y). The arrangement of the RGB (5, 6 and 5) and RGB (8, 8 and 8) data stream bits on the VPO-bus is given in Table 6.

The data stream format YUV 4 : 2 : 2 (the 8 higher output signals VPO15 to VPO8) in LLC data rate fulfils the CCIR-656 standard with its own timing reference code at the start and end of each video data block.

A pixel in the format tables is the time required to transfer a full set of samples. If 16-bit 4 : 2 : 2 format is selected two luminance samples are transmitted in comparison to one (B – Y) and one (R – Y) sample within a pixel. The time frames are controlled by the HREF signal.

Fast enable is achieved by setting input $\overline{FEI}$ to LOW. The signal is used to control fast switching on the digital VPO-bus. HIGH on this pin forces the VPO outputs to a high-impedance state (see Figs 18 and 19). The I²C-bus bit OEYC has to be set HIGH to use this function.

The digitized PAL, SECAM or NTSC signals AD1 (7 to 0) and AD2 (7 to 0) are connected directly to the VPO-bus via I²C-bus bit VIPB = 1 and MODE = 4, 5, 6 or 7.

AD1 (7 to 0) → VPO (15 to 8) and
AD2 (7 to 0) → VPO (7 to 0).

The selection of the analog input channels is controlled via I²C-bus subaddress 02 MODE select.

The upsampled 8-bit offset binary CVBS signal (VBI-data bypass) is multiplexed under control of the I²C-bus to the digital VPO-bus (see Fig.8).

8.8 Reference signals HREF, VREF and CREF

- HREF: The positive slope of the HREF output signal indicates the beginning of a new active video line. The high period is 720 luminance samples long and is also present during the vertical blanking.
  The description of timing and position from HREF is illustrated in Figs 15, 16, 21 and 23.
- VREF: The VREF output delivers a vertical reference signal or an inverse composite blank signal controlled via the I²C-bus [subaddress 11, inverse composite blank (COMPO)]. Furthermore four different modes of vertical reference signals are selectable via the I²C-bus [subaddress 13, vertical reference output control (VCTR1 and VCTR0)]. The description of VREF timing and position is illustrated in Figs 15, 16, 24 and 25.
- CREF: The CREF output delivers a clock/pixel qualifier signal for external interfaces to synchronize to the VPO-bus data stream.

  Four different modes for the clock qualifier signal are selectable via the I²C-bus [subaddress 13, clock reference output control (CCTR1 and CCTR0)]. The description of CREF timing and position is illustrated in Figs 16, 18, 20 and 21.

8.9 Synchronization

The prefiltered luminance signal is fed to the synchronization stage. Its bandwidth is reduced to 1 MHz in a low-pass filter. The sync pulses are sliced and fed to the phase detectors where they are compared with the sub-divided clock frequency. The resulting output signal is applied to the loop filter to accumulate all phase deviations. Internal signals (e. g. HCL and HSY) are generated in accordance with analog front-end requirements. The output signals HS, VS, and PLIN are locked to the timing reference, guaranteed between the input signal and the HREF signal, as further improvements to the circuit may change the total processing delay. It is therefore not recommended to use them for applications which require absolute timing accuracy on the input signals. The loop filter signal drives an oscillator to generate the line frequency control signal LFCO (see Fig.7).

8.10 Clock generation circuit

The internal CGC generates all clock signals required for the video input processor. The internal signal LFCO is a digital-to-analog converted signal provided by the horizontal PLL. It is the multiple of the line frequency

$$6.75\,\text{MHz} = \frac{429}{432} \times f_H$$

Internally the LFCO signal is multiplied by a factor of 2 or 4 in the PLL circuit (including phase detector, loop filtering, VCO and frequency divider) to obtain the LLC and LLC2 output clock signals. The rectangular output clocks have a 50% duty factor (see Fig.26).

8.11 Power-on reset and CE input

A missing clock, insufficient digital or analog V_{DDA0} supply voltages (below 2.7 V) will initiate the reset sequence; all outputs are forced to 3-state. The indicator output $\overline{RES}$ is LOW for approximately 128LLC after the internal reset and can be applied to reset other circuits of the digital TV system.

It is possible to force a reset by pulling the chip enable (CE) to ground. After the rising edge of CE and sufficient power supply voltage, the outputs LLC, LLC2, CREF, RTCO, RTS0, RTS1, GPSW and SDA return from 3-state to active, while HREF, VREF, HS and VS remain in 3-state and have to be activated via I²C-bus programming (see Table 5).

8.12 RTCO output

The real time control and status output signal contains serial information about the actual system clock (increment of the HPLL), subcarrier frequency [increment and phase (via reset) of the FSC-PLL] and PAL sequence bit. The signal can be used for various applications in external circuits, e.g. in a digital encoder to achieve clean encoding (see Fig.20).

8.13 The Line-21 text slicer

The text slicer block detects and acquires Line-21 Closed Captioning data from a 525-line CVBS signal. Extended data services on Line-21 Field 2 are also supported.
If valid data is detected the two data bytes are stored in two I²C-bus registers. A parity check is also performed and the result is stored in the MSB of the corresponding byte.
A third I²C-bus register is provided for data valid and data ready flags. The two bits F1VAL and F2VAL indicate that the input signal carries valid Closed Captioning data in the corresponding fields. The data ready bits F1RDY and F2RDY have to be evaluated if asynchronous I²C-bus reading is used.

8.13.1 Suggestions for I²C-bus interface of the display software reading line-21 data

There are two methods by which the software can acquire the data:

1. Synchronous reading once per frame (or once per field); It can use either the rising edge (Line-21 Field 1) or both edges (Line-21 Field 1 or 2) of the ODD signal (pin RTSO) to initiate an I²C-bus read transfer of the three registers 1A, 1B and 1C.
2. Asynchronous reading; It can poll either the F1RDY bit (Line-21 Field 1) or both F1RDY/F2RDY bits (Line-21 Field 1 or 2). After valid data has been read the corresponding F*RDY bit is set to LOW until new data has arrived. The polling frequency has to be slightly higher than the frame or field frequency, respectively.

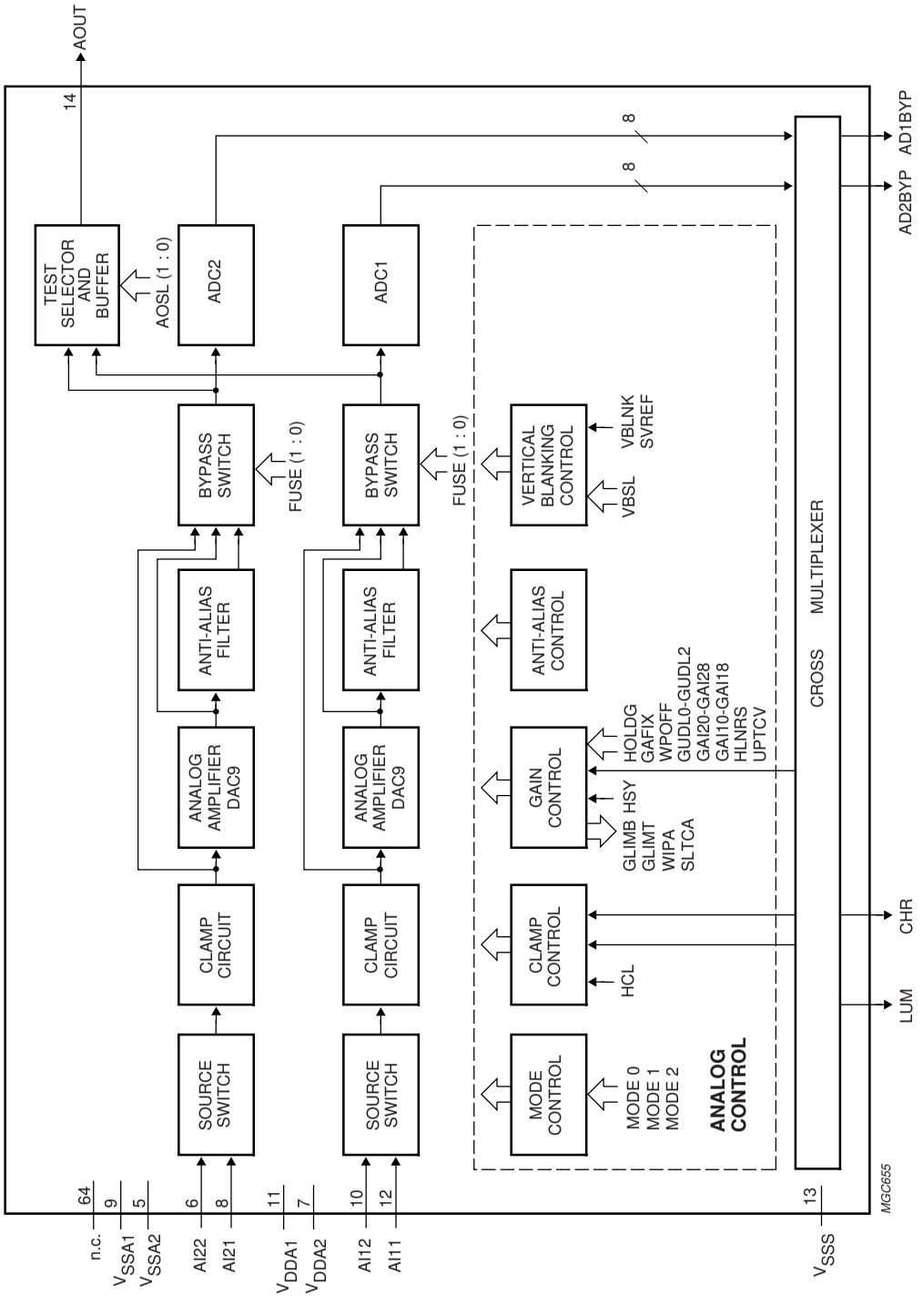


Fig.5 Analog input processing.

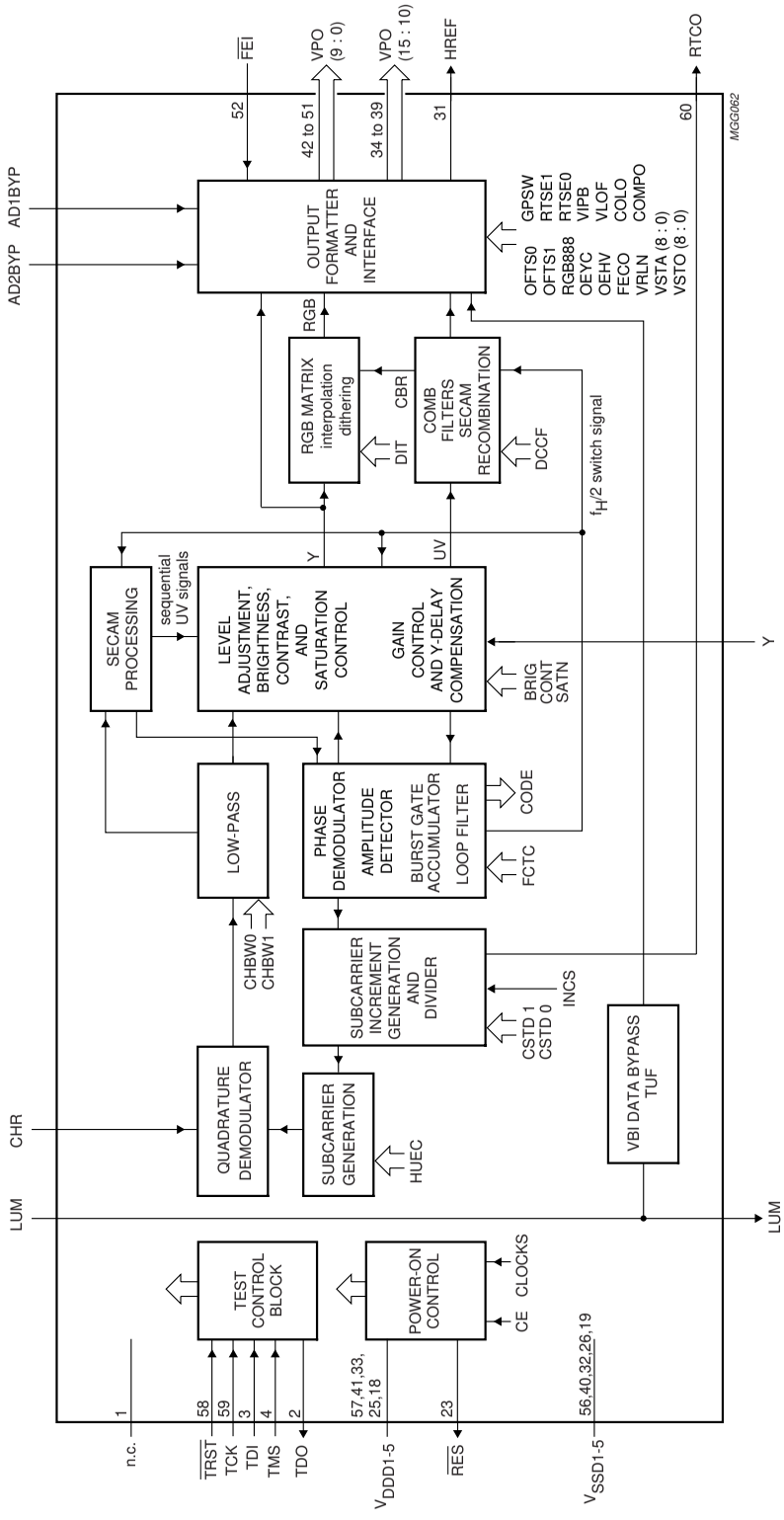


Fig.6 Chrominance circuit.

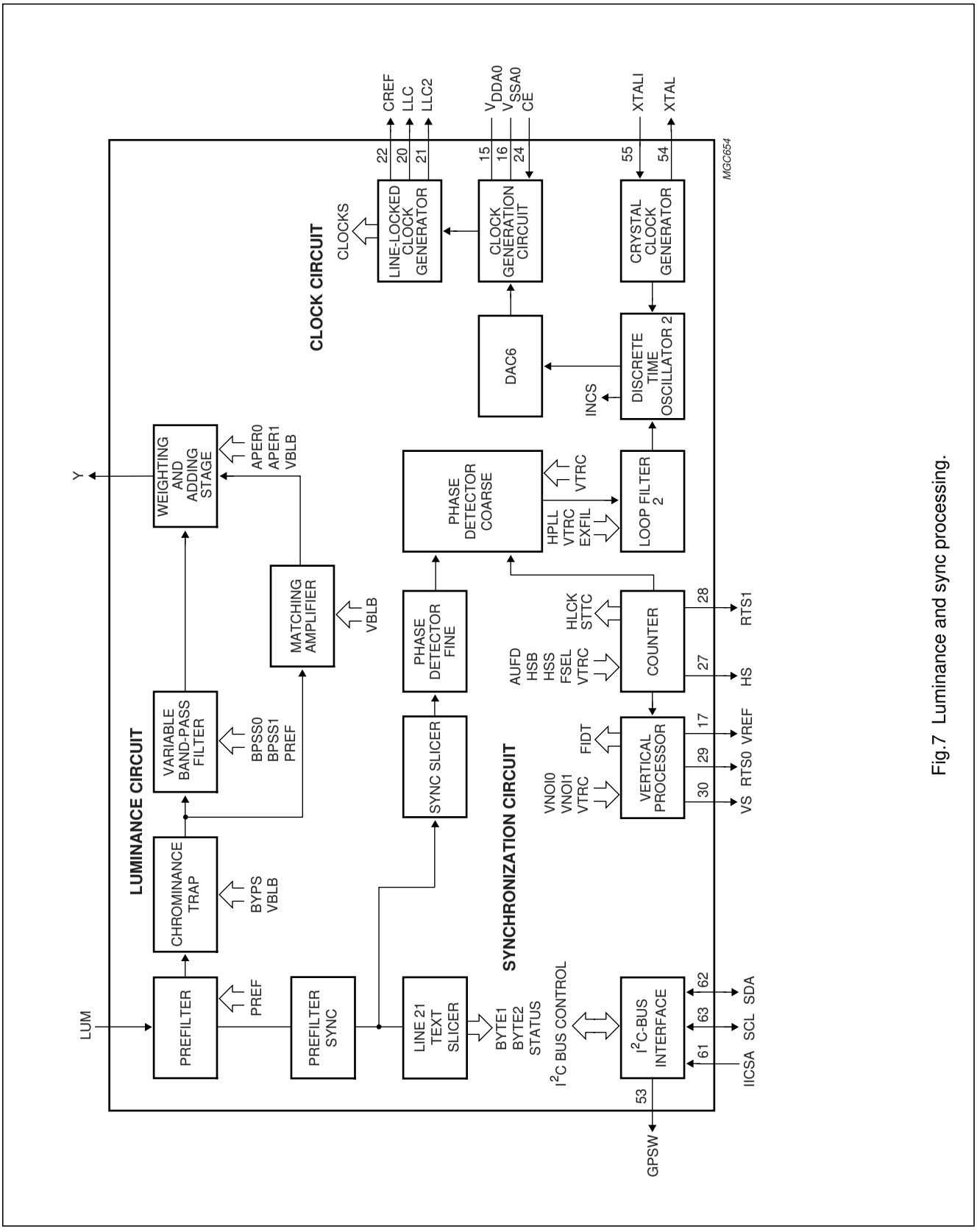
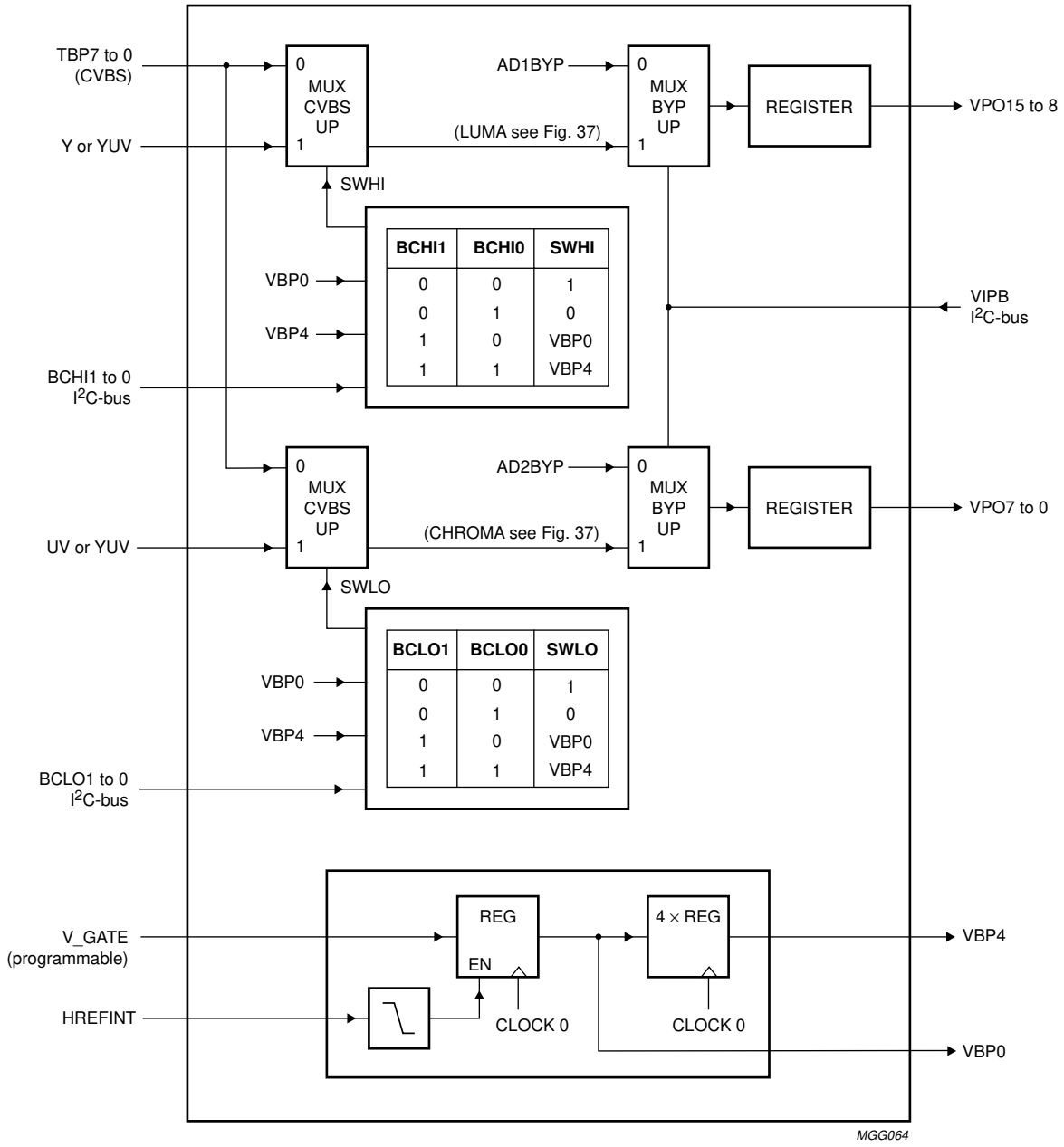
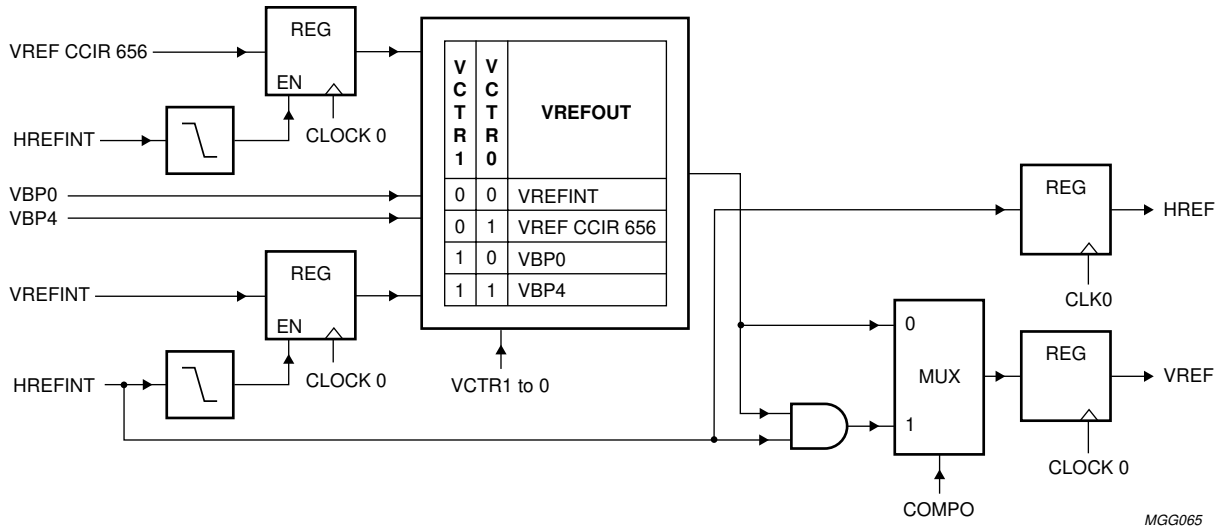


Fig.7 Luminance and sync processing.



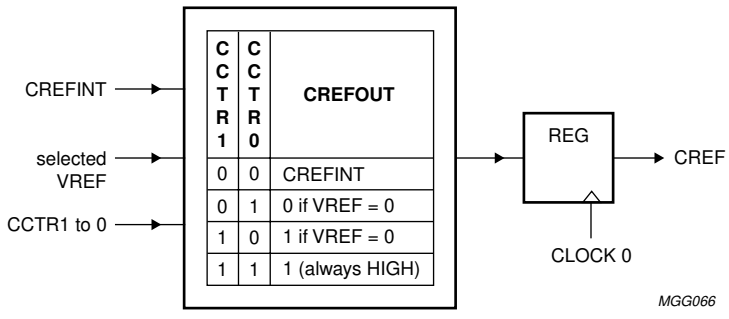
HREFINT = internal horizontal reference.
TBP = upsampled CVBS input data (27 MHz).
AD1BYP/AD2BYP = digitized CVBS input data and Y/C input data (13.5 MHz).
VBP0 = programmable vertical reference signal.
VBP4 = delayed programmable vertical reference signal (4LLC clocks delay).

Fig.8 Multiplexing of the CVBS signal to the VPO-bus.



VREF_CCIR 656 = vertical reference signal referring to the field interval definitions of CCIR656.
HREFINT = internal horizontal reference signal.
VREFINT = internal vertical reference signal.
VBP0 = programmable vertical reference signal.
VBP4 = delayed programmable vertical reference signal (4LLC clocks delay).

Fig.9 VREF output signal generation.



CREFINT = internal clock qualifier signal.

Fig.10 CREF output signal generation.

9 BOUNDARY-SCAN TEST

The SAA7111A has built in logic and 5 dedicated pins to support boundary-scan testing which allows board testing without special hardware (nails). The SAA7111A follows the *'IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture*' set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset (TRST), Test Data Input (TDI) and Test Data Output (TDO).

The BST functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported (see Table 1). Details about the JTAG BST-TEST can be found in the specification "*EEE Std. 1149.1"*. A file containing the detailed Boundary-Scan Description Language (BSDL) description of the SAA7111A is available on request.

9.1 Initialization of boundary-scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the TRST pin LOW.

9.2 Device identification codes

A Device Identification Register (DIR) is specified in *'IEEE Std. 1149.1-1990 - IEEE Standard Test Access Port and Boundary-Scan Architecture*' (IEEE Std. 1149.1b-1994). It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and determination of the version number of ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC.
The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller and this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number.
The device identification register contains 32-bits, numbered 31 to 0, where bit 31 is the Most Significant Bit (MSB) (nearest to TDI) and bit 0 is the Least Significant Bit (LSB) (nearest to TDO); see Fig.11.

Table 1 BST instructions supported by the SAA7111A

INSTRUCTION	DESCRIPTION
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary-scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary-scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.
INTEST	This optional instruction allows testing of the internal logic (no support for customers available).
USER1	This private instruction allows testing by the manufacturer (no support for customers available).

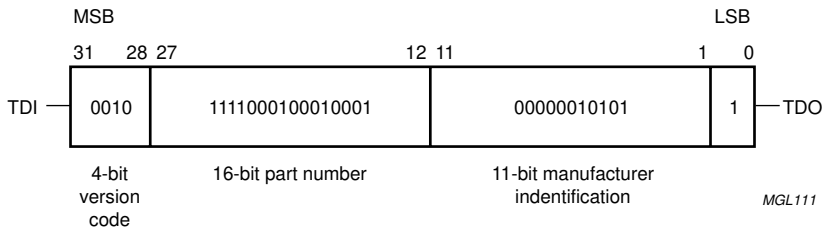


Fig.11 32 bits of identification code.

10 GAIN CHARTS

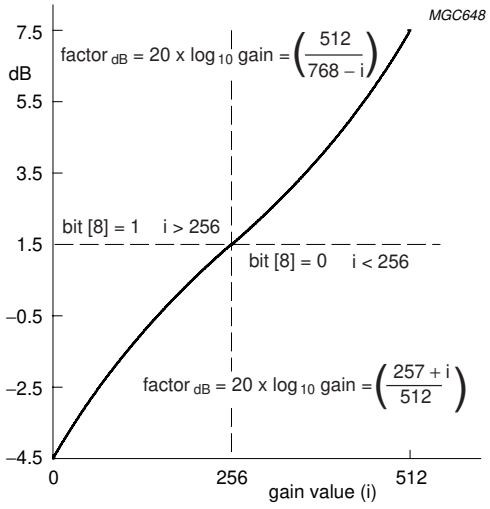
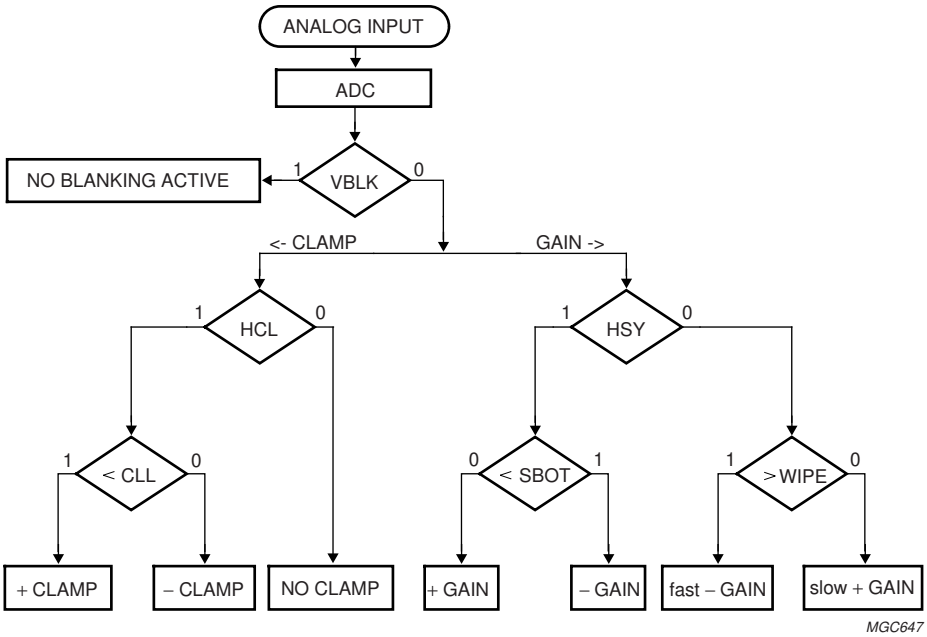
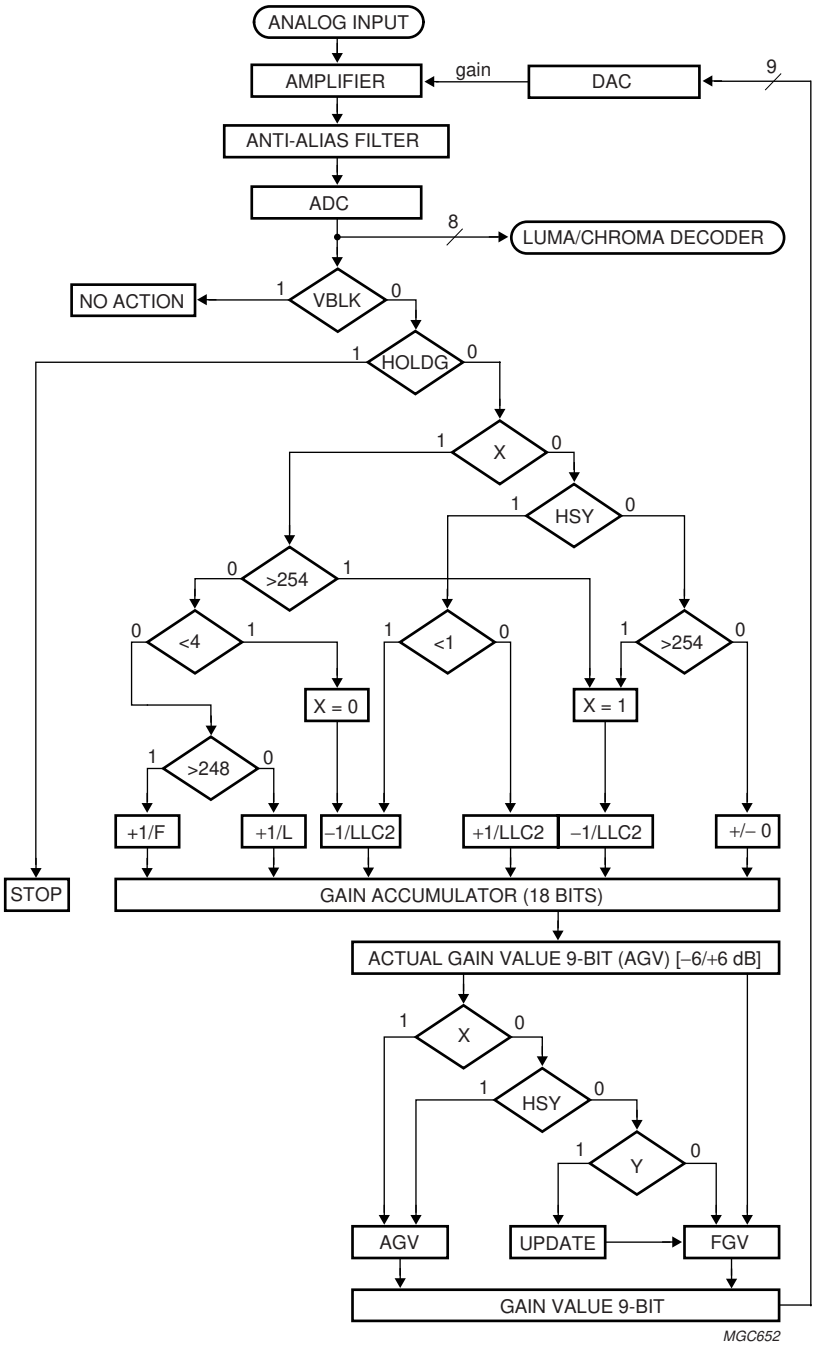


Fig.12 Amplifier curve.



WIPE = white peak level (254); SBOT = sync bottom level (1); CLL = clamp level [60 Y (128 C)];
HSY = horizontal sync pulse; HCL = horizontal clamp pulse.

Fig.13 Clamp and gain flow.



X = system variable; Y = IAGV − FGVI > GUDL; VBLK = vertical blanking pulse;
HSY = horizontal sync pulse; AGV = actual gain value; FGV = frozen gain value.

Fig.14 Gain flow chart.

11 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); all ground pins connected together and all supply pins connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.5	+4.6	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
$V_{i(A)}$	input voltage at analog inputs		–0.5	V_{DDA} + 0.5 (4.6 max.)	V
$V_{o(A)}$	output voltage at analog output		–0.5	V_{DDA} + 0.5	V
$V_{i(D)}$	input voltage at digital inputs and outputs	outputs in 3-state	–0.5	+5.5	V
$V_{o(D)}$	output voltage at digital outputs	outputs active	–0.5	V_{DDD} + 0.5	V
ΔV_{SS}	voltage difference between V_{SSAall} and V_{SSall}		–	100	mV
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
$T_{amb(bias)}$	operating ambient temperature under bias		–10	+80	°C
V_{esd}	electrostatic discharge all pins	note 1	–2000	+2000	V

Note

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

12 CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; V_{DDA} = 3.1 to 3.5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current		–	63	70	mA
P_D	digital power		–	0.21	–	W
V_{DDA}	analog supply voltage		3.1	3.3	3.5	V
I_{DDA}	analog supply current	AOSL = [1:0] = 00b; AOUT not connected	–	52	–	mA
P_A	analog power		–	0.17	–	W
P_{A+D}	analog and digital power		–	0.38	–	W
P_{pd}	analog and digital power in power-down mode	CE connected to ground (since version 3)	–	0.02	–	W
Analog part						
I_{clamp}	clamping current	V_I = 0.9 V DC	–	±3.5	–	μA
$V_{i(p-p)}$	input voltage (peak-to-peak value)	for normal video levels [1 V (p-p)]; –3 dB termination 27/47 Ω and AC coupling required; coupling capacitor = 22 nF	0.3	0.7	1.2	V
$\|Z_i\|$	input impedance	clamping current off	200	–	–	kΩ
C_i	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α_{cs}	channel crosstalk	f_i = 5 MHz	–	–	–50	dB
Analog-to-digital converters						
B	bandwidth	at –3 dB	–	7	–	MHz
ϕ_{diff}	differential phase (amplifier plus anti-alias filter = bypass)		–	2	–	deg
G_{diff}	differential gain (amplifier plus anti-alias filter = bypass)		–	2	–	%
f_{clkADC}	ADC clock frequency		12.8	–	14.3	MHz
DLE	DC differential linearity error		–	0.7	–	LSB
ILE	DC integral linearity error		–	1	–	LSB
Digital inputs						
$V_{IL(SCL,SDA)}$	LOW level input voltage pins SDA and SCL		–0.5	–	+0.3V_{DDD}	V
V_{IH}	HIGH level input voltage pins SDA and SCL		0.7V_{DDD}	–	V_{DDD} + 0.5	V
$V_{IL(xtal)}$	LOW level CMOS input voltage pin XTALI		–0.3	–	+0.8	V
$V_{IH(xtal)}$	HIGH level CMOS input voltage pin XTALI		2.0	–	V_{DDD} + 0.3	V
V_{ILn}	LOW level input voltage all other inputs		–0.3	–	+0.8	V
V_{IHn}	HIGH level input voltage all other inputs		2.0	–	5.5	V
I_{LI}	input leakage current		–	–	1	µA
C_i	input capacitance	outputs at 3-state	–	–	8	pF
$C_{i(n)}$	input capacitance all other inputs		–	–	5	pF
Digital outputs						
$V_{OL(SCL,SDA)}$	LOW level output voltage pins SDA and SCL	SDA/SCL at 3 mA (6 mA) sink current	–	–	0.4 (0.6)	V
V_{OL}	LOW level output voltage	V_{DDD} = max; I_{OL} = 2 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	V_{DDD} = min, I_{OH} = –2 mA	2.4	–	V_{DDD} + 0.5	V
$V_{OL(clk)}$	LOW level output voltage for clocks		–0.5	–	+0.6	V
$V_{OH(clk)}$	HIGH level output voltage for clocks		2.4	–	V_{DDD} + 0.5	V
I_{LO}	output leakage current	at 3-state mode	–	–	10	µA
$\overline{FEI}$ input timing						
$t_{SU;DAT}$	input data set-up time		13	–	–	ns
$t_{HD;DAT}$	input data hold time		3	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data and control output timing; note 1						
C_L	output load capacitance		15	–	40	pF
$t_{OHD;DAT}$	output hold time	C_L = 15 pF	4	–	–	ns
t_{PD}	propagation delay	C_L = 25 pF	–	–	20	ns
t_{PDZ}	propagation delay to 3-state		–	–	20	ns
Clock output timing (LLC and LLC2); note 2						
$C_{L(LLC)}$	output load capacitance		15	–	40	pF
T_{cy}	cycle time	LLC	35	–	39	ns
		LLC2	70	–	78	ns
δ_{LLC}	duty factors for t_{LLCH}/t_{LLC} and t_{LLC2H}/t_{LLC2}	C_L = 25 pF	40	–	60	%
t_r	rise time LLC, LLC2		–	–	5	ns
t_f	fall time LLC, LLC2		–	–	5	ns
t_d	delay time LLC output to LLC2 output	at 1.5 V; LLC/LLC2 = 25 pF	–4	–	+8	ns
Data qualifier output timing (CREF)						
$t_{OHD;CREF}$	output hold time	C_L = 15 pF	4	–	–	ns
$t_{PD;CREF}$	propagation delay from positive edge of LLC	C_L = 25 pF	–	–	20	ns
Clock input timing (XTALI)						
δ_{XTALI}	duty factor for t_{XTALIH}/t_{XTALI}	nominal frequency	40	–	60	%
Horizontal PLL						
f_{Hn}	nominal line frequency	50 Hz field	–	15625	–	Hz
		60 Hz field	–	15734	–	Hz
$\Delta f_H/f_{Hn}$	permissible static deviation		–	–	5.7	%
Subcarrier PLL						
f_{SCn}	nominal subcarrier frequency	PAL BGHI	–	4433619	–	Hz
		NTSC M; NTSC-Japan	–	3579545	–	Hz
		PAL M	–	3575612	–	Hz
		PAL N	–	3582056	–	Hz
Δf_{SC}	lock-in range		±400	–	–	Hz
Crystal oscillator						
f_n	nominal frequency	3rd harmonic; note 3	–	24.576	–	MHz
$\Delta f/f_n$	permissible nominal frequency deviation		–	–	±50	10^{-6}