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SAA7128H; SAA7129H

Digital video encoder

Rev. 03 — 9 December 2004 Product data sheet

1. General description

The SAA7128H; SAA7129H encodes digital C_R-Y-C_B video data to an NTSC, PAL or SECAM CVBS or S-video signal. Simultaneously, RGB or bypassed but interpolated C_R-Y-C_B signals are available via three additional DACs. The circuit at a 54 MHz multiplexed digital D1 input port accepts two *ITU-R BT.656* compatible C_R-Y-C_B data streams with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data with overlay and MPEG decoded data without overlay, where one data stream is latched at the rising clock edge and the other at the falling clock edge.

It includes a sync/clock generator and on-chip DACs.

2. Features

- Monolithic CMOS 3.3 V device, 5 V I²C-bus optional
- Digital PAL/NTSC/SECAM encoder
- System pixel frequency 13.5 MHz
- 54 MHz double-speed multiplexed D1 interface capable of splitting data into two separate channels (encoded and baseband)
- Three Digital-to-Analog Converters (DACs) for CVBS (CSYNC), VBS (CVBS) and C (CVBS) two times oversampled with 10-bit resolution (signals in brackets optional)
- Three DACs for RED (C_R), GREEN (Y) and BLUE (C_B) two times oversampled with 9-bit resolution (signals in brackets optional)
- An advanced composite sync is available on the CVBS output for RGB display centering
- Real-time control of subcarrier
- Cross-color reduction filter
- Closed captioning encoding and World Standard Teletext (WST) and North-American Broadcast Text System (NABTS) teletext encoding including sequencer and filter
- Copy Generation Management System (CGMS) encoding (CGMS described by standard CPR-1204 of EIAJ); 20 bits in lines 20/283 (NTSC) can be loaded via I²C-bus
- Fast I²C-bus control port (400 kHz)
- Line 23 Wide Screen Signalling (WSS) encoding
- Video Programming System (VPS) data encoding in line 16 (50/625 lines counting)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Color Bar Generator (CBG)

PHILIPS

- Macrovision® Pay-per-View copy protection system rev. 7.01 and rev. 6.1 optional; this applies to SAA7128H only. The device is protected by US patents 4631603, 4577216 and 4819098 and other intellectual property rights; use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited; please contact your nearest Philips Semiconductors sales office for more information.
- Controlled rise/fall times of output syncs and blanking
- On-chip crystal oscillator (3rd-harmonic or fundamental crystal)
- Down mode (low output voltage) or power-save mode of DACs
- QFP44 package

3. Quick reference data

Table 1: Quick reference data

V_{DDD} = 3.0 V to 3.6 V; T_{amb} = 0 °C to 70 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage			3.15	3.3	3.45	V
V_{DDD}	digital supply voltage			3.0	3.3	3.6	V
I_{DDA}	analog supply current		[1]	-	130	150	mA
I_{DDD}	digital supply current	V_{DDD} = 3.3 V	[1]	-	75	100	mA
V_i	input signal voltage levels			TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)			1.25	1.35	1.50	V
R_L	load resistance			75	-	300	Ω
$LE_{lf(i)}$	low frequency integral linearity error			-	-	±3	LSB
$LE_{lf(d)}$	low frequency differential linearity error			-	-	±1	LSB
T_{amb}	ambient temperature			0	-	70	°C

[1] At maximum supply voltage with highly active input signals.

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAA7128H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
SAA7129H			

5. Block diagram

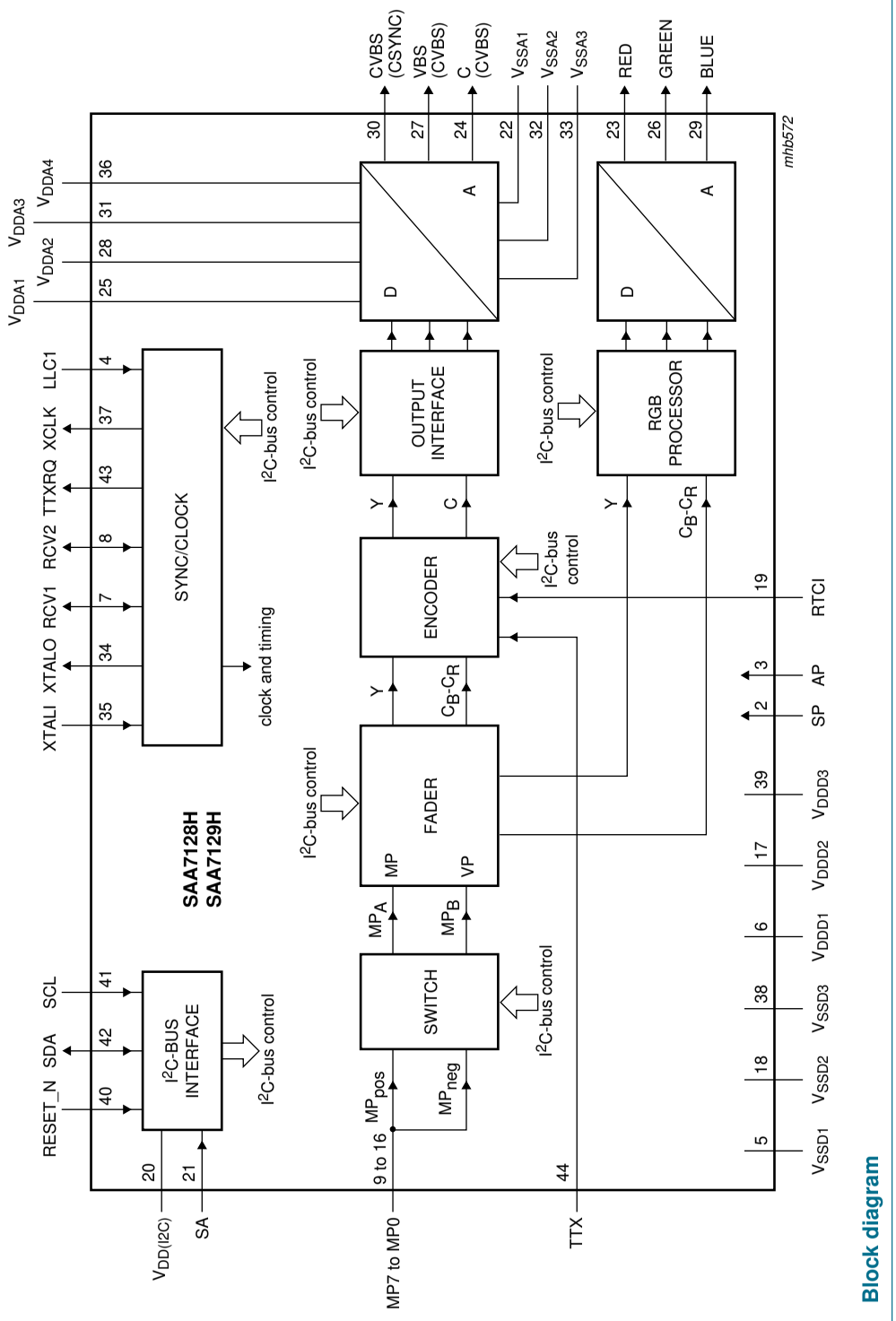

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

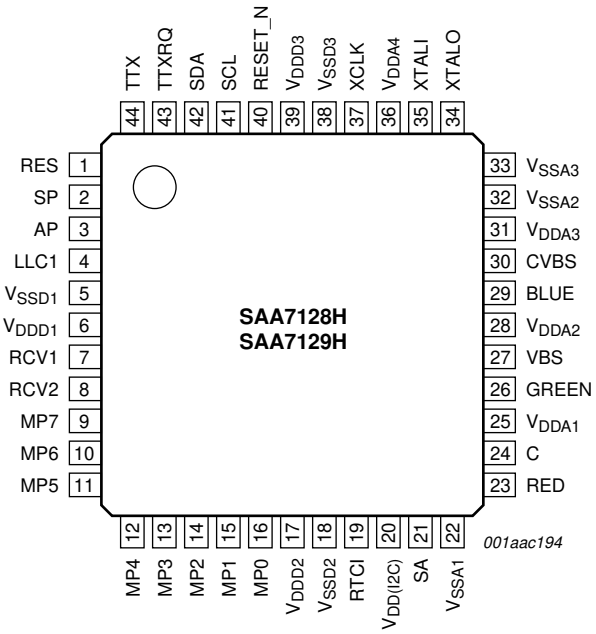

Fig 2. Pin configuration

6.2 Pin description

Table 3: Pinning

Symbol	Pin	Type	Description
RES	1	-	reserved pin; do not connect
SP	2	I	test pin; connected to digital ground for normal operation
AP	3	I	test pin; connected to digital ground for normal operation
LLC1	4	I	line-locked clock input; this is the 27 MHz master clock
V_{SSD1}	5	supply	digital ground 1
V_{DDD1}	6	supply	digital supply voltage 1
RCV1	7	I/O	raster control 1 for video port; this pin receives/provides a VS/FS/FSEQ signal
RCV2	8	I/O	raster control 2 for video port; this pin provides an HS pulse of programmable length or receives an HS pulse

Table 3: Pinning...*continued*

Symbol	Pin	Type	Description
MP7	9	I	double-speed 54 MHz MPEG port; it is an input for *ITU-R BT.656* style multiplexed C_R-Y-C_B data; data is sampled on the rising and falling clock edge; data sampled on the rising edge is then sent to the encoding part of the device; data sampled on the falling edge is sent to the RGB part of the device (or vice versa, depending on programming)
MP6	10	I	
MP5	11	I	
MP4	12	I	
MP3	13	I	
MP2	14	I	
MP1	15	I	
MP0	16	I	
V_{DDD2}	17	supply	digital supply voltage 2
V_{SSD2}	18	supply	digital ground 2
RTCI	19	I	real-time control input; if the LLC1 clock is provided by an SAA7113 or SAA7118, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality
$V_{DD(I2C)}$	20	supply	sense input for I^2C-bus voltage; connect to I^2C-bus supply
SA	21	I	select I^2C-bus address; LOW selects slave address 88h, HIGH selects slave address 8Ch
V_{SSA1}	22	supply	analog ground 1 for RED (C_R), C (CVBS) and GREEN (Y) outputs
RED	23	O	analog output of RED (C_R) signal
C	24	O	analog output of chrominance (CVBS) signal
V_{DDA1}	25	supply	analog supply voltage 1 for RED (C_R) and C (CVBS) outputs
GREEN	26	O	analog output of GREEN (Y) signal
VBS	27	O	analog output of VBS (CVBS) signal
V_{DDA2}	28	supply	analog supply voltage 2 for VBS (CVBS) and GREEN (Y) outputs
BLUE	29	O	analog output of BLUE (C_B) signal
CVBS	30	O	analog output of CVBS (CSYNC) signal
V_{DDA3}	31	supply	analog supply voltage 3 for BLUE (C_B) and CVBS (CSYNC) outputs
V_{SSA2}	32	supply	analog ground 2 for VBS (CVBS), BLUE (C_B) and CVBS (CSYNC) outputs
V_{SSA3}	33	supply	analog ground 3 for the DAC reference ladder and the oscillator
XTALO	34	O	crystal oscillator output
XTALI	35	I	crystal oscillator input; if the oscillator is not used, this pin should be connected to ground
V_{DDA4}	36	supply	analog supply voltage 4 for the DAC reference ladder and the oscillator
XCLK	37	O	clock output of the crystal oscillator
V_{SSD3}	38	supply	digital ground 3
V_{DDD3}	39	supply	digital supply voltage 3
RESET_N	40	I	Reset input, active LOW. After reset is applied, all digital I/Os are in input mode; PAL black burst on CVBS, VBS and C; RGB outputs set to lowest voltage. The I^2C-bus receiver waits for the START condition.
SCL	41	I/(O)	serial clock input (I^2C-bus) with inactive output path
SDA	42	I/O	serial data input/output (I^2C-bus)
TTXRQ	43	O	teletext request output, indicating when text bits are requested
TTX	44	I	teletext bit stream input

7. Functional description

The digital video encoder encodes digital luminance and color difference signals into analog CVBS, S-video and simultaneously RGB or C_R-Y-C_B signals. NTSC-M, PAL-B/G, SECAM and sub-standards are supported.

Both interlaced and non-interlaced operation is possible for all standards.

The basic encoder function consists of subcarrier generation and color modulation and insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of *RS170A* and *ITU-R BT.470-3*.

For ease of post analog filtering the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

The total filter transfer characteristics are illustrated in Figure 8 to Figure 13. The DACs for Y, C and CVBS are realized with full 10-bit resolution; 9-bit resolution for RGB output. The C_R-Y-C_B to RGB dematrix can be bypassed optionally in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_R-Y-C_B formats are *ITU-R BT.656* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally when the device is operated in slave mode. Two independent data streams can be processed, one latched by the rising edge of LLC1, the other latched by the falling edge of LLC1. The purpose of that is e.g. to forward one of the data streams containing both video and On-Screen Display (OSD) information to the RGB outputs, and the other stream containing video only to the encoded outputs CVBS and S-video.

For optimum display of RGB signals through a euro-connector TV set, an early composite sync pulse (up to 31 LLC1 clock periods) can be provided at the CVBS output.

As a further alternative, the VBS and C outputs may provide a second and third CVBS signal.

It is also possible to connect a Philips digital video decoder (SAA7111A, SAA7113 or SAA7118) to the SAA7128H; SAA7129H. Via the RTCI pin, connected to RTCO of a decoder, information concerning actual subcarrier, PAL-ID and definite subcarrier phase can be inserted.

The device synthesizes all necessary internal signals, color subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via I^2C-bus.

The IC also contains closed caption and extended data services encoding (line 21), and supports anti-taping signal generation in accordance with Macrovision. It is also possible to load data for copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters, such as:

- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude, etc.

During reset (RESET_N = LOW) and after reset is released, all digital I/O stages are set to input mode and the encoder is set to PAL mode and outputs a 'black burst' signal on CVBS and S-video outputs, while RGB outputs are set to their lowest output voltages. A reset forces the I^2C-bus interface to abort any running bus transfer.

7.1 Versatile fader

Important note: whenever the fader is activated with the SYMP bit set to a logic 1 (enabling the detection of embedded Start of Active Video (SAV) and End of Active Video (EAV)), codes 00h and FFh are not allowed within the actual video data (as prescribed by *ITU-R BT.656*). If SAV (00h) has been detected, the fader automatically passes 100% of the respective signal until SAV is detected.

Within the digital video encoder, two data streams can be faded against each other; these data streams can be input to the double speed MPEG port, which is able to separate two independent 27 MHz data streams MP_A and MP_B via a cross switch controlled by EDGE1 and EDGE2.

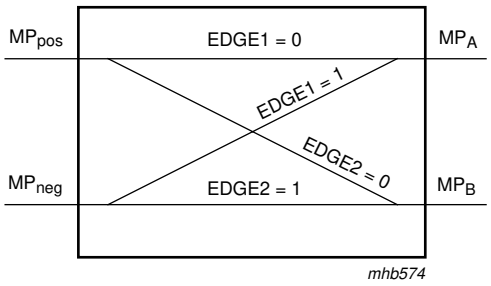

Fig 3. Cross switch

7.1.1 Configuration examples

Figure 4 to Figure 7 show examples on how to configure the fader between the input ports and the outputs, separated into the composite (and S-video) encoder and the RGB encoder.

7.1.1.1 Configuration 1

Input MP_A can be faded into MP_B. The resulting output of the fader is then encoded simultaneously to composite (and S-video) and RGB output (RGBIN = ENCIN = 1). In this example, either MP_A or MP_B could be an overlay (menu) signal to be faded smoothly in and out.

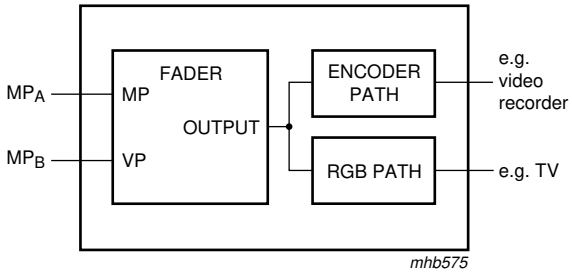

Fig 4. Configuration 1

7.1.1.2 Configuration 2

Input MP_A can be faded into MP_B. The resulting output of the fader is then encoded to RGB output, while the signal coming from MP_B is fed directly to composite (and S-video) output (RGBIN = 1, ENCIN = 0). Also in this example, either MP_A or MP_B could be an overlay (menu) signal to be faded smoothly in and out, whereas the overlay appears only in the RGB output connected to the TV set.

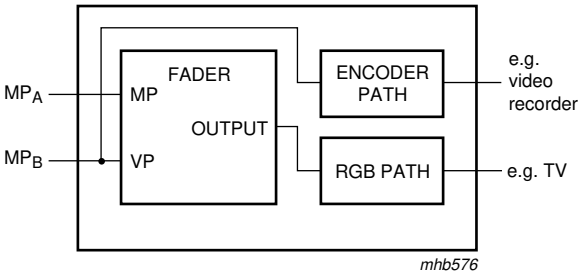

Fig 5. Configuration 2

7.1.1.3 Configuration 3

Input MP_B is passed directly to the RGB output, assuming e.g. it contains video including overlay. MP_A is equivalently passed through the inactive fader to the composite (and S-video) output, assuming e.g. it contains video excluding overlay (RGBIN = 0, ENCIN = 1).

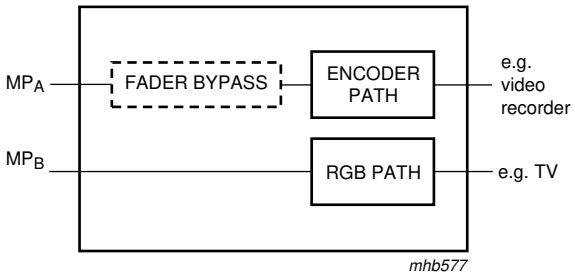

Fig 6. Configuration 3

7.1.1.4 Configuration 4

Only MP_B input is in use; its signal is both composite (and S-video) and RGB encoded (RGBIN = ENCIN = 0).

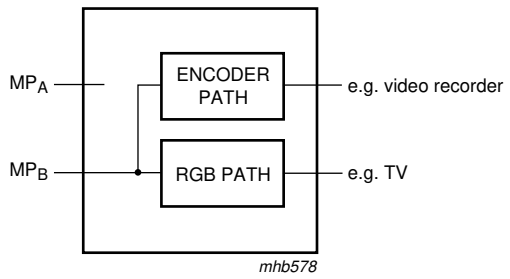

Fig 7. Configuration 4

7.1.2 Parameters of the fader

Basically, there are three independent fade factors available, allowing for the equation:

Output = (FADEx × In1) + [(1 − FADEx) × In2]

Where x = 1, 2 or 3.

Factor FADE1 is effective, when a color in the data stream fed to the MPEG port fader input is recognized as being between KEY1L and KEY1U. That means, the color is not identified by a single numeric value, but an upper and lower threshold in a 24-bit YUV color space can be defined. FADE1 = 00h results in 100 % signal at the MPEG port fader input and 0 % signal at the fader video port input. Variation of 63 steps is possible up to FADE1 = 3Fh, resulting in 0 % signal at the MPEG port fader input and 100 % signal at the fader video port input.

Factor FADE2 is effective, when a color in the data stream fed to the MPEG port fader input is recognized as being between KEY2L and KEY2U. FADE2 is to be seen in conjunction with a color that is defined by a 24-bit internal Color Look-Up Table (CLUT). FADE2 = 00h results in 100 % of the internally defined LUT color and 0 % signal at the fader video port input. Variation of 63 steps is possible up to FADE2 = 3Fh, resulting in 0 % of the internally defined LUT color and 100 % signal at the fader video port input.

Finally, factor FADE3 is effective, when a color in the data stream fed to the MPEG port fader input is recognized as neither being between KEY1L and KEY1U nor being between KEY2L and KEY2H. FADE3 = 00h results in 100 % signal at the MPEG port fader input and 0 % signal at the fader video port input. Variation of 63 steps is possible up to FADE3 = 3Fh, resulting in 0 % signal at the MPEG port fader input and 100 % signal at the fader video port input.

Optionally, all upper and lower thresholds can be ignored, enabling to fade signals only against the LUT color.

If bit CFADM is set HIGH, all data at the MPEG port fader are faded against the LUT color, if bit CFADV is set HIGH, all data at the video port fader are faded against the LUT color.

7.2 Data manager

In the data manager, a pre-defined color look-up table located in this block can be read out in a pre-defined sequence (8 steps per active video line) as an alternative to the external video data, achieving a color bar test pattern generator without the need for an external data source.

7.3 Encoder

7.3.1 Video path

The encoder generates out of Y, U and V baseband signals luminance and color subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process such as additional insertion of AGC super-white pulses (programmable in height) are supported by the SAA7128H only.

In order to enable easy post analog filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, providing luminance in 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figure 10 and Figure 11. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher color bandwidth, which can be made use of for Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figure 8 and Figure 9.

The amplitude, beginning and ending of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, color in a 10-bit resolution is provided on the subcarrier.

The numeric ratio between Y and C outputs is in accordance with the respective standards.

7.3.2 Teletext insertion and encoding

Pin TTX receives a WST or NABTS teletext bitstream sampled at the LLC clock. Two protocols are provided:

- At each rising edge of output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX
- The signal TTXRQ performs only a single LOW-to-HIGH transition and remains at HIGH-level for 360, 296 or 288 teletext bits, depending on the chosen standard.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which are selectable independently for both fields. The internal insertion window for text is set to 360 (PAL-WST), 296 (NTSC-WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Figure 23.

7.3.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

7.3.4 Closed caption encoder

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times horizontal line frequency.

7.3.5 Anti-taping (SAA7128H only)

For more information contact your nearest Philips Semiconductors sales office.

7.4 RGB processor

This block contains a dematrix in order to produce red, green and blue signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and color difference signals and 2 times oversampling for luminance and 4 times oversampling for color difference signals is performed. The transfer curves of luminance and color difference components of RGB are illustrated in Figure 12 and Figure 13 respectively.

7.5 SECAM processor

SECAM specific pre-processing is achieved by a pre-emphasis of color difference signals (for gain and phase see Figure 14 and Figure 15 respectively).

A baseband frequency modulator with a reference frequency shifted from 4.286 MHz to DC carries out SECAM modulation in accordance with appropriate standard or optional wide clipping limits.

After HF pre-emphasis, line-by-line sequential carriers with black reference of 4.25 MHz (Db) and 4.40625 MHz (Dr) are generated on a DC reference carrier (anti-Cloche filter; see Figure 16 and Figure 17) using specified values for FSC programming bytes.

Alternating phase reset in accordance with SECAM standard is carried out automatically. During vertical blanking, the so-called 'bottle pulses' are not provided.

7.6 Output interface/DACs

In the output interface, encoded Y and C signals are converted from digital-to-analog in a 10-bit resolution. Y and C signals are also combined in a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay (equal to 82 LLC clock periods, measured from MP input to the analog outputs) as the Y, C and RGB outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Red, green and blue signals are also converted from digital-to-analog, each providing a 9-bit resolution.

Outputs of the DACs can be set together via software control to minimum output voltage (approximately 0.2 V DC) for either purpose. Alternatively, the buffers can be switched into 3-state output condition; this allows for a 'wired AND' configuration with other 3-state outputs and can also be used as a power-save mode.

7.7 Synchronization

The synchronization of the SAA7128H; SAA7129H is able to operate in two modes; slave mode and master mode.

In master mode, see Figure 19, the circuit generates all necessary timings in the video signal itself, and it can provide timing signals at the RCV1 and RCV2 ports. In slave mode, it accepts timing information either from the RCV pins or from the embedded timing data of the *ITU-R BT.656* data stream.

For the SAA7128H; SAA7129H, the only difference between master and slave mode is that it ignores the timing information at its inputs in master mode. Thus, if in slave mode, any timing information is missing, the IC will continue running free without a visible effect. But there must not be any additional pulses (with wrong phase) because the circuit will not ignore them.

In slave mode, see Figure 18, an interface circuit decides which signal is expected at the RCV1 port and which information is taken from its active slope. The polarity can be chosen. If PRCV1 is logic 0, the rising slope will be active.

The signal can be:

- A Vertical Sync (VS) pulse; the active slope sets the vertical phase
- An odd/even signal; the active slope sets the vertical phase, the internal field flag to odd and optionally sets the horizontal phase
- A Field Sequence (FSEQ) signal; it marks the first field of the 4 (NTSC) or 8 (PAL) or 12 (SECAM) field sequences; in addition to the odd/even signal, it also sets the PAL phase and optionally defines the subcarrier phase.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The horizontal phase can be set via a separate input RCV2. In the event of VS pulses at RCV1, this is mandatory. It is also possible to set the signal path to blank via this input.

From the *ITU-R BT.656* data stream, the SAA7128H; SAA7129H decodes only the start of the first line in the odd field. All other information is ignored and may miss. If this kind of slave mode is active, the RCV pins may be switched to output mode.

In slave mode, the horizontal trigger phase can be programmed to any point in the line, the vertical phase from line 0 to line 15 counted from the first serration pulse in half line steps.

Whenever synchronization information cannot be derived directly from the inputs, the SAA7128H; SAA7129H will calculate it from the internal horizontal, vertical and PAL phase. This gives good flexibility with respect to external synchronization, but the circuit does not suppress illegal settings. In such an event, the odd/even information may vanish as it does in the non-interlaced modes.

In master mode, the line lengths are fixed to 1728 clocks at 50 Hz and 1716 clocks at 60 Hz. To allow non-interlaced frames, the field lengths can be varied by ±0.5 lines. In the event of non-interlace, the SAA7128H; SAA7129H does not provide odd/even information and the output signal does not contain the PAL ‘Bruch sequence’.

At the RCV1 pin the IC can provide:

- A Vertical Sync (VS) signal with 2.5 (50 Hz) or 3 (60 Hz) lines duration
- An odd/even signal which is LOW in odd fields
- A Field Sequence (FSEQ) signal which is HIGH in the first field of the 4 or 8 or 12 field sequences.

At the RCV2 pin, there is a horizontal pulse of programmable phase and duration available. This pulse can be suppressed in the programmable inactive part of a field, giving a composite blank signal.

The directions and polarities of the RCV ports can be chosen independently. Timing references can be found in Table 55 and Table 63.

7.8 Clock

The input to LLC1 can either be an external clock source or the buffered on-chip clock XCLK. The internal crystal oscillator can be run with either a 3rd-harmonic or a fundamental crystal frequency.

7.9 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbit/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and readable, except one read only status byte.

The I²C-bus slave address is defined as 88h with pin 21 (SA) tied LOW and as 8Ch with pin 21 (SA) tied HIGH.

7.10 Input levels and formats

The SAA7128H; SAA7129H expects digital Y, C_B and C_R data with levels (digital codes) in accordance with *ITU-R BT.601*.

For C and CVBS outputs, deviating amplitudes of the color difference signals can be compensated by an independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features a gain setting individually for luminance (GY) and color difference signals (GCD).

Reference levels are measured with a color bar, 100 % white, 100 % amplitude and 100 % saturation.

Table 4: *ITU-R BT.601* signal component levels

Color	Signals [1]					
	Y	C_B	C_R	R [2]	G [2]	B [2]
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

[1] Transformation:
$R = Y + 1.3707 \times (C_R - 128)$
$G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$
$B = Y + 1.7324 \times (C_B - 128)$.

[2] Representation of R, G and B (or C_R, Y and C_B) at the output is 9 bits at 27 MHz.

Table 5: 8-bit multiplexed format (similar to *ITU-R BT.601*)

Time	Bits							
	0	1	2	3	4	5	6	7
Sample	C_B0	Y0	C_R0	Y1	C_B2	Y2	C_R2	Y3
Luminance pixel number	0		1		2		3	
Color pixel number	0				2			

7.11 Bit allocation map

Table 6: Slave receiver (slave address 88h)

Register function	Subaddress	Data byte [1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte (read only)	00h	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E
Null	01h to 25h	0	0	0	0	0	0	0	0
Wide screen signal	26h	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27h	WSSON	0	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28h	DECCOL	DECFIS	BS5	BS4	BS3	BS2	BS1	BS0
Burst end	29h	0	0	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2Ah	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2Bh	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2Ch	CGEN	0	0	0	CG19	CG18	CG17	CG16
Output port control	2Dh	CVBSEN1	CVBSEN0	CVBSTRI	YTRI	CTRI	RTRI	GTRI	BTRI
Null	2Eh to 37h	0	0	0	0	0	0	0	0
Gain luminance for RGB	38h	0	0	0	GY4	GY3	GY2	GY1	GY0
Gain color difference for RGB	39h	0	0	0	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3Ah	CBENB	0	0	SYMP	DEMOFF	CSYNC	MP2C	VP2C
Key color 1 lower limit U	42h	KEY1LU7	KEY1LU6	KEY1LU5	KEY1LU4	KEY1LU3	KEY1LU2	KEY1LU1	KEY1LU0
Key color 1 lower limit V	43h	KEY1LV7	KEY1LV6	KEY1LV5	KEY1LV4	KEY1LV3	KEY1LV2	KEY1LV1	KEY1LV0
Key color 1 lower limit Y	44h	KEY1LY7	KEY1LY6	KEY1LY5	KEY1LY4	KEY1LY3	KEY1LY2	KEY1LY1	KEY1LY0
Key color 2 lower limit U	45h	KEY2LU7	KEY2LU6	KEY2LU5	KEY2LU4	KEY2LU3	KEY2LU2	KEY2LU1	KEY2LU0
Key color 2 lower limit V	46h	KEY2LV7	KEY2LV6	KEY2LV5	KEY2LV4	KEY2LV3	KEY2LV2	KEY2LV1	KEY2LV0
Key color 2 lower limit Y	47h	KEY2LY7	KEY2LY6	KEY2LY5	KEY2LY4	KEY2LY3	KEY2LY2	KEY2LY1	KEY2LY0
Key color 1 upper limit U	48h	KEY1UU7	KEY1UU6	KEY1UU5	KEY1UU4	KEY1UU3	KEY1UU2	KEY1UU1	KEY1UU0
Key color 1 upper limit V	49h	KEY1UV7	KEY1UV6	KEY1UV5	KEY1UV4	KEY1UV3	KEY1UV2	KEY1UV1	KEY1UV0
Key color 1 upper limit Y	4Ah	KEY1UY7	KEY1UY6	KEY1UY5	KEY1UY4	KEY1UY3	KEY1UY2	KEY1UY1	KEY1UY0
Key color 2 upper limit U	4Bh	KEY2UU7	KEY2UU6	KEY2UU5	KEY2UU4	KEY2UU3	KEY2UU2	KEY2UU1	KEY2UU0
Key color 2 upper limit V	4Ch	KEY2UV7	KEY2UV6	KEY2UV5	KEY2UV4	KEY2UV3	KEY2UV2	KEY2UV1	KEY2UV0
Key color 2 upper limit Y	4Dh	KEY2UY7	KEY2UY6	KEY2UY5	KEY2UY4	KEY2UY3	KEY2UY2	KEY2UY1	KEY2UY0
Fade factor key color 1	4Eh	0	0	FADE15	FADE14	FADE13	FADE12	FADE11	FADE10
CFade, Fade factor key color 2	4Fh	CFADEM	CFADEV	FADE25	FADE24	FADE23	FADE22	FADE21	FADE20

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Table 6: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress	Data byte [1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Fade factor other	50h	0	0	FADE35	FADE34	FADE33	FADE32	FADE31	FADE30
Look-up table key color 2 U	51h	LUTU7	LUTU6	LUTU5	LUTU4	LUTU3	LUTU2	LUTU1	LUTU0
Look-up table key color 2 V	52h	LUTV7	LUTV6	LUTV5	LUTV4	LUTV3	LUTV2	LUTV1	LUTV0
Look-up table key color 2 Y	53h	LUTY7	LUTY6	LUTY5	LUTY4	LUTY3	LUTY2	LUTY1	LUTY0
VPS enable, input control 2	54h	VPSEN	0	ENCIN	RGBIN	DELIN	VPSEL	EDGE2	EDGE1
VPS byte 5	55h	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56h	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57h	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58h	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59h	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5Ah	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5Bh	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5Ch	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, real-time control, black level	5Dh	GAINU8	DECOE	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, real-time control, blanking level	5Eh	GAINV8	DECPH	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5Fh	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60h	0	0	0	0	0	0	0	0
Standard control	61h	DOWNB	DOWNA	INPI	YGS	SECAM	SCBW	PAL	FISE
RTC enable, burst amplitude	62h	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63h	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64h	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65h	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66h	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67h	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68h	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69h	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6Ah	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
RCV port control	6Bh	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2

Table 6: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress	Data byte [1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Trigger control	6Ch	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6Dh	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6Eh	SBLBN	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLC0
Closed caption, teletext enable	6Fh	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV2 output start	70h	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71h	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72h	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
TTX request H start	73h	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request H delay	74h	TTXHD7	TTXHD6	TTXHD5	TTXHD4	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance, Vsync shift	75h	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	VS_S2	VS_S1	VS_S0
TTX odd request vertical start	76h	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77h	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request vertical start	78h	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request vertical end	79h	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7Ah	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7Bh	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7Ch	TTX60	LAL8	TTXO	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7Dh	0	0	0	0	0	0	0	0
Disable TTX line	7Eh	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7Fh	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13

[1] All bits labelled '0' are reserved. They must be programmed with logic 0.

7.12 I²C-bus format

Table 7: I²C-bus address; see Table 8

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 8: Explanation of Table 7

Part	Description
S	START condition
SLAVE ADDRESS	1000 100X or 1000 110X [1]
ACK	acknowledge, generated by the slave
SUBADDRESS [2]	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

[1] X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.

[2] If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

7.13 Slave receiver

Table 9: Subaddress 26h

Bit	Symbol	Description
7	WSS7	wide screen signalling bits: enhanced services field
6	WSS6	
5	WSS5	
4	WSS4	
3	WSS3	wide screen signalling bits: aspect ratio field
2	WSS2	
1	WSS1	
0	WSS0	

Table 10: Subaddress 27h

Bit	Symbol	Description
7	WSSON	0 = Wide screen signalling output is disabled; default state after reset, 1 = Wide screen signalling output is enabled.
6	-	this bit is reserved and must be set to logic 0
5	WSS13	wide screen signalling bits: reserved field
4	WSS12	
3	WSS11	
2	WSS10	wide screen signalling bits: subtitles field
1	WSS9	
0	WSS8	

Table 11: Subaddress 28h

Bit	Symbol	Description
7	DECCOL	0 = disable color detection bit of RTCI input, 1 = enable color detection bit of RTCI input; bit RTCE must be set to logic 1, see Figure 22
6	DECFIS	0 = field sequence as FISE in subaddress 61, 1 = field sequence as FISE bit in RTCI input; bit RTCE must be set to logic 1, see Figure 22
5	BS5	starting point of burst in clock cycles: PAL: BS[5:0] = 33 (21h); default value after reset NTSC: BS[5:0] = 25 (19h).
4	BS4	
3	BS3	
2	BS2	
1	BS1	
0	BS0	

Table 12: Subaddress 29h

Bit	Symbol	Description
7	-	these 2 bits are reserved; each must be set to logic 0
6	-	
5	BE5	ending point of burst in clock cycles: PAL: BE[5:0] = 29 (1Dh); default value after reset NTSC: BE[5:0] = 29 (1Dh).
4	BE4	
3	BE3	
2	BE2	
1	BE1	
0	BE0	

Table 13: Subaddress 2Ah

Bit	Symbol	Description
7 to 0	CG[07:00]	LSB of the byte is encoded immediately after run-in, the MSB of the byte has to carry the CRCC bit, in accordance with the definition of copy generation management system encoding format

Table 14: Subaddress 2Bh

Bit	Symbol	Description
7 to 0	CG[15:08]	second byte; the MSB of the byte has to carry the CRCC bit, in accordance with the definition of copy generation management system encoding format

Table 15: Subaddress 2Ch

Bit	Symbol	Description
7	CGEN	0 = copy generation data output is disabled; default state after reset, 1 = copy generation data output is enabled.
6	-	these 3 bits are reserved; each must be set to logic 0
5	-	
4	-	

Table 15: Subaddress 2Ch*...continued*

Bit	Symbol	Description
3	CG19	remaining bits of copy generation code
2	CG18	
1	CG17	
0	CG16	

Table 16: Subaddress 2Dh

Bit	Symbol	Description
7	CVBSEN1	0 = luminance output signal is switched to Y DAC; default state after reset, 1 = CVBS output signal is switched to Y DAC.
6	CVBSEN0	0 = chrominance output signal is switched to C DAC; default state after reset, 1 = CVBS output signal is switched to C DAC.
5	CVBSTRI	0 = DAC for CVBS output in 3-state mode (high-impedance), 1 = DAC for CVBS output in normal operation mode; default state after reset.
4	YTRI	0 = DAC for Y output in 3-state mode (high-impedance), 1 = DAC for Y output in normal operation mode; default state after reset.
3	CTRI	0 = DAC for C output in 3-state mode (high-impedance), 1 = DAC for C output in normal operation mode; default state after reset.
2	RTRI	0 = DAC for RED output in 3-state mode (high-impedance), 1 = DAC for RED output in normal operation mode; default state after reset.
1	GTRI	0 = DAC for GREEN output in 3-state mode (high-impedance), 1 = DAC for GREEN output in normal operation mode; default state after reset.
0	BTRI	0 = DAC for BLUE output in 3-state mode (high-impedance), 1 = DAC for BLUE output in normal operation mode; default state after reset.

Table 17: Subaddress 38h

Bit	Symbol	Description
7 to 5	-	these 3 bits are reserved; each must be set to logic 0
4 to 0	GY[4:0]	gain luminance of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$; suggested nominal value = –6 (11010b), depending on external application

Table 18: Subaddress 39h

Bit	Symbol	Description
7 to 5	-	these 3 bits are reserved; each must be set to logic 0
4 to 0	GCD[4:0]	gain color difference of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$; suggested nominal value = –6 (11010b), depending on external application

Table 19: Subaddress 3Ah

Bit	Symbol	Description
7	CBENB	0 = data from input ports is encoded; default state after reset, 1 = color bar with fixed colors is encoded.
6	-	these 2 bits are reserved; each must be set to a logic 0
5	-	
4	SYMP	0 = horizontal and vertical trigger is taken from RCV2 and RCV1, respectively; default state after reset, 1 = horizontal and vertical trigger is decoded out of *ITU-R BT.656* compatible data at MPEG port.
3	DEMOFF	0 = YC_BC_R-to-RGB dematrix is active; default state after reset, 1 = YC_BC_R-to-RGB dematrix is bypassed.
2	CSYNC	0 = CVBS output signal is switched to CVBS DAC; default state after reset, 1 = advanced composite sync is switched to CVBS DAC.
1	MP2C	0 = input data is twos complement from MPEG port fader input, 1 = input data is straight binary from MPEG port fader input; default state after reset.
0	VP2C	0 = input data is twos complement from video port fader input, 1 = input data is straight binary from video port fader input; default state after reset.

Table 20: Subaddresses 42h to 44h and 48h to 4Ah

Address	Byte	Description
42h, 48h	KEY1LU[7:0] KEY1UU[7:0]	Key color 1 lower and upper limits for U, V and Y; if MPEG input signal is within the limits of key color 1 the incoming signals at the video port and MPEG port are added together according to the equation: FADE1 × video signal + (1 − FADE1) × MPEG signal Default value of all bytes after reset = 80h.
43h, 49h	KEY1LV[7:0] KEY1UV[7:0]	
44h, 4Ah	KEY1LY[7:0] KEY1UY[7:0]	

Table 21: Subaddresses 45h to 47h and 4Bh to 4Dh

Address	Byte	Description
45h, 4Bh	KEY2LU[7:0] KEY2UU[7:0]	Key color 2 lower and upper limits for U, V and Y; if MPEG input signal is within the limits of key color 2 the incoming signals at the video port and MPEG port are added together according to the equation: FADE2 × video signal + (1 − FADE2) × LUT values Default value of all bytes after reset = 80h.
46h, 4Ch	KEY2LV[7:0] KEY2UV[7:0]	
47h, 4Dh	KEY2LY[7:0] KEY2UY[7:0]	

Table 22: Subaddress 4Eh

Bit	Symbol	Description
7 to 6	-	these 2 bits are reserved; each must be set to logic 0
5 to 0	FADE1[5:0]	these 6 bits form factor FADE1 which determines the ratio between the MPEG and video input signal in the resulting video data stream if the key color 1 is detected in the MPEG input signal: FADE1 = 00h: 100 % MPEG, 0 % video FADE1 = 3Fh: 100 % video, 0 % MPEG; default value after reset.

Table 23: Subaddress 4Fh

Bit	Symbol	Description
7	CFADEM	0 = fader operates in normal mode; default state after reset, 1 = the entire video input stream is faded with the color stored in the LUT (subaddresses 51h to 53h) regardless of the MPEG input signal; the color keys are disabled.
6	CFADEV	0 = fader operates in normal mode; default state after reset, 1 = the entire MPEG input stream is faded with the color stored in the LUT (subaddresses 51h to 53h) regardless of the video input signal; the color keys are disabled.
5 to 0	FADE2[5:0]	these 6 bits form factor FADE2 which determines the ratio between the LUT color values (subaddresses 51h to 53h) and the video input signal in the resulting video data stream if the key color 2 is detected in the MPEG input signal: FADE2 = 00h: 100 % LUT color, 0 % video FADE2 = 3Fh: 100 % video, 0 % LUT color; default value after reset.

Table 24: Subaddress 50h

Bit	Symbol	Description
7 to 6	-	these 2 bits are reserved; each must be a logic 0
5 to 0	FADE3[5:0]	these 6 bits form factor FADE3 which determines the ratio between the MPEG and video input signal in the resulting video data stream if neither the key color 1 nor the key color 2 is detected in the MPEG input signal: FADE3 = 00h: 100 % MPEG, 0 % video FADE3 = 3Fh: 100 % video, 0 % MPEG; default value after reset.

Table 25: Subaddress 51h

Bit	Symbol	Description
7 to 0	LUTU[7:0]	LUT for the color values inserted in case of key color 2 U detection in the MPEG input data stream; LUTU[7:0] = 80h; default value after reset

Table 26: Subaddress 52h

Bit	Symbol	Description
7 to 0	LUTV[7:0]	LUT for the color values inserted in case of key color 2 V detection in the MPEG input data stream; LUTV[7:0] = 80h; default value after reset

Table 27: Subaddress 53h

Bit	Symbol	Description
7 to 0	LUTY[7:0]	LUT for the color values inserted in case of key color 2 Y detection in the MPEG input data stream; LUTY[7:0] = 80h; default value after reset

Table 28: Subaddress 54h

Bit	Symbol	Description
7	VPSEN	0 = video programming system data insertion is disabled; default state after reset, 1 = video programming system data insertion in line 16 is enabled.
6	-	this bit is not used and should be set to logic 0
5	ENCIN	0 = encoder path is fed with MP_B input data; fader is bypassed; default state after reset, 1 = encoder path is fed with output signal of fader; see Section 7.1.
4	RGBIN	0 = RGB path is fed with MP_B input data; fader is bypassed; default state after reset, 1 = RGB path is fed with output signal of fader; see Section 7.1.
3	DELIN	0 = not supported in current version; do not use, 1 = recommended value; default state after reset.
2	VPSEL	0 = not supported in current version; do not use, 1 = recommended value; default state after reset.
1	EDGE2	0 = MP_B data is sampled on the rising clock edge; default state after reset, 1 = MP_B data is sampled on the falling clock edge.
0	EDGE1	0 = MP_A data is sampled on the rising clock edge; default state after reset, 1 = MP_A data is sampled on the falling clock edge.

Table 29: Subaddress 55h

Bit	Symbol	Description
7 to 0	VPS5[7:0]	fifth byte of video programming system data in line 16; LSB first

Table 30: Subaddress 56h

Bit	Symbol	Description
7 to 0	VPS11[7:0]	eleventh byte of video programming system data in line 16; LSB first

Table 31: Subaddress 57h

Bit	Symbol	Description
7 to 0	VPS12[7:0]	twelfth byte of video programming system data in line 16; LSB first

Table 32: Subaddress 58h

Bit	Symbol	Description
7 to 0	VPS13[7:0]	thirteenth byte of video programming system data in line 16; LSB first

Table 33: Subaddress 59h

Bit	Symbol	Description
7 to 0	VPS14[7:0]	fourteenth byte of video programming system data in line 16; LSB first

Table 34: Subaddress 5Ah

Bit	Symbol	Description
7 to 0	CHPS[7:0]	phase of encoded color subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees: 0Fh = PAL-B/G and data from input ports 3Ah = PAL-B/G and data from look-up table 35h = NTSC-M and data from input ports 57h = NTSC-M and data from look-up table.

Table 35: Subaddress 5Bh

Bit	Symbol	Description
7 to 0	GAINU[7:0]	these are the 8 LSBs of the 9-bit code that selects the variable gain for the C_B signal; input representation in accordance with *ITU-R BT.601*; see Table 36; the MSB is held in subaddress 5Dh; see Table 39

Table 36: GAINU values

Conditions [1]	Encoding
White-to-black = 92.5 IRE	GAINU = −2.17 × nominal to +2.16 × nominal
GAINU[8:0] = 0	output subcarrier of U contribution = 0
GAINU[8:0] = 118 (76h)	output subcarrier of U contribution = nominal
White-to-black = 100 IRE	GAINU = −2.05 × nominal to +2.04 × nominal
GAINU[8:0] = 0	output subcarrier of U contribution = 0
GAINU[8:0] = 125 (7Dh)	output subcarrier of U contribution = nominal
GAINU[8:0] = 106 (6Ah)	nominal GAINU for SECAM encoding

[1] All IRE values are rounded up.

Table 37: Subaddress 5Ch

Bit	Symbol	Description
7 to 0	GAINV[7:0]	these are the 8 LSBs of the 9-bit code that selects the variable gain for the C_R signal; input representation in accordance with *ITU-R BT.601*; see Table 38; the MSB is held in subaddress 5Eh; see Table 41

Table 38: GAINV values

Conditions [1]	Encoding
White-to-black = 92.5 IRE	GAINV = −1.55 × nominal to +1.55 × nominal
GAINV[8:0] = 0	output subcarrier of V contribution = 0
GAINV[8:0] = 165 (A5h)	output subcarrier of V contribution = nominal
White-to-black = 100 IRE	GAINV = −1.46 × nominal to +1.46 × nominal
GAINV[8:0] = 0	output subcarrier of V contribution = 0
GAINV[8:0] = 175 (AFh)	output subcarrier of V contribution = nominal

Table 38: GAINV values *...continued*

Conditions [1]	Encoding
GAINV[8:0] = 129 (81h)	nominal GAINV for SECAM encoding

[1] All IRE values are rounded up.

Table 39: Subaddress 5Dh

Bit	Symbol	Description
7	GAINU8	MSB of the 9-bit code that sets the variable gain for the C_B signal; see Table 35.
6	DECOE	real-time control: 0 = disable odd/even field control bit from RTCI 1 = enable odd/even field control bit from RTCI; see Figure 22.
5 to 0	BLCKL[5:0]	variable black level; input representation in accordance with *ITU-R BT.601*; see Table 40

Table 40: BLCKL values

Conditions [1]	Encoding [1]
White-to-sync = 140 IRE [2]	recommended value: BLCKL = 58 (3Ah)
BLCKL = 0 [2]	output black level = 29 IRE
BLCKL = 63 (3Fh) [2]	output black level = 49 IRE
White-to-sync = 143 IRE [3]	recommended value: BLCKL = 51 (33h)
BLCKL = 0 [3]	output black level = 27 IRE
BLCKL = 63 (3Fh) [3]	output black level = 47 IRE

[1] All IRE values are rounded up.

[2] Output black level/IRE = BLCKL × 2/6.29 + 28.9.

[3] Output black level/IRE = BLCKL × 2/6.18 + 26.5.

Table 41: Subaddress 5Eh

Bit	Symbol	Description
7	GAINV8	MSB of the 9-bit code that sets the variable gain for the C_R signal; see Table 37.
6	DECPH	real-time control: 0 = disable subcarrier phase reset bit from RTCI 1 = enable subcarrier phase reset bit from RTCI; see Figure 22.
5 to 0	BLNNL[5:0]	variable blanking level; see Table 42

Table 42: BLNNL values

Conditions [1]	Encoding [1]
White-to-sync = 140 IRE [2]	recommended value: BLNNL = 46 (2Eh)
BLNNL = 0 [2]	output blanking level = 25 IRE
BLNNL = 63 (3Fh) [2]	output blanking level = 45 IRE
White-to-sync = 143 IRE [3]	recommended value: BLNNL = 53 (35h)
BLNNL = 0 [3]	output blanking level = 26 IRE