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# DATA SHEET



# SAA7324
# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

Product specification
Supersedes data of 1999 May 17
File under Integrated Circuits, IC01

2000 Jun 26

Philips
Semiconductors

PHILIPS

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

# SAA7324

**CONTENTS**

# Digital servo processor and Compact Disc decoder with integrated DAC (CD10 II)

SAA7324

## 1 FEATURES

- Integrated bitstream DAC with differential outputs, operating at $96f_s$ with 3rd-order noise shaper; typical performance of –90 dB signal-to-noise ratio
- Separate serial input and output interfaces allow data 'loopback' mode for use of onboard DAC with external Electronic Shock Absorption (ESA) systems
- Up to 4 times speed mode
- Low voltage operation at up to 2 times speed
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- Two and four times oversampling integrated digital filter, including $f_s$ mode
- Audio data peak level detection
- Kill interface for external DAC deactivation during digital silence
- All SAA737x (CD7) digital servo and high-level functions
- Low focus noise
- Same playability performance as SAA737x (CD7)
- Automatic closed-loop gain control available for focus and radial loops
- Pulsed sledge support

ReWritable CD COMPATIBLE

I²C BUS

- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I²C-bus
- On-chip clock multiplier allows the use of 8.4672, 16.9344 or 33.8688 MHz crystals or ceramic resonators.

## 2 GENERAL DESCRIPTION

The SAA7324 (CD10 II) is a single chip combining the functions of a CD decoder, digital servo and bitstream DAC. The decoder/servo part is based on the SAA737x (CD7) and is software compatible with this design. Extra functions are controlled by use of 'shadow' registers (see Section 7.15.3).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

## 3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| SAA7324H | QFP64 | plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm | SOT393-1 |

## 4 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | n = 4 mode; note 1 | 3.0 | 3.3 | 3.6 | V |
| | | n = 1 or 2 mode; note 1 | 2.4 | – | 3.6 | V |
| $I_{DD}$ | supply current | $V_{DD}$ = 3.3 V | – | 20 | – | mA |
| | | $V_{DD}$ = 2.4 V | – | 14 | – | mA |
| $f_{xtal}$ | crystal frequency | | 4 | 8.4672 | 35 | MHz |
| $T_{amb}$ | ambient temperature | | –10 | – | +70 | °C |
| $T_{stg}$ | storage temperature | | –55 | – | +125 | °C |
| $S/N_{DAC}$ | onboard DAC signal-to-noise ratio | 1 kHz; 1$f_s$; see Figs 38 and 39 | –85 | –90 | – | dB |

**Note**

1. n = overspeed factor.

## 5 BLOCK DIAGRAM

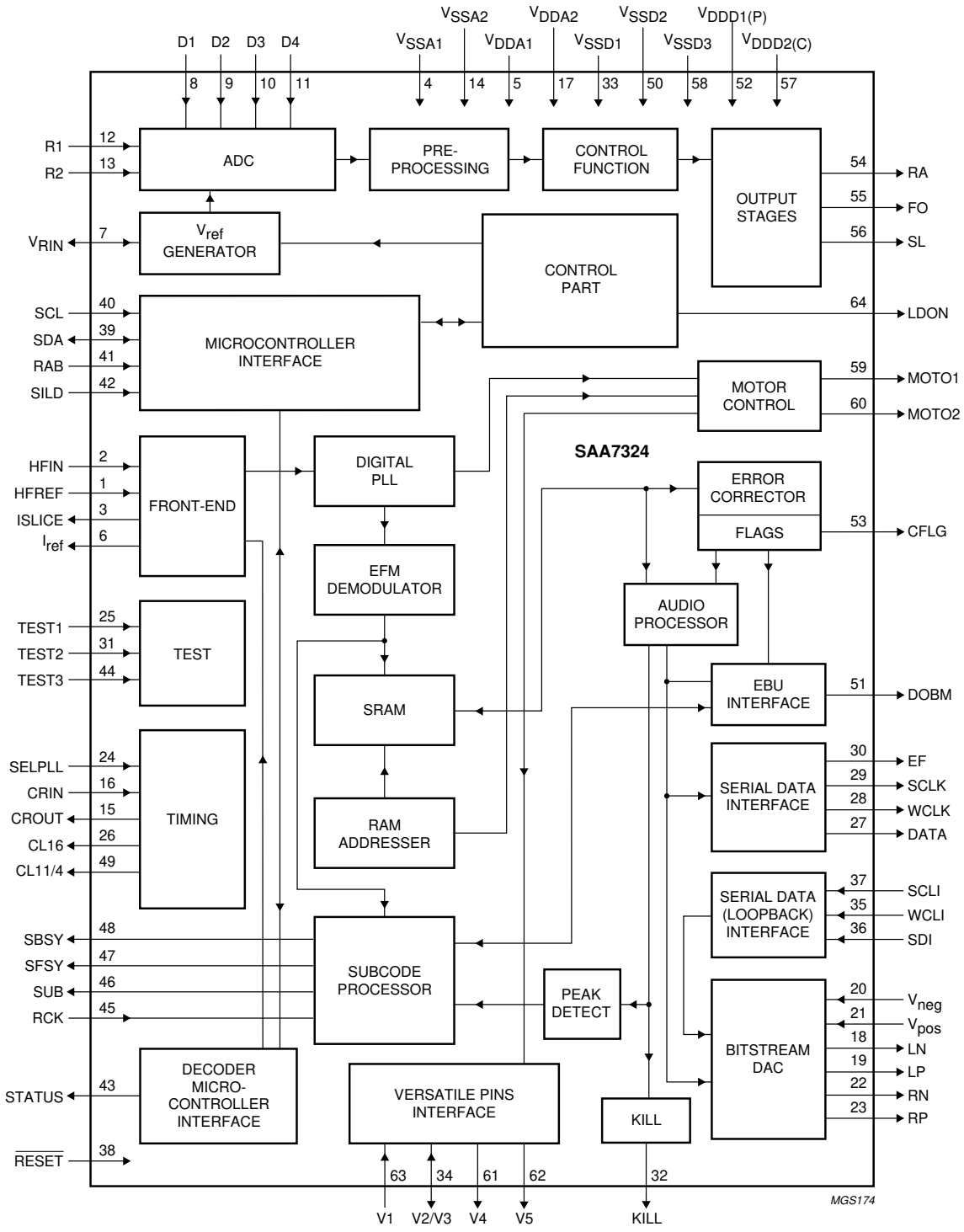



Fig.1 Block diagram.

## 6 PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| HFREF | 1 | comparator common mode input |
| HFIN | 2 | comparator signal input |
| ISLICE | 3 | current feedback output from data slicer |
| $V_{SSA1}$ | 4(1) | analog ground 1 |
| $V_{DDA1}$ | 5(1) | analog supply voltage 1 |
| $I_{ref}$ | 6 | reference current output |
| $V_{RIN}$ | 7 | reference voltage for servo ADCs |
| D1 | 8 | unipolar current input 1 (central diode signal input) |
| D2 | 9 | unipolar current input 2 (central diode signal input) |
| D3 | 10 | unipolar current input 3 (central diode signal input) |
| D4 | 11 | unipolar current input 4 (central diode signal input) |
| R1 | 12 | unipolar current input 1 (satellite diode signal input) |
| R2 | 13 | unipolar current input 2 (satellite diode signal input) |
| $V_{SSA2}$ | 14(1) | analog ground 2 |
| CROUT | 15 | crystal/resonator output |
| CRIN | 16 | crystal/resonator input |
| $V_{DDA2}$ | 17(1) | analog supply voltage 2 |
| LN | 18 | DAC left channel differential negative output |
| LP | 19 | DAC left channel differential positive output |
| $V_{neg}$ | 20 | DAC negative reference input |
| $V_{pos}$ | 21 | DAC positive reference input |
| RN | 22 | DAC right channel differential negative output |
| RP | 23 | DAC right channel differential positive output |
| SELPLL | 24 | selects whether internal clock multiplier PLL is used |
| TEST1 | 25 | test control input 1 (this pin should be tied LOW) |
| CL16 | 26 | 16.9344 MHz system clock output |
| DATA | 27 | serial d4(1) data output (3-state) |
| WCLK | 28 | word clock output (3-state) |
| SCLK | 29 | serial bit clock output (3-state) |
| EF | 30 | C2 error flag output (3-state) |
| TEST2 | 31 | test control input 2 (this pin should be tied LOW) |
| KILL | 32 | kill output (programmable; open-drain) |
| $V_{SSD1}$ | 33(1) | digital ground 1 |
| V2/V3 | 34 | versatile I/O: versatile input 2 or versatile output 3 (open-drain) |
| WCLI | 35 | word clock input (for data loopback to DAC) |
| SDI | 36 | serial data input (for data loopback to DAC) |
| SCLI | 37 | serial bit clock input (for data loopback to DAC) |
| $\overline{RESET}$ | 38 | power-on reset input (active LOW) |
| SDA | 39 | microcontroller interface data I/O line ($I^2C$-bus; open-drain output) |
| SCL | 40 | microcontroller interface clock line input ($I^2C$-bus) |

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| RAB | 41 | microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode) |
| SILD | 42 | microcontroller interface $\overline{R}$/W and load control line input (4-wire bus mode) |
| STATUS | 43 | servo interrupt request line/decoder status register output (open-drain) |
| TEST3 | 44 | test control input 3 (this pin should be tied LOW) |
| RCK | 45 | subcode clock input |
| SUB | 46 | P-to-W subcode bit 3-states output (3-state) |
| SFSY | 47 | subcode frame sync output (3-state) |
| SBSY | 48 | subcode block sync output (3-state) |
| CL11/4 | 49 | 11.2896 or 4.2336 MHz (for microcontroller) clock output |
| $V_{SSD2}$ | 50(1) | digital ground 2 |
| DOBM | 51 | bi-phase mark output (externally buffered; 3-state) |
| $V_{DDD1(P)}$ | 52(1) | digital supply voltage 1 for periphery |
| CFLG | 53 | correction flag output (open-drain) |
| RA | 54 | radial actuator output |
| FO | 55 | focus actuator output |
| SL | 56 | sledge control output |
| $V_{DDD2(C)}$ | 57(1) | digital supply voltage 2 for core |
| $V_{SSD3}$ | 58(1) | digital ground 3 |
| MOTO1 | 59 | motor output 1; versatile (3-state) |
| MOTO2 | 60 | motor output 2; versatile (3-state) |
| V4 | 61 | versatile output 4 |
| V5 | 62 | versatile output 5 |
| V1 | 63 | versatile input 1 |
| LDON | 64 | laser drive on output (open-drain) |

**Note**

1. All supply pins must be connected to the same external power supply voltage.

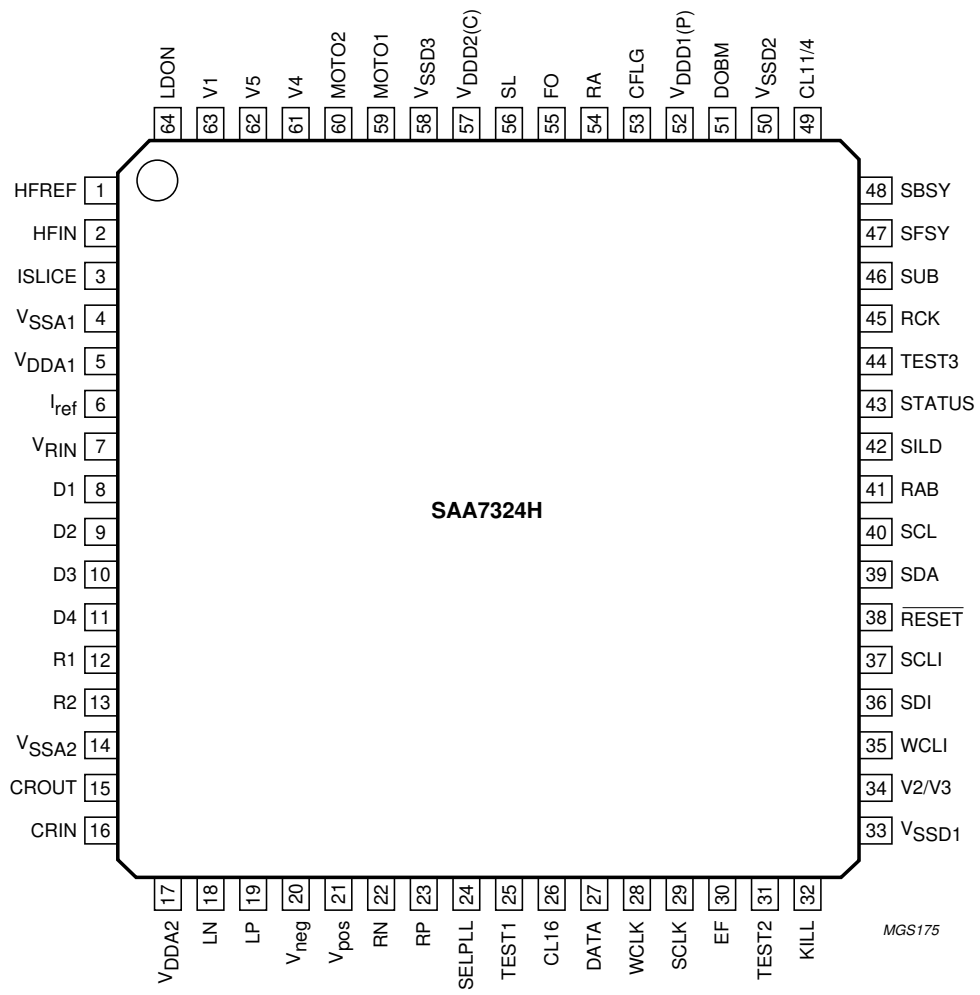



Fig.2 Pin configuration.

## 7 FUNCTIONAL DESCRIPTION

### 7.1 Decoder part

#### 7.1.1 PRINCIPAL OPERATING MODES OF THE DECODER

The decoding part supports a full audio specification and can operate at two different disc speeds, from single-speed (n = 1) to 4 times speed (n = 4). The factor ‘n’ is called the overspeed factor. A simplified data flow through the decoder part is illustrated in Fig.7.

#### 7.1.2 DECODING SPEED AND CRYSTAL FREQUENCY

The SAA7324 is a two speed decoding device, with an internal Phase-Locked Loop (PLL) clock multiplier. Depending on the crystal frequency used and the internal clock settings (selectable via decoder register B), the playback speeds shown in Table 1 are possible, where ‘n’ is the overspeed factor (1, 2 or 4).

An internal clock multiplier is present, controlled by SELPLL, and should only be used if a 8.4672 or 16.9344 MHz crystal, ceramic resonator or external clock is present.

### 7.1.3 LOCK-TO-DISC MODE

For electronic shock absorption applications, the SAA7324 can be put into lock-to-disc mode. This allows Constant Angular Velocity (CAV) disc playback with varying input data rates from the inside-to-outside of the disc.

In the lock-to-disc mode, the FIFO is blocked and the decoder will adjust its output data rate to the disc speed. Hence, the frequency of the I²S-bus (WCLK and SCLK) clocks are dependent on the disc speed. In the lock-to-disc mode there is a limit on the maximum variation in disc speed that the SAA7324 will follow. Disc speeds must always be within 25% to 100% range of their nominal value. The lock-to-disc mode is enabled/disabled by decoder register E.

### 7.1.4 STANDBY MODES

The SAA7324 may be placed in two standby modes selected by decoder register B (it should be noted that the device core is still active):

- Standby 1: CD-STOP mode; most I/O functions are switched off
- Standby 2: CD-PAUSE mode; audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active; this is also called a ‘Hot Pause’.

In the standby modes the various pins will have the following values:

- MOTO1 and MOTO2: put in high-impedance, PWM mode (standby 1 and reset: operating in standby 2); put in high-impedance, PDM mode (standby 1 and reset: operating in standby 2)
- SCL and SDA: no interaction; normal operation continues
- SCLK, WCLK, DATA, EF and DOBM: 3-state in both standby modes; normal operation continues after reset
- CRIN, CROUT, CL16 and CL11/4: no interaction; normal operation continues
- V1, V2/V3, V4, V5 and CFLG: no interaction; normal operation continues.

**Table 1** Playback speeds

| REGISTER B | REGISTER E | SELPLL | CRYSTAL FREQUENCY (MHz) | | | CL11 FREQUENCY (MHz)[1] |
|---|---|---|---|---|---|---|
| | | | 33.8688 | 16.9344 | 8.4672 | |
| 00XX | 0XXX | 0 | n = 1 | – | – | 11.2896 |
| 00XX | 0XXX | 1 | – | – | n = 1 | 11.2896 |
| 01XX | 0XXX | 0 | – | n = 1 | – | 5.6448 |
| 01XX | 0XXX | 1 | – | n = 1 | – | 11.2896 |
| 10XX | 0XXX | 0 | n = 2 | – | – | 11.2896 |
| 10XX | 0XXX | 1 | – | – | n = 2 | 11.2896 |
| 11XX | 0XXX | 0 | – | n = 2[2] | – | 5.6448 |
| 11XX | 0XXX | 1 | – | n = 2 | – | 11.2896 |
| 00XX | 1XXX | 0 | n = 4[2] | – | – | 11.2896 |
| 00XX | 1XXX | 1 | – | – | n = 4 | 11.2896 |
| 01XX | 1XXX | 0 | – | n = 4[2] | – | 5.6448 |
| 01XX | 1XXX | 1 | – | n = 4 | – | 11.2896 |

**Notes**

1. The CL11 output is always a 5.6448 MHz clock if a 16.9344 MHz external clock is used and SELPLL = 0. CL11 is available on the CL11/4 output, enabled by programming shadow register 3 (see Section 7.15.3).
2. Data capture performance is not optimized for this option.

### 7.2 Crystal oscillator

The crystal oscillator is a conventional 2-pin design operating between 8 and 35 MHz. This oscillator is capable of operating with ceramic resonators and with both fundamental and third overtone crystals. External components should be used to suppress the fundamental output of the third overtone crystals as shown in Figs 3 and 4. Typical oscillation frequencies required are 8.4672, 16.9344 or 33.8688 MHz depending on the internal clock settings used and whether or not the clock multiplier is enabled.

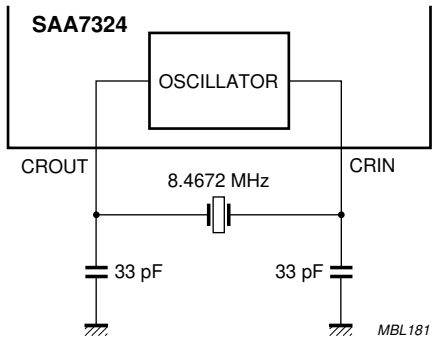



Fig.3 8.4672 MHz fundamental configuration.

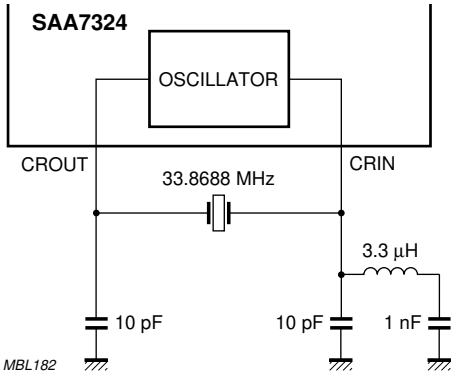


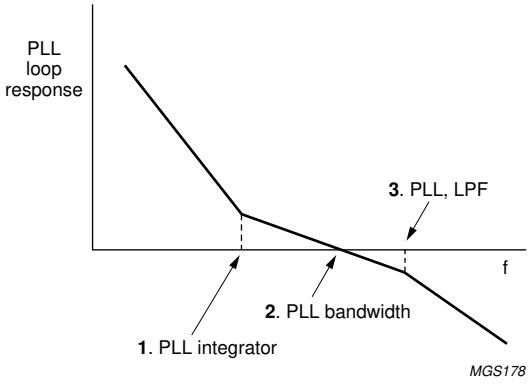

Fig.4 33.8688 MHz overtone configuration.

### 7.3 Data slicer and clock regenerator

The SAA7324 has an integrated slice level comparator which can be clocked by the crystal frequency clock, or 4 times the crystal frequency clock (if SELPLL is set HIGH while using a 16.9344 MHz crystal and register 4 is set to 0XXX), or 8 times the crystal frequency clock (if SELPLL is set HIGH while using an 8.4672 MHz crystal, and register 4 is set to 0XXX). The slice level is controlled by an internal current source applied to an external capacitor under the control of the Digital Phase-Locked Loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization. The PLL response is shown in Fig.5.

For certain applications an off-track input is necessary. This is internally connected from the servo part (its polarity can be changed by the foc_parm1 parameter), but may be input via the V1 pin if selected by register C. If this flag is HIGH, the SAA7324 will assume that its servo part is following on the wrong track, and will flag all incoming HF data as incorrect.




1, 2 and 3 are all programmable via decoder register 8.

Fig.5 Digital PLL loop response.

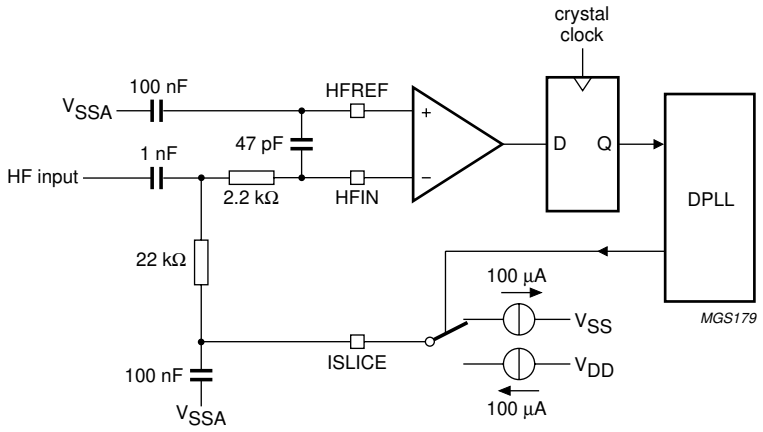



Fig.6 Data slicer showing typical application components (for n = 1).

### 7.4 Demodulator

#### 7.4.1 Frame sync protection

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data.
The master counter is only reset if:

- A sync coincidence is detected; sync pattern occurs 588 ±1 EFM clocks after the previous sync pattern
- A new sync pattern is detected within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active HIGH after 1 sync coincidence is found, and reset LOW if during 61 consecutive frames no sync coincidence is found. The PLL lock signal can be accessed via the SDA or STATUS pins selected by decoder registers 2 and 7.

Also incorporated in the demodulator is a Run Length 2 (RL2) correction circuit. Every symbol detected as RL2 will be pushed back to RL3. To do this, the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

#### 7.4.2 EFM demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

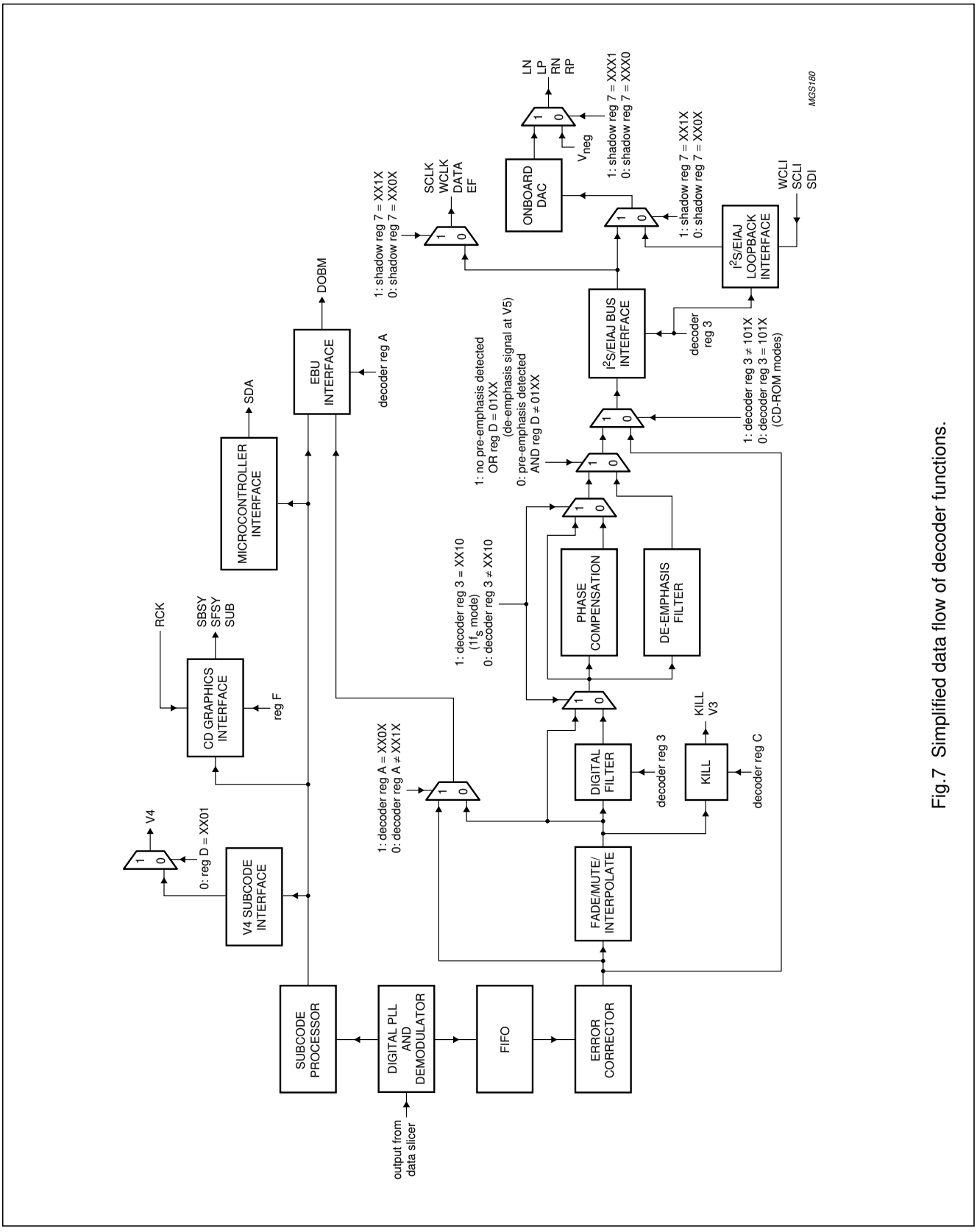



Fig.7 Simplified data flow of decoder functions.

### 7.5 Subcode data processing

#### 7.5.1 Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the SDA or STATUS pins, selected via decoder register 2. Good Q-channel data may be read from SDA.

#### 7.5.2 EIAJ 3 AND 4-WIRE SUBCODE (CD GRAPHICS) INTERFACES

Data from all the subcode channels (P-to-W) may be read via the subcode interface, which conforms to EIAJ CP-2401. The interface is enabled and configured as either a 3 or 4-wire interface via decoder register F.

The subcode interface output formats are illustrated in Fig.8, where the RCK signal is supplied by another device such as a CD graphics decoder.

#### 7.5.3 V4 SUBCODE INTERFACE

Data of subcode channels, Q-to-W, may be read via pin V4 if selected via decoder register D. The format is similar to RS232 and is illustrated in Fig.9. The subcode sync word is formed by a pause of (200/n) μs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between (11.3/n) μs and (90/n) μs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

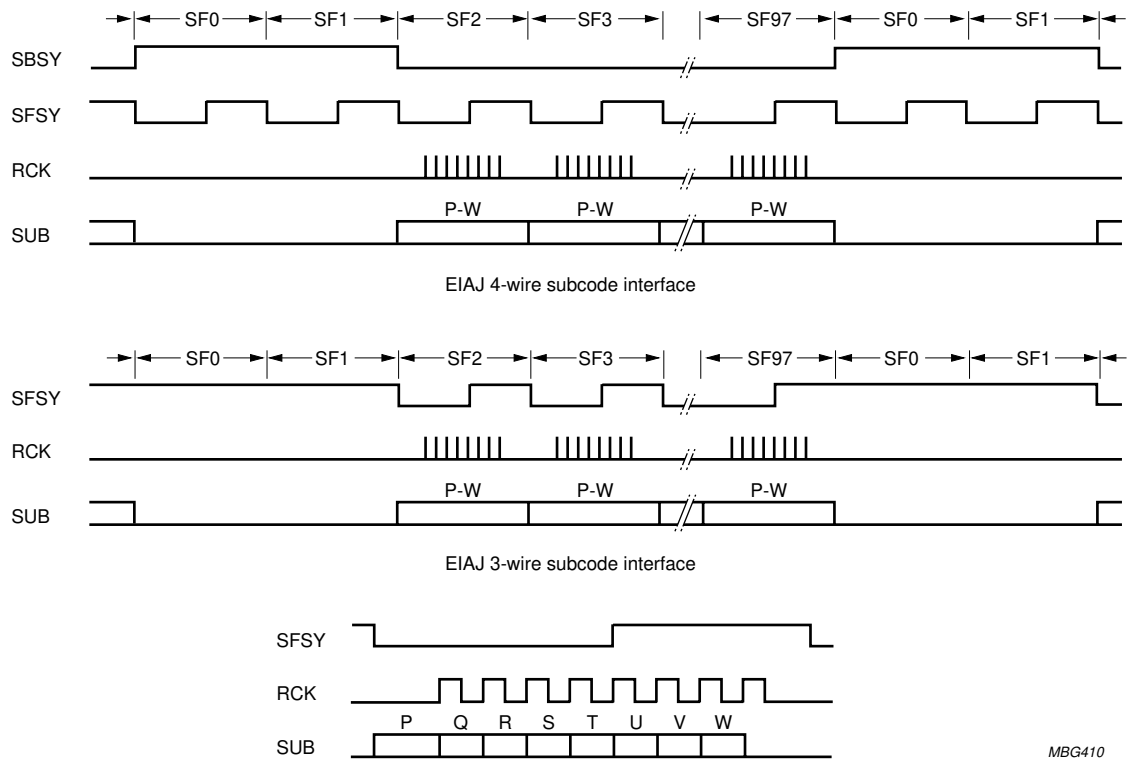
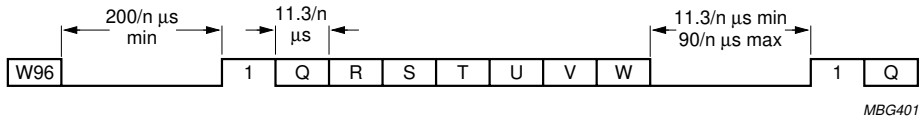



Fig.8 EIAJ subcode (CD graphics) interface format.




n = disc speed.

Fig.9 Subcode format and timing on pin V4.

### 7.6 FIFO and error corrector

The SAA7324 has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.

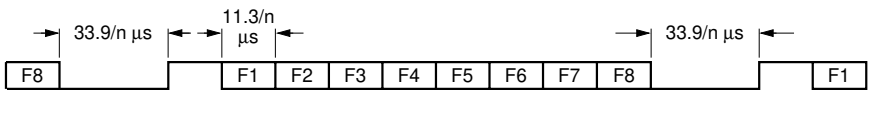
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after (de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM). The EF output will flag bytes in error in both audio and CD-ROM modes.

#### 7.6.1 FLAGS OUTPUT (CFLG)

The flags output pin CFLG shows the status of the error corrector and interpolator and is updated every frame (7.35 × n kHz). In the SAA7324 chip a 1-bit flag is present on the CFLG pin as illustrated in Fig.10. This signal shows the status of the error corrector and interpolator.

The first flag bit, F1, is the absolute time sync signal, the FIFO-passed subcode sync and relates the position of the subcode sync to the audio data (DAC output). This flag may also be used in a super FIFO or in the synchronization of different players. The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by decoder register A.




n = disc speed.

Fig.10 Flag output timing diagram.

**Table 2** Output flags

| F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | X | X | no absolute time sync |
| 1 | X | X | X | X | X | X | X | absolute time sync |
| X | 0 | 0 | X | X | X | X | X | C1 frame contained no errors |
| X | 0 | 1 | X | X | X | X | X | C1 frame contained 1 error |
| X | 1 | 0 | X | X | X | X | X | C1 frame contained 2 errors |
| X | 1 | 1 | X | X | X | X | X | C1 frame uncorrectable |
| X | X | X | 0 | 0 | X | X | 0 | C2 frame contained no errors |
| X | X | X | 0 | 0 | X | X | 1 | C2 frame contained 1 error |
| X | X | X | 0 | 1 | X | X | 0 | C2 frame contained 2 errors |
| X | X | X | 0 | 1 | X | X | 1 | C2 frame contained 3 errors |
| X | X | X | 1 | 0 | X | X | 0 | C2 frame contained 4 errors |
| X | X | X | 1 | 1 | X | X | 1 | C2 frame uncorrectable |
| X | X | X | X | X | 0 | 0 | X | no interpolations |
| X | X | X | X | X | 0 | 1 | X | at least one 1-sample interpolation |
| X | X | X | X | X | 1 | 0 | X | at least one hold and no interpolations |
| X | X | X | X | X | 1 | 1 | X | at least one hold and one 1-sample interpolation |

## 7.7 Audio functions

### 7.7.1 De-emphasis and phase linearity

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase of the digital oversampling filter to $\leq \pm 1°$ within the band 0 to 16 kHz. With de-emphasis the filter is not phase linear.

If the de-emphasis signal is set to be available at V5, selected via decoder register D, then the de-emphasis filter is bypassed.

### 7.7.2 Digital oversampling filter

For optimizing performance with an external DAC, the SAA7324 contains a 2 to 4 times oversampling IIR filter. The filter specification of the 4 times oversampling filter is given in Table 3.

These attenuations do not include the sample-and-hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled −0.5 dB down to avoid overflow on full-scale sine wave inputs (0 to 20 kHz).

**Table 3** Filter specification

| PASS BAND | STOP BAND | ATTENUATION |
|---|---|---|
| 0 to 9 kHz | – | ≤0.001 dB |
| 19 to 20 kHz | – | ≤0.03 dB |
| – | 24 kHz | ≥25 dB |
| – | 24 to 27 kHz | ≥38 dB |
| – | 27 to 35 kHz | ≥40 dB |
| – | 35 to 64 kHz | ≥50 dB |
| – | 64 to 68 kHz | ≥31 dB |
| – | 68 kHz | ≥35 dB |
| – | 69 to 88 kHz | ≥40 dB |

### 7.7.3 Concealment

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see Fig.11).

In CD-ROM modes (i.e. the external DAC interface is selected to be in a CD-ROM format) concealment is not executed.

### 7.7.4 MUTE, FULL-SCALE, ATTENUATION AND FADE

A digital level controller is present on the SAA7324 which performs the functions of soft mute, full-scale, attenuation and fade; these are selected via decoder register 0:

- Mute: signal reduced to 0 in a maximum of 128 steps; (3/n) ms
- Attenuation: signal scaled by −12 dB
- Full-scale: ramp signal back to 0 dB level; from mute takes (3/n) ms
- Fade: activates a 128 stage counter which allows the signal to be scaled up/down by 0.07 dB steps
  - 128 = full-scale
  - 120 = −0.5 dB (i.e. full-scale if oversampling filter used)
  - 32 = −12 dB
  - 0 = mute.

### 7.7.5 PEAK DETECTOR

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via pin SDA.

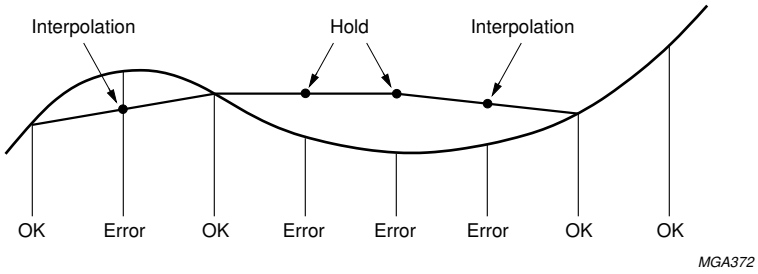



Fig.11 Concealment mechanism.

## 7.8 DAC interface

### 7.8.1 INTERNAL BITSTREAM DIGITAL-TO-ANALOG CONVERTER (DAC)

The onboard bitstream DAC operates at a clock frequency of $96f_s$ and is designed for operation with an audio input at $1f_s$. Optimum performance is dependent on the application circuit used and careful consideration should be given to the recommended application circuits shown in Figs 38 and 39. The onboard DAC is controlled from shadow register 7 (see Section 7.15.3 for definition of shadow registers). This shadow register controls routing of data into the onboard DAC and also controls the DAC output pins, which can be held at zero when the onboard DAC is not required; see Table 4:

Audio data from the decoder part of the SAA7324 can be routed as described in Sections 7.8.1.1 and 7.8.1.2.

**Table 4** Shadow register

| SHADEN | SHADOW ADDRESS | REGISTER | DATA | FUNCTION | RESET |
|---|---|---|---|---|---|
| 1 | 0111 (7H) | control of onboard DAC | XXX0 | hold onboard DAC outputs at zero | reset |
| | | | XXX1 | enable onboard DAC outputs | – |
| | | | XX0X | use external DAC or route audio data into onboard DAC (loopback mode) | reset |
| | | | XX1X | route audio data into onboard DAC (non-loopback mode) | – |

#### *7.8.1.1 Use onboard DAC*

Setting shadow register 7 to XX11 will route audio data from the CD10 decoder into the internal DAC, and enables the DAC output pins (LN, LP, RN and RP). To enable the on-board DAC, the DAC interface format (set by register 3) must be set to 16-bit $1f_s$ mode, either $I^2S$ or EIAJ format. CD-ROM mode can also be used if interpolation is not required. The serial data output pins for interfacing with an external DAC (SCLK, WCLK, DATA and EF) are set to high-impedance.

#### *7.8.1.2 Loopback external data into onboard DAC*

The onboard DAC can also be set to accept serial data inputs from an external source, e.g. an Electronic Shock Absorption (ESA) IC. This is known as loopback mode and is enabled by setting shadow register 7 to XX01.

This enables the serial data output pins (SCLK, WCLK, DATA and EF) so that data can be routed from the SAA7324 to an external ESA system (or external DAC).

The serial data from an external ESA IC can then also be input to the onboard DAC on the SAA7324 by utilising the serial data input interface (SCLI, SDI and WCLI).

In this mode, a wide range of data formats to the external ESA IC can be programmed as shown in Table 5. However, the serial input on the SAA7324 will always expect the input data from the ESA IC to be 16-bit $1f_s$ and the same data format, either $I^2S$-bus or EIAJ, as the serial output format (set by decoder register 3).

### 7.8.2 External DAC interface

Audio data from the SAA7324 can be sent to an external DAC, identical to the SAA737x series. This is similar to the 'loopback' mode, but in this case the internal DAC outputs can be held at zero. i.e. shadow register 7 is set to XX00. The SAA7324 is compatible with a wide range of external DACs. Eleven formats are supported and are given in Table 5. Figures 12 and 13 show the Philips I²S-bus and the EIAJ data formats respectively. When the decoder is operated in lock-to-disc mode, the SCLK frequency is dependent on the disc speed factor 'd'.

All formats are MSB first and $f_s$ is (44.1 × n) kHz. The polarity of the WCLK and the data can be inverted; selectable by decoder register 7. It should be noted that EF is only a defined output in CD-ROM and $1f_s$ modes.

When using an external DAC (or when using the onboard DAC in non-loopback mode), the serial data inputs to the onboard DAC (SCLI, SDI and WCLI) should be left unconnected.

**Table 5** DAC interface formats

| REGISTER 3 | SAMPLE FREQUENCY | NUMBER OF BITS | SCLK (MHz) | FORMAT | INTERPOLATION |
|---|---|---|---|---|---|
| 1010 | $f_s$ | 16 | 2.1168 × n | CD-ROM (I²S-bus) | no |
| 1011 | $f_s$ | 16 | 2.1168 × n | CD-ROM (EIAJ) | no |
| 1110 | $f_s$ | 16/18[1] | 2.1168 × n | Philips I²S-bus 16/18 bits[1] | yes |
| 0010 | $f_s$ | 16 | 2.1168 × n | EIAJ 16 bits | yes |
| 0110 | $f_s$ | 18 | 2.1168 × n | EIAJ 18 bits | yes |
| 0000 | $4f_s$ | 16 | 8.4672 × n | EIAJ 16 bits | yes |
| 0100 | $4f_s$ | 18 | 8.4672 × n | EIAJ 18 bits | yes |
| 1100 | $4f_s$ | 18 | 8.4672 × n | Philips I²S-bus 18 bits | yes |
| 0011 | $2f_s$ | 16 | 4.2336 × n | EIAJ 16 bits | yes |
| 0111 | $2f_s$ | 18 | 4.2336 × n | EIAJ 18 bits | yes |
| 1111 | $2f_s$ | 18 | 4.2336 × n | Philips I²S-bus 18 bits | yes |

**Note**

1. In this mode the first 16 bits contain data, but if any of the fade, attenuate or de-emphasis filter functions are activated then the first 18 bits contain data.

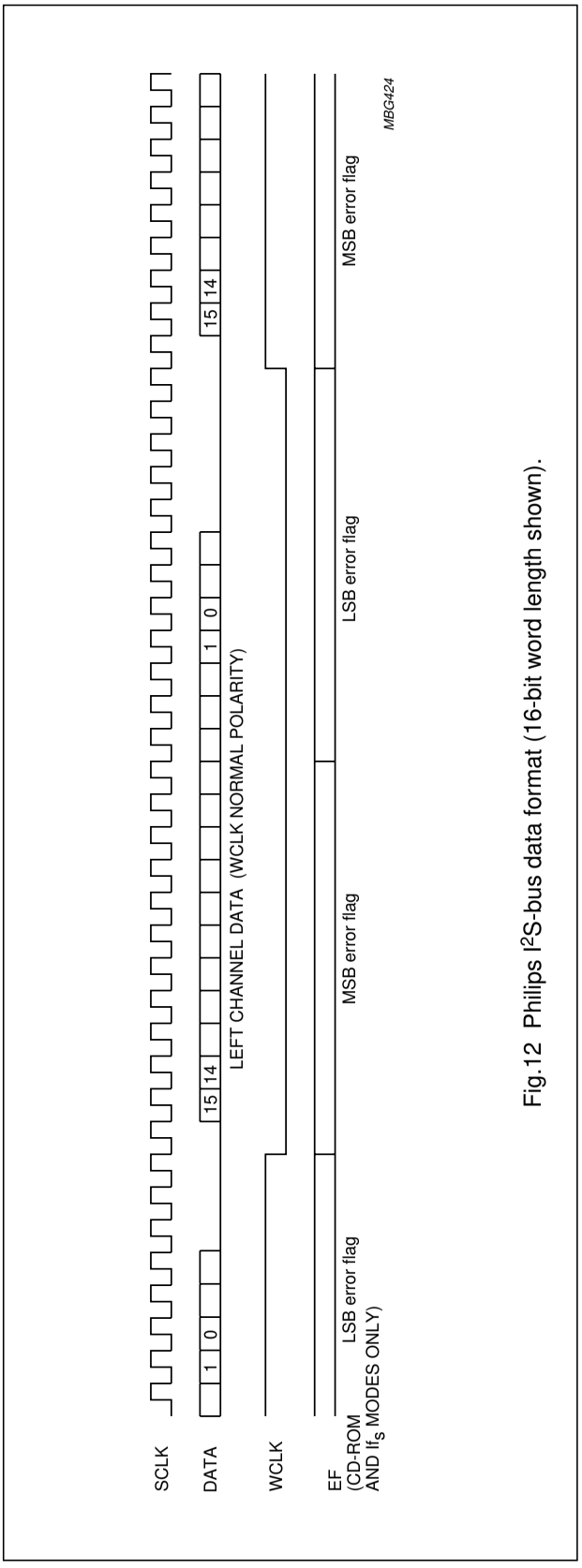



Fig.12 Philips I²S-bus data format (16-bit word length shown).

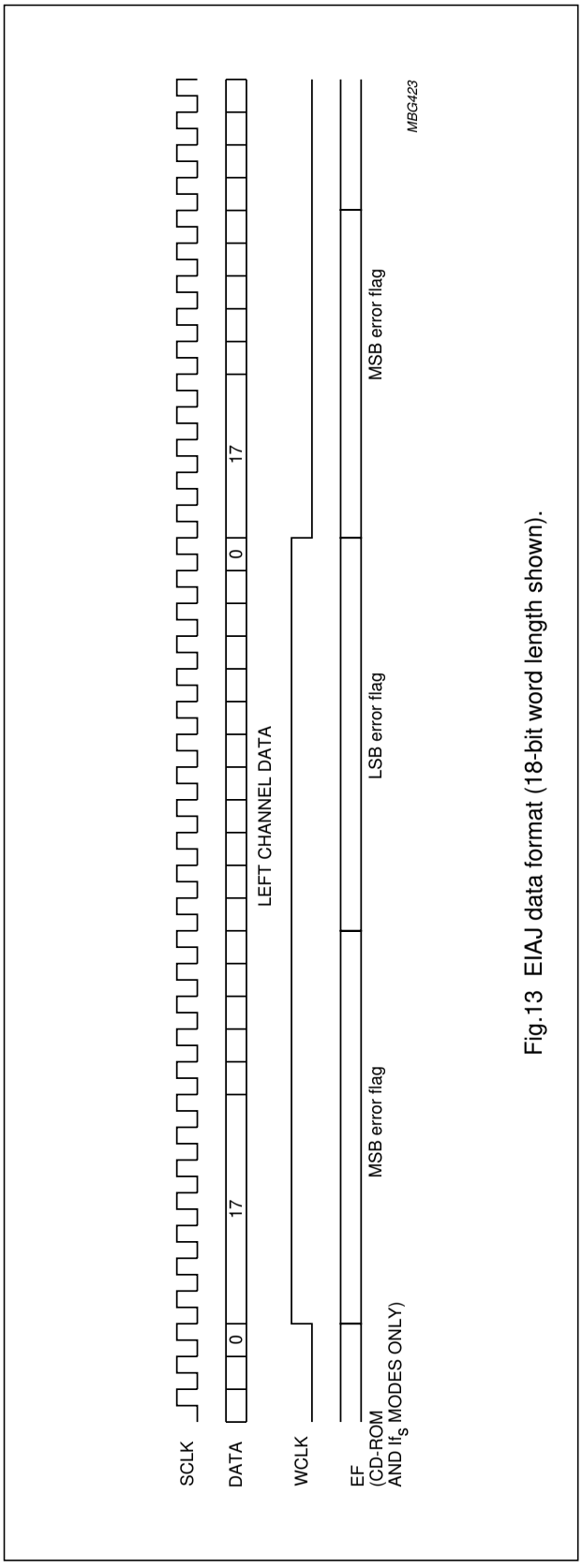



Fig.13 EIAJ data format (18-bit word length shown).

### 7.9 EBU interface

The bi-phase mark digital output signal at pin DOBM is in accordance with the format defined by the IEC 958 specification. Three different modes can be selected via decoder register A:

- DOBM pin held LOW
- Data taken before concealment, mute and fade (must always be used for CD-ROM modes)
- Data taken after concealment, mute and fade.

#### 7.9.1 FORMAT

The digital audio output consists of 32-bit words ('subframes') transmitted in bi-phase mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384. The formats are given in Table 6.

**Table 6** Format

| FUNCTION | BITS | DESCRIPTION |
|---|---|---|
| Sync | 0 to 3 | – |
| Auxiliary | 4 to 7 | not used; normally zero |
| Error flags | 4 | CFLG error and interpolation flags when selected by register A |
| Audio sample | 8 to 27 | first 4 bits not used (always zero); 2's complement; LSB = bit 12, MSB = bit 27 |
| Validity flag | 28 | valid = logic 0 |
| User data | 29 | used for subcode data (Q-to-W) |
| Channel status | 30 | control bits and category code |
| Parity bit | 31 | even parity for bits 4 to 30 |

**Table 7** Description of Table 6

| FUNCTION | DESCRIPTION |
|---|---|
| Sync | The sync word is formed by violation of the bi-phase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations: sync B: start of a block (384 words), word contains left sample; sync M: word contains left sample (no block start) and sync W: word contains right sample. |
| Audio sample | Left and right samples are transmitted alternately. |
| Validity flag | Audio samples are flagged (bit 28 = 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment. |
| User data | Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate. |
| Channel status | The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is given in Table 8. |

**Table 8** Bit assignment

| FUNCTION | BITS | DESCRIPTION |
|---|---|---|
| Control | 0 to 3 | copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis |
| Reserved mode | 4 to 7 | always zero |
| Category code | 8 to 15 | CD: bit 8 = logic 1, all other bits = logic 0 |
| Clock accuracy | 28 to 29 | set by register A; 10 = level I; 00 = level II; 01 = level III |
| Remaining | 6 to 27 and 30 to 191 | always zero |

### 7.10 KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel prior to the digital filter. The output is switched to active LOW when silence has been detected for at least 270 ms, or if mute is active, or in CD-ROM modes. Two modes are available which can be selected by decoder register C:

1. Pin KILL: KILL active LOW indicates silence detected on both left and right channels
2. Pin KILL: KILL active LOW indicates silence detected on left channel. V3 active LOW indicates silence detected on right channel.

It should be noted that when mute is active or in CD-ROM modes the output(s) are switched LOW.

### 7.11 Audio features off

The audio features can be turned off (selected by decoder register E) which affects the following functions:

- Digital filter, fade, peak detector, KILL circuit (but outputs KILL, V3 still active) are disabled
- V5 (if selected to be the de-emphasis flag output) and the EBU outputs become undefined.

It should be noted that the EBU output should be set LOW prior to switching the audio features off and after switching the audio features back on, a full-scale command should be given.

### 7.12 The versatile pins interface

The SAA7324 has four pins that can be reconfigured for different applications. One of these pins, V2/V3, can be programmed as an input (V2) or as an output (V3). Control of the V2/V3 pin is via shadow register 3; see Table 9.

Selection of the V2/V3 pin does not affect the function programmed by decoder register C i.e. the V2 or V3 pin can be changed from V2/V3 function either before or after setting the desired function via decoder register 1100. Selection of, for instance, a V3 function while the V2/V3 pin is set to V2 will not affect the V2 functionality.

The functions of these versatile pins is identical to the SAA737x series. The functions of these versatile pins is programmed by decoder registers C and D, as shown in Table 10.

**Table 9** V2 or V3 configuration

| SHADEN | ADDRESS | REGISTER | DATA | FUNCTION | RESET |
|---|---|---|---|---|---|
| 1 | 0011 (3H) | control of V2 or V3 pin | 0XXX | V2/V3 pin configured as V2 input | reset |
| | | | 1XXX | V2/V3 pin configured as V3 output (open-drain) | |

**Table 10** Pin applications

| PIN NAME | PIN NUMBER | TYPE | REGISTER ADDRESS | REGISTER DATA | FUNCTION |
|---|---|---|---|---|---|
| V1 | 63 | input | 1100 | XXX1 | external off-track signal input |
| | | | – | XXX0 | internal off-track signal used input may be read via decoder status bit; selected via register 2 |
| V2 | 36 | input | – | – | input may be read via decoder status bit; selected via register 2 |
| V3 | 36 | output | 1100 | XX0X | KILL output for right channel |
| | | | – | X01X | output = 0 |
| | | | – | X11X | output = 1 |
| V4 | 61 | output | 1101 | 0000 | 4-line motor drive (using V4 and V5) |
| | | | – | XX01 | Q-to-W subcode output |
| | | | – | XX10 | output = 0 |
| | | | – | XX11 | output = 1 |
| V5 | 62 | output | 1101 | 01XX | de-emphasis output (active HIGH) |
| | | | – | 10XX | output = 0 |
| | | | – | 11XX | output = 1 |

## 7.13 Spindle motor control

### 7.13.1 MOTOR OUTPUT MODES

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by decoder register 6, are supported:

- Pulse density, 2-line (true complement output), (1 × n) MHz sample frequency
- PWM output, 2-line, (22.05 × n) kHz modulation frequency
- PWM output, 4-line, (22.05 × n) kHz modulation frequency
- CDV motor mode.

#### *7.13.1.1 Pulse density output mode*

In the pulse density mode the motor output pin (MOTO1) is the pulse density modulated motor output signal. A 50% duty factor corresponds with the motor not actuated, higher duty factors mean acceleration, lower mean braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a (1 × n) MHz internal clock signal. Possible application diagrams are illustrated in Fig.14.

#### *7.13.1.2 PWM output mode (2-line)*

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output. The motor braking signal is pulse-width modulated on the MOTO2 output. The timing is illustrated in Fig.15. A typical application diagram is illustrated in Fig.16.

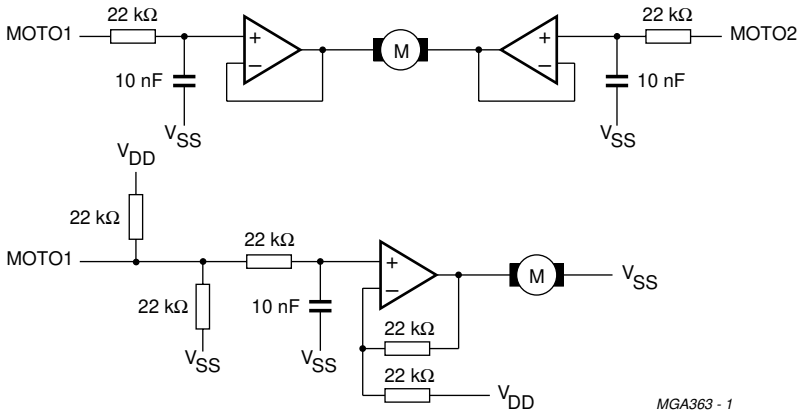



Fig.14 Motor pulse density application diagrams.

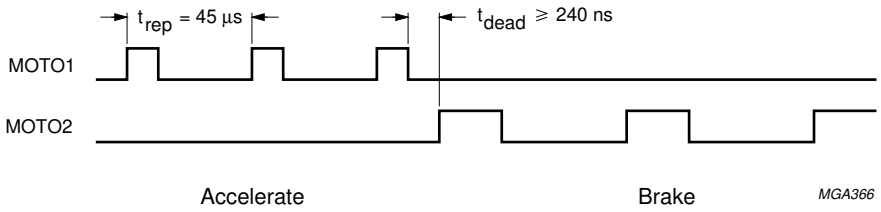



Fig.15 2-line PWM mode timing.

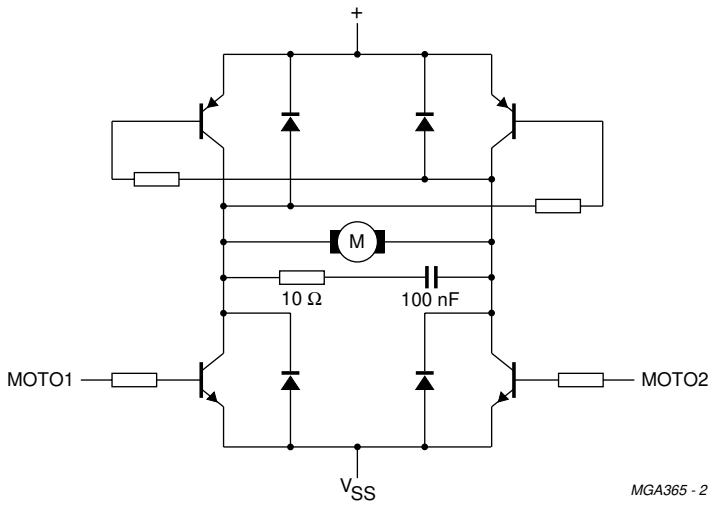



Fig.16 Motor 2-line PWM mode application diagram.

*7.13.1.3 PWM output mode (4-line)*

Using two extra outputs from the versatile pins interface, it is possible to use the SAA7324 with a 4-input motor bridge. The timing is illustrated in Fig.17. A typical application diagram is illustrated in Fig.18.

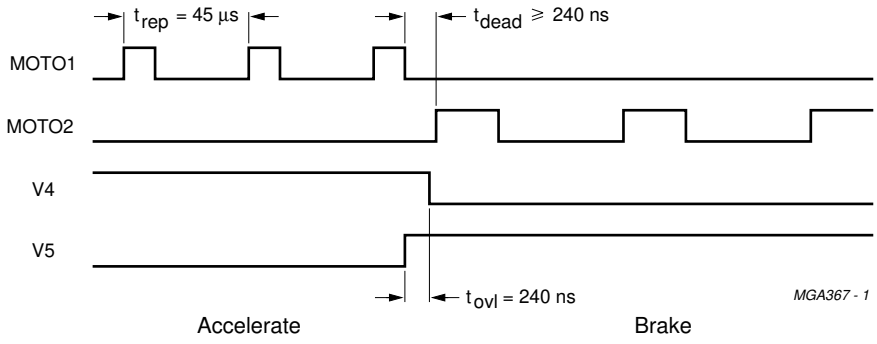



Fig.17 4-line PWM mode timing.

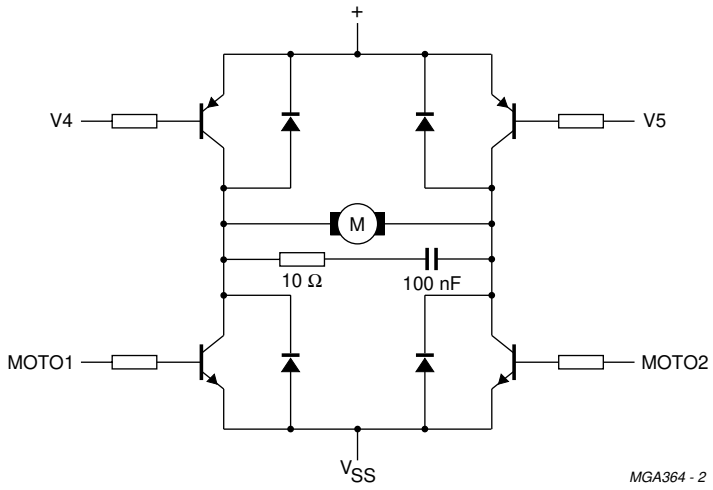



Fig.18 Motor 4-line PWM mode application diagram.

#### *7.13.1.4 CDV/CAV output mode*

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin [carrier frequency (300 × d) Hz], where 'd' is the disc speed factor. The PLL frequency signal will be put in pulse-density modulated form (carrier frequency 4.23 × n MHz) on the MOTO2 pin. The integrated motor servo is disabled in this mode.

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half full) will result in a PWM output of 60%.

In the lock-to-disc (CAV) mode the CDV motor mode is the only mode that can be used to control the motor.

### 7.13.2 Spindle motor operating modes

The operating modes of the motor servo is controlled by decoder register 1 (see Table 11).

In the SAA7324 decoder there is an anti-windup mode for the motor servo, selected via decoder register 1. When the anti-windup mode is activated the motor servo integrator will hold if the motor output saturates.

#### *7.13.2.1 Power limit*

In start mode 1, start mode 2, stop mode 1 and stop mode 2, a fixed positive or negative voltage is applied to the motor. This voltage can be programmed as a percentage of the maximum possible voltage, via register 6, to limit current drain during start and stop.

The following power limits are possible:

- 100% (no power limit), 75%, 50%, or 37% of maximum.

### 7.13.3 Loop characteristics

The gain and crossover frequencies of the motor control loop can be programmed via decoder registers 4 and 5. The following parameter values are possible:

- Gains: 3.2, 4.0, 6.4, 8.0, 12.8, 16, 25.6 and 32
- Crossover frequency $f_4$: 0.5 × n Hz, 0.7 × n Hz, 1.4 × n Hz and 2.8 × n Hz
- Crossover frequency $f_3$: 0.85 × n Hz, 1.71 × n Hz and 3.42 × n Hz.

It should be noted that the crossover frequencies $f_3$ and $f_4$ are scaled with the overspeed factor 'n' whereas the gains are not.

### 7.13.4 FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g.: as a result of motor rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator tries to conceal as much as possible to minimize the effect of data loss.

**Table 11** Operating modes

| MODE | DESCRIPTION |
|---|---|
| Start mode 1 | The disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller. |
| Start mode 2 | The disc is accelerated as in start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to jump mode. The motor status signals selectable via register 2 are valid. |
| Jump mode | Motor servo enabled but FIFO kept reset at 50%, integrator is held. The audio is muted but it is possible to read the subcode. It should be noted that in the CD-ROM modes the data, on EBU and the $I^2S$-bus is not muted. |
| Jump mode 1 | Similar to jump mode but motor integrator is kept at zero. Used for long jumps where there is a large change in disc speed. |
| Play mode | FIFO released after resetting to 50%. Audio mute released. |
| Stop mode 1 | Disc is braked by applying a negative voltage to the motor. No decisions are involved. |
| Stop mode 2 | The disc is braked as in stop mode 1 but the PLL will monitor the disc speed. As soon as the disc reaches 12% (or 6%, depending on the programmed brake percentage, via register E) of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to Off mode. |
| Off mode | Motor not steered. |

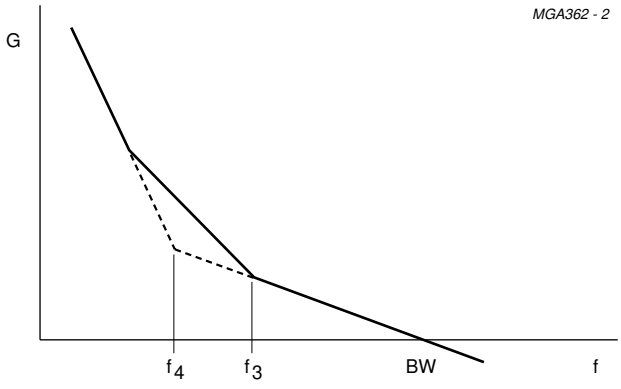



Fig.19 Motor servo mode diagram.