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DATA SHEET

SAA7377
Digital servo processor and Compact Disc decoder (CD7)

Product specifications
File under Integrated Circuits, IC01

1998 Jul 06

Philips
Semiconductors

PHILIPS

Digital servo processor and Compact Disc decoder (CD7) SAA7377

CONTENTS

Digital servo processor and Compact Disc decoder (CD7)

SAA7377

1 FEATURES

- Single-speed mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio only
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I²C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7377 is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current		–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7377GP	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

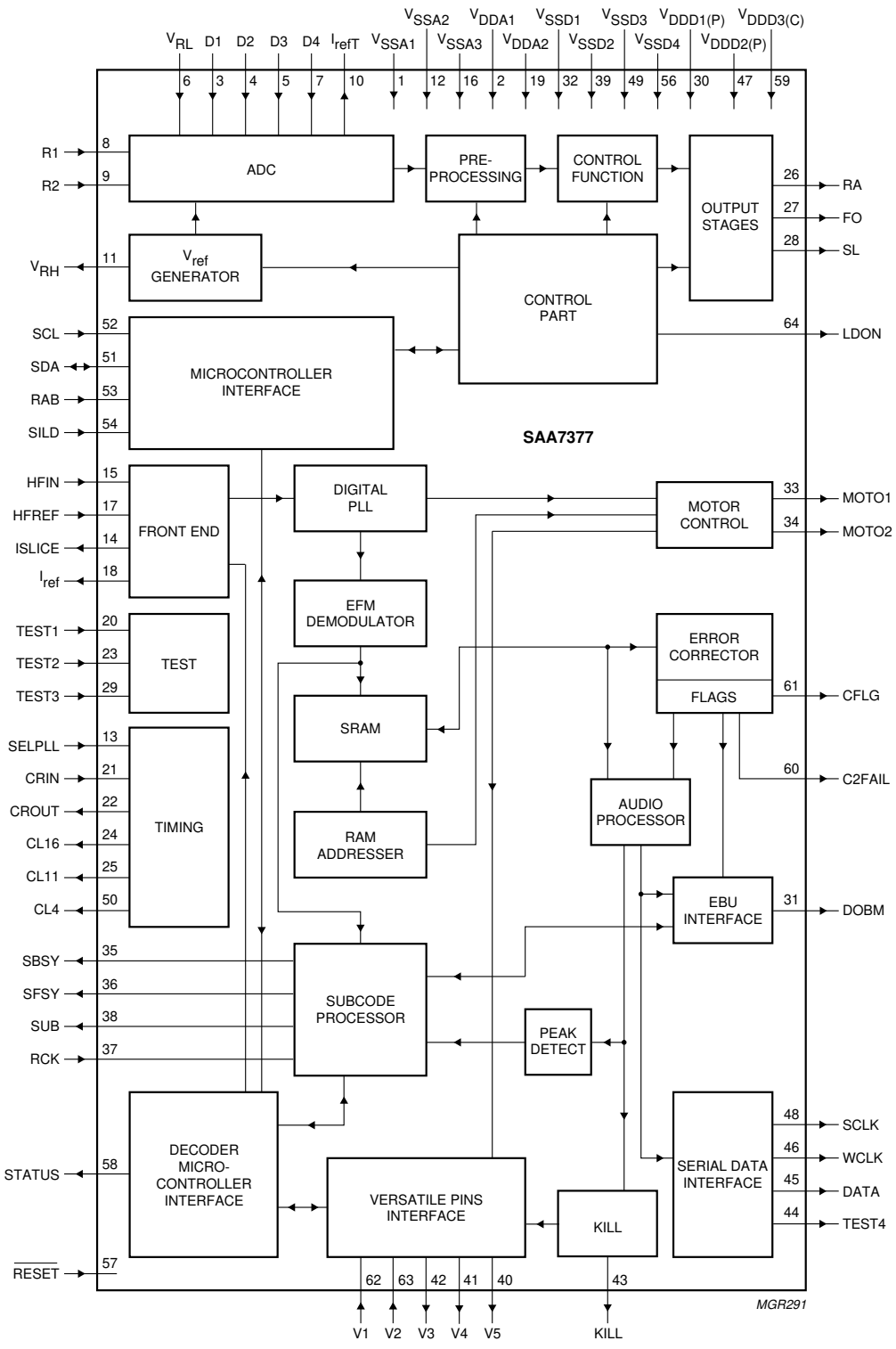

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448 MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode output bits (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
TEST4	44	test output pin; this pin should be left unconnected
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47(1)	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49(1)	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56(1)	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59(1)	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

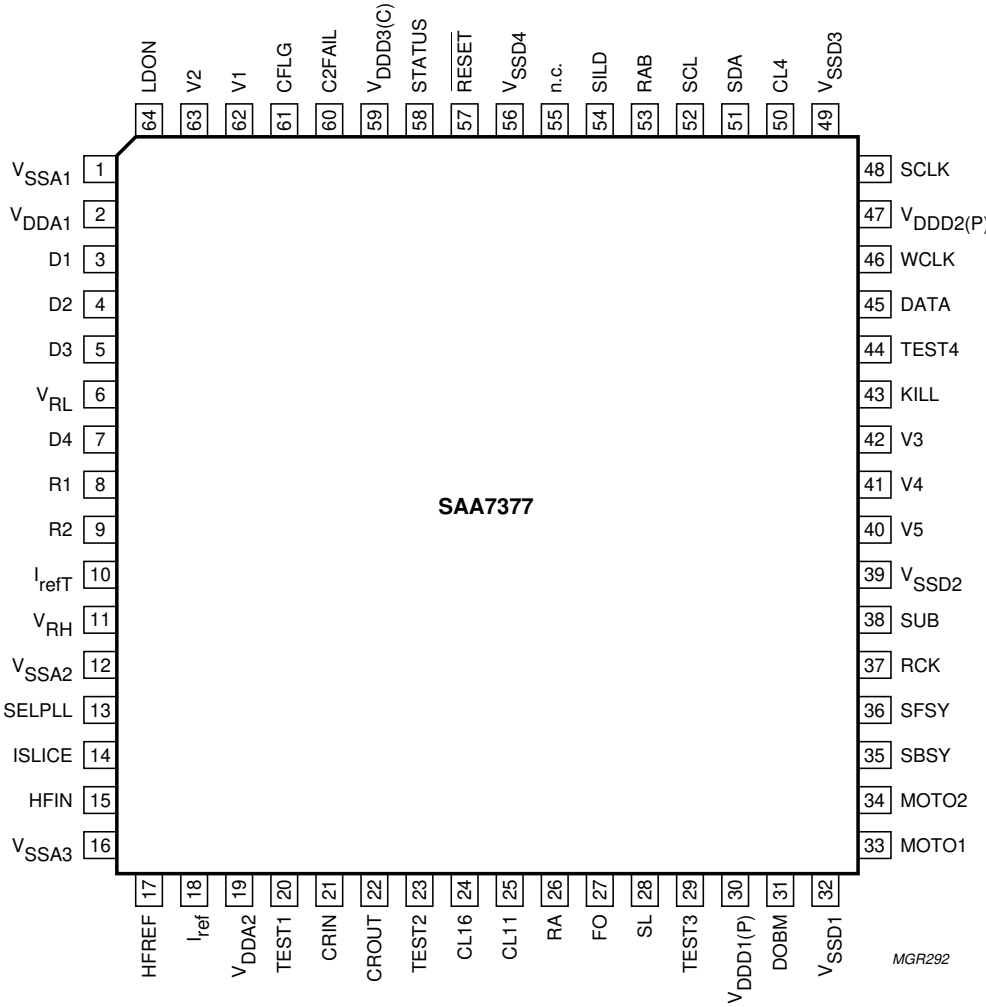

Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Decoder part

7.1.1 PRINCIPLE OPERATIONAL MODES OF THE DECODER

The decoding part operates at single-speed and supports a full audio specification.

A simplified data flow through the decoder part is illustrated in Fig.6.

7.1.2 CRYSTAL FREQUENCY SELECTION

The SAA7377, which has an internal phase-locked loop clock multiplier, can be used with 33.8688, 16.9344 or 8.4672 MHz crystal frequencies by setting register B and SELPLL as shown in Table 1. The internal clock multiplier, controlled by SELPLL, should only be used if a 8.4672 MHz crystal, ceramic resonator or external clock is present. It should be noted that the CL11 output is a 5.6448 MHz clock if a 16.9344 MHz external clock is used.

Table 1 Crystal frequency selection

REGISTER B	SELPLL	CRYSTAL FREQUENCY (MHz)
00xx	0	33.8688
00xx	1	8.4672
01xx	0	16.9344

7.1.3 STANDBY MODES

The SAA7377 may be placed in two standby modes selected by register B (it should be noted that the device core is still active)

Standby 1: “CD-STOP” mode. Most I/O functions are switched off.

Standby 2: “CD-PAUSE” mode. Audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active. This is also called a “Hot Pause”.

In the standby modes the various pins will have the following values;

MOTO1 and MOTO2: put in high-impedance, PWM mode (standby 1 and $\overline{\text{RESET}}$, operating in standby 2). Put in high-impedance, PDM mode (standby 1 and $\overline{\text{RESET}}$, operating in standby 2).

SCL, SDA, SILD and RAB: no interaction. Normal operation continues.

SCLK, WCLK, DATA, CL11 and DOBM: 3-state in both standby modes. Normal operation continues after reset.

CRIN, CROUT, CL16 and CL4: no interaction. Normal operation continues.

V1, V2, V3, V4, V5, CFLG and C2FAIL: no interaction. Normal operation continues.

7.2 Crystal oscillator

The crystal oscillator is a conventional 2 pin design operating between 8 and 35 MHz. This oscillator is capable of operating with ceramic resonators and also with both fundamental and third overtone crystals. External components should be used to suppress the fundamental output of the third overtone crystals as shown in Figs 3 and 4. Typical oscillation frequencies required are 8.4672, 16.9344 or 33.8688 MHz depending on the internal clock settings used and whether or not the clock multiplier is enabled.

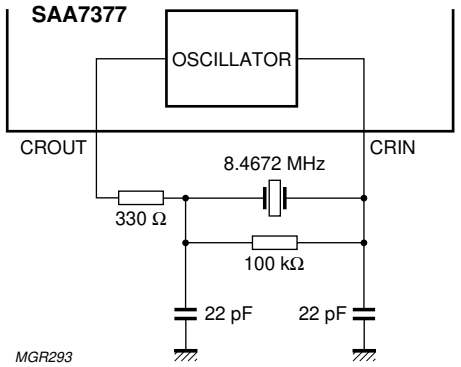

Fig.3 8.4672 MHz fundamental configuration.

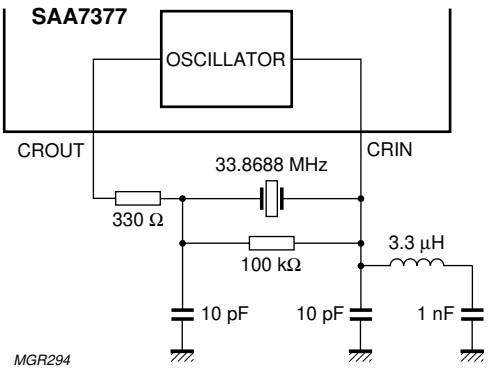

Fig.4 33.8688 MHz overtone configuration.

7.3 Data slicer and clock regenerator

The SAA7377 has an integrated slice level comparator which can be clocked by the crystal frequency clock, or 8 times the crystal frequency clock (if SELPLL is set HIGH while using an 8.4672 MHz crystal, and register 4 is set to 0xxx). The slice level is controlled by an internal current source applied to an external capacitor under the control of the Digital Phase-Locked Loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization.

For certain applications an off-track input is necessary. This is internally connected from the servo part (its polarity can be changed by the foc_parm1 parameter), but may be input via the V1 pin if selected by register C. If this flag is HIGH, the SAA7377 will assume that its servo part is following on the wrong track and will flag all incoming HF data as incorrect.

7.4 Demodulator

7.4.1 FRAME SYNC PROTECTION

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data.

The master counter is only reset if:

- A sync coincidence detected; sync pattern occurs 588 ±1 EFM clocks after the previous sync pattern
- A new sync pattern is detected within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active HIGH after 1 sync coincidence found, and reset LOW if, during 61 consecutive frames, no sync coincidence is found. The PLL lock signal can be accessed via the SDA or STATUS pins selected by register 2 and 7.

Also incorporated in the demodulator is a Run Length 2 (RL2) correction circuit. Every symbol detected as RL2 will be pushed back to RL3. To do this, the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

7.4.2 EFM DEMODULATION

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

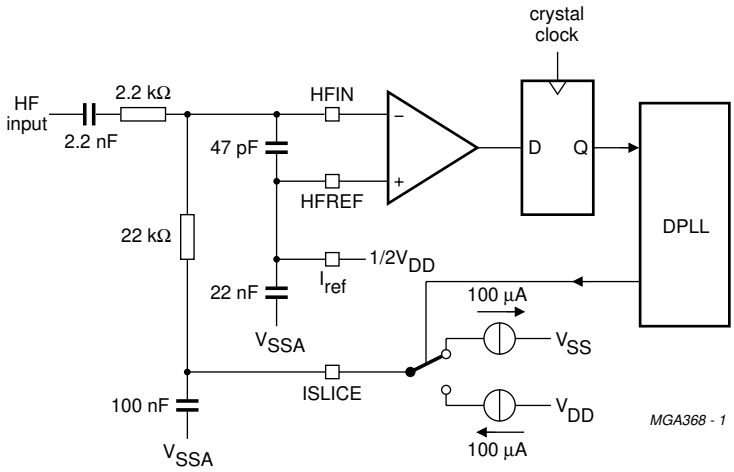

Fig.5 Data slicer showing typical application components.

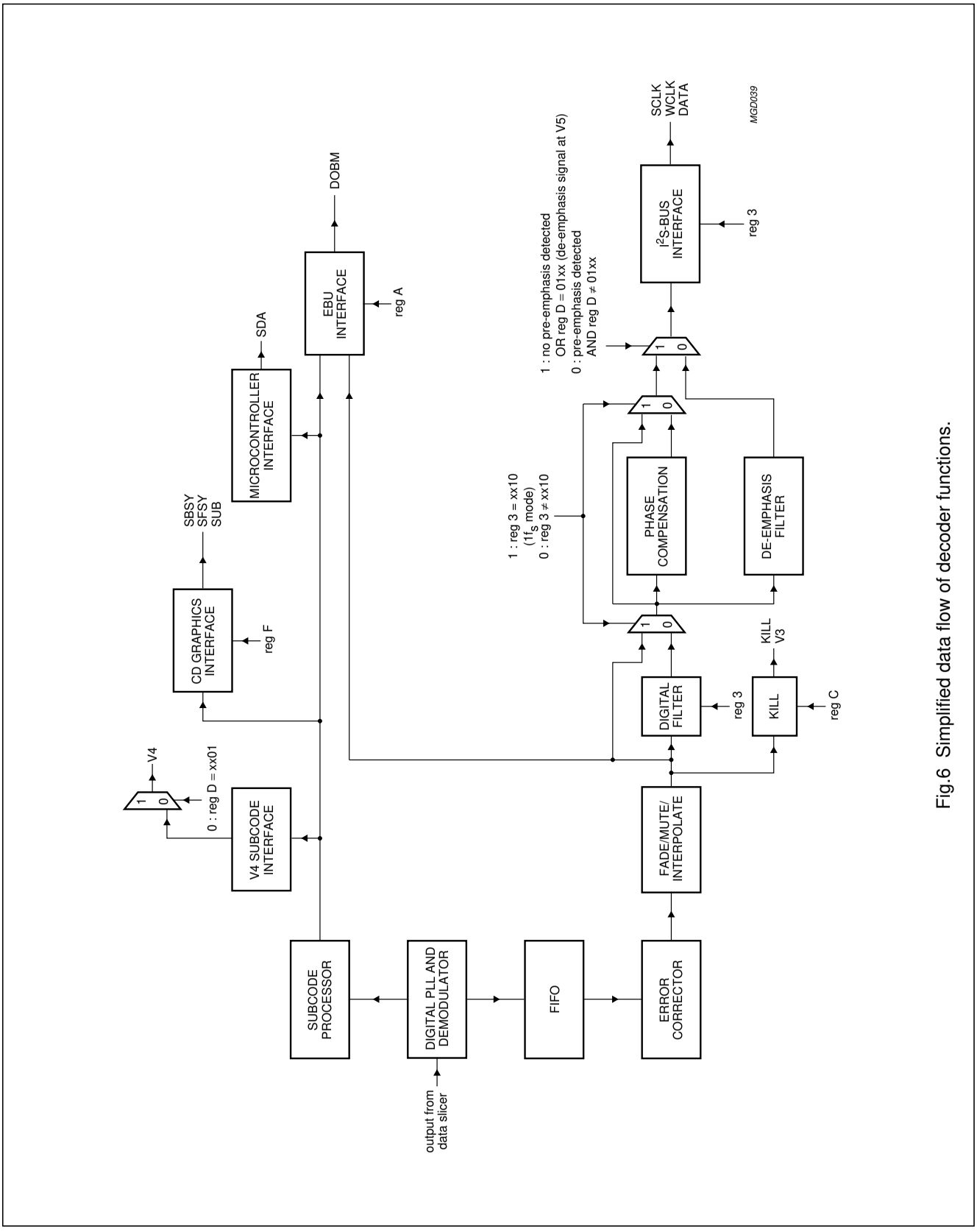

Fig.6 Simplified data flow of decoder functions.

7.5 Subcode data processing

7.5.1 Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the SDA or STATUS pins, selected via register 2. Good Q-channel data may be read from SDA.

7.5.2 EIAJ 3 AND 4-WIRE SUBCODE (CD GRAPHICS) INTERFACES

Data from all the subcode channels (P-to-W) may be read via the subcode interface, which conforms to EIAJ CP-2401. The interface is enabled and configured as either a 3-wire or 4-wire interface via register F. The subcode interface output formats are illustrated in Fig.7, where the RCK signal is supplied by another device such as a CD graphics decoder.

7.5.3 V4 SUBCODE INTERFACE

Data of subcode channels, Q-to-W, may be read via pin V4 if selected via register D. The format is similar to RS232 and is illustrated in Fig.8. The subcode sync word is formed by a pause of 200 μs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between 11.3 μs and 90 μs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

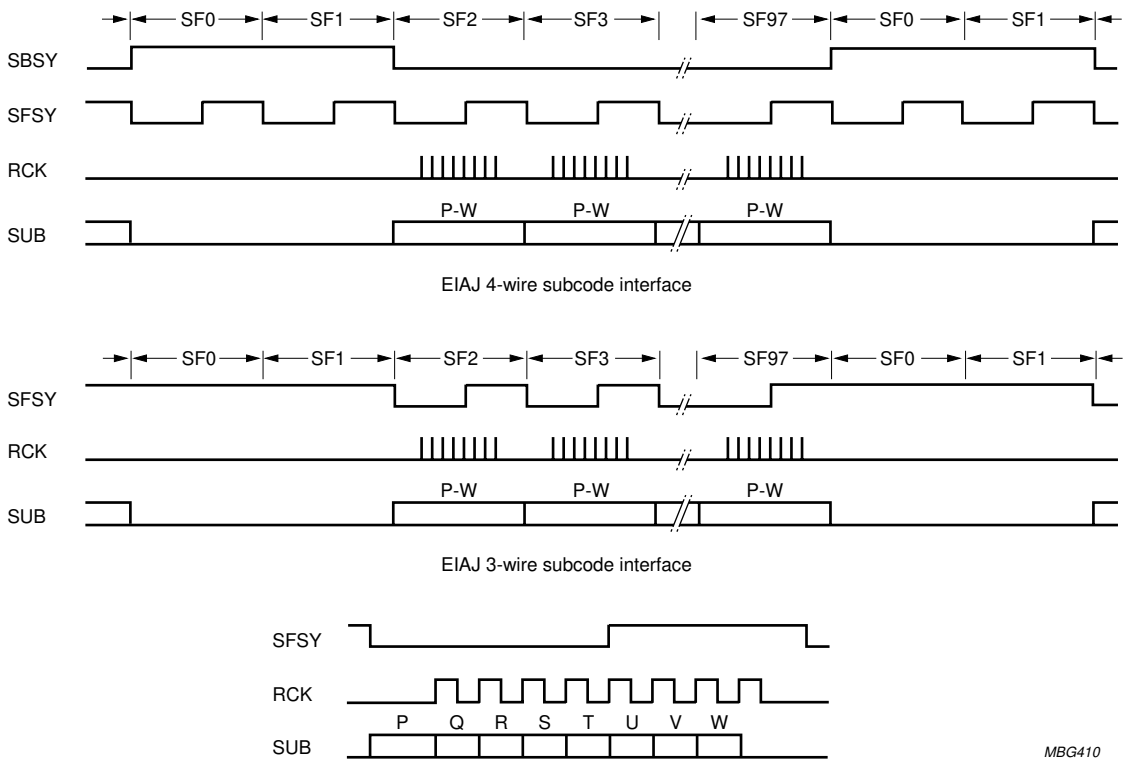

Fig.7 EIAJ subcode (CD graphics) interface format.

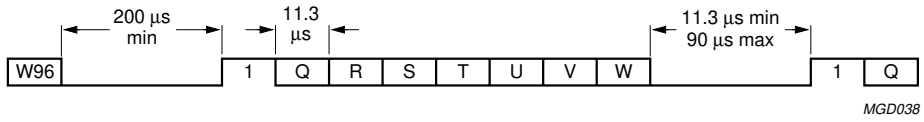

Fig.8 Subcode format and timing on pin V4.

7.6 FIFO and error corrector

The SAA7377 has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.

The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after (de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM).

7.6.1 FLAGS OUTPUT (CFLG)

The flags output pin CFLG (open-drain) shows the status of the error corrector and interpolator and is updated every frame (7.35 kHz). In the SAA7377 chip a 1-bit flag is present on the CFLG pin as illustrated in Fig.9. This signal shows the status of the error corrector and interpolator.

The first flag bit, F1, is the absolute time sync signal, the FIFO-passed subcode sync and relates the position of the subcode sync to the audio data (DAC output). This flag may also be used in a super FIFO or in the synchronization of different players. The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by register A.

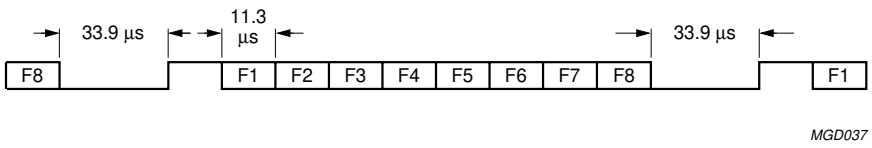

Fig.9 Flag output timing diagram.

Table 2 Output flags

F1	F2	F3	F4	F5	F6	F7	F8	DESCRIPTION
0	x	x	x	x	x	x	x	no absolute time sync
1	x	x	x	x	x	x	x	absolute time sync
x	0	0	x	x	x	x	x	C1 frame contained no errors
x	0	1	x	x	x	x	x	C1 frame contained 1 error
x	1	0	x	x	x	x	x	C1 frame contained 2 errors
x	1	1	x	x	x	x	x	C1 frame uncorrectable
x	x	x	0	0	x	x	0	C2 frame contained no errors
x	x	x	0	0	x	x	1	C2 frame contained 1 error
x	x	x	0	1	x	x	0	C2 frame contained 2 errors
x	x	x	0	1	x	x	1	C2 frame contained 3 errors
x	x	x	1	0	x	x	0	C2 frame contained 4 errors
x	x	x	1	1	x	x	1	C2 frame uncorrectable
x	x	x	x	x	0	0	x	no interpolations
x	x	x	x	x	0	1	x	at least one 1 sample interpolation
x	x	x	x	x	1	0	x	at least one hold and no interpolations
x	x	x	x	x	1	1	x	at least one hold and one 1 sample interpolation

7.6.2 C2FAIL

The C2FAIL pin indicates that invalid data has occurred on the I²S-bus interface. However, due to the structure of the corrector it is impossible to determine which byte has failed. C2FAIL will go LOW for 140 µs when invalid data is detected, this data may then occur 15 ms before or after the pin is activated.

7.7 Audio functions

7.7.1 De-emphasis and phase linearity

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase of the digital oversampling filter to ≤ ±1° within the band 0 to 16 kHz. With de-emphasis the filter is not phase linear.

If the de-emphasis signal is set to be available at V5, selected via register D, then the de-emphasis filter is bypassed.

7.7.2 Digital oversampling filter

The SAA7377 contains a 2 to 4 times oversampling IIR filter. The filter specification of the 4 times oversampling filter is given in Table 3.

These attenuations do not include the sample-and-hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled −0.5 dB down, to avoid overflow on full-scale sine wave inputs (0 to 20 kHz).

Table 3 Filter specification

PASS BAND	STOP BAND	ATTENUATION
0 to 9 kHz	–	≤0.001 dB
19 to 20 kHz	–	≤0.03 dB
–	24 kHz	≥25 dB
–	24 to 27 kHz	≥38 dB
–	27 to 35 kHz	≥40 dB
–	35 to 64 kHz	≥50 dB
–	64 to 68 kHz	≥31 dB
–	68 kHz	≥35 dB
–	69 to 88 kHz	≥40 dB

7.7.3 CONCEALMENT

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see Fig.10).

7.7.4 MUTE, FULL SCALE, ATTENUATION AND FADE

A digital level controller is present on the SAA7377 which performs the functions of soft mute, full scale, attenuation and fade; these are selected via register 0:

Mute: signal reduced to 0 in a maximum of 128 steps; 3 ms.

Attenuate: signal scaled by −12 dB.

Full scale: ramp signal back to 0 dB level. From mute takes 3 ms.

Fade: activates a 128 stage counter which allows the signal to be scaled up/down by 0.07 dB steps

128 = full scale.

120 = −0.5 dB (i.e. full scale if oversampling filter used).

32 = −12 dB.

0 = mute.

7.7.5 PEAK DETECTOR

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via SDA.

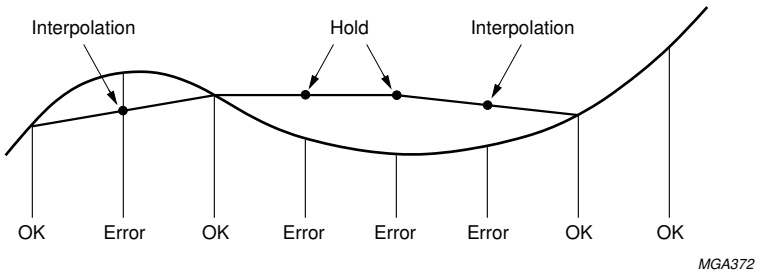

Fig.10 Concealment mechanism.

7.8 DAC interface

The SAA7377 is compatible with a wide range of digital-to-analog converters (DACs). Nine formats are supported and are given in Table 4. Figures 11 and 12 show the Philips I²S-bus and the EIAJ data formats respectively. All formats are MSB first and f_s is 44.1 kHz. The polarity of the WCLK and the data can be inverted; selectable by register 7.

Table 4 DAC interface formats

REGISTER 3	SAMPLE FREQUENCY	NUMBER OF BITS	SCLK (MHz)	FORMAT	INTERPOLATION
1110	f_s	16/18[1]	2.1168	Philips I²S-bus; 16/18 bits[1]	yes
0010	f_s	16	2.1168	EIAJ 16 bits	yes
0110	f_s	18	2.1168	EIAJ 18 bits	yes
0000	$4f_s$	16	8.4672	EIAJ 16 bits	yes
0100	$4f_s$	18	8.4672	EIAJ 18 bits	yes
1100	$4f_s$	18	8.4672	Philips I²S-bus; 18 bits	yes
0011	$2f_s$	16	4.2336	EIAJ 16 bits	yes
0111	$2f_s$	18	4.2336	EIAJ 18 bits	yes
1111	$2f_s$	18	4.2336	Philips I²S-bus; 18 bits	yes

Note

1. In this mode the first 16 bits contain data, but if any of the fade, attenuate or de-emphasis filter functions are activated then the first 18 bits contain data.

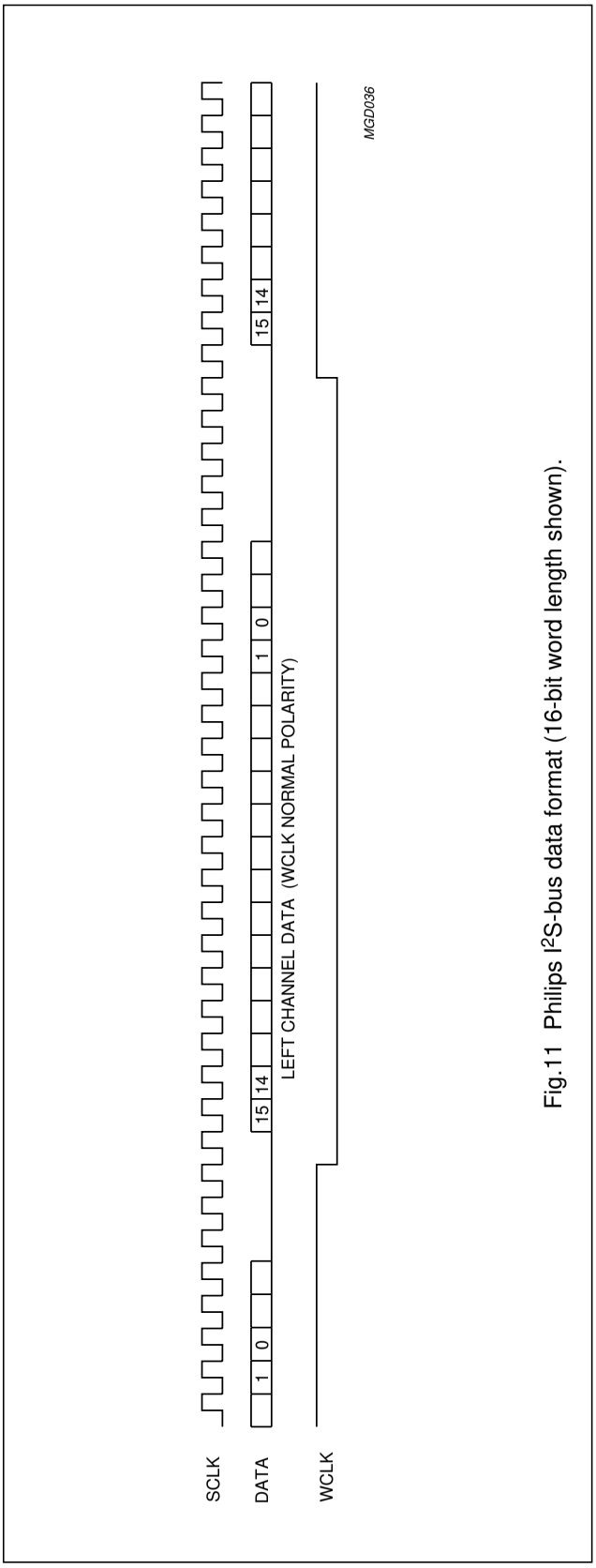

Fig.11 Philips I²S-bus data format (16-bit word length shown).

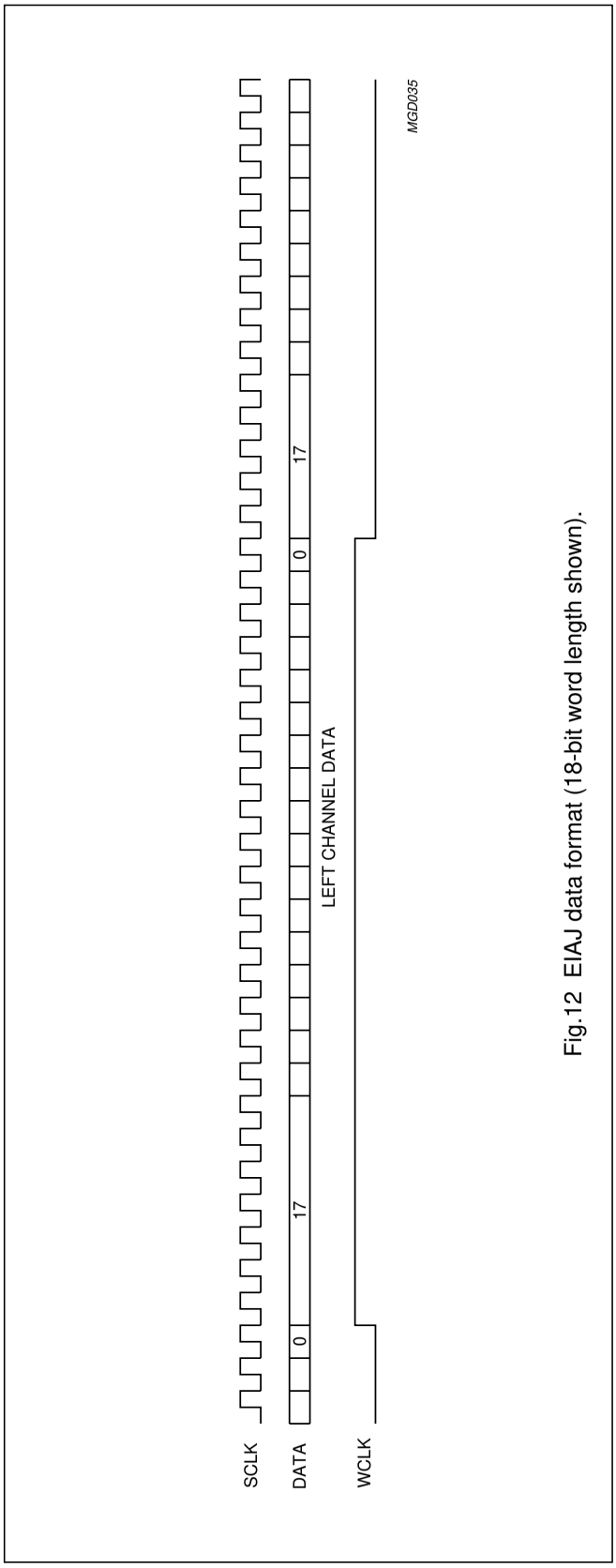

Fig.12 EIAJ data format (18-bit word length shown).

7.9 EBU interface

The bi-phase mark digital output signal at pin DOBM is in accordance with the format defined by the IEC958 specification. The DOBM pin can be held LOW and selected via register A.

7.9.1 FORMAT

The digital audio output consists of 32-bit words ('subframes') transmitted in bi-phase mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384. Table 5 gives the formats.

Table 5 Format

FUNCTION	BITS	DESCRIPTION
Sync	0 to 3	–
Auxiliary	4 to 7	not used; normally zero
Error flags	4	CFLG error and interpolation flags when selected by register A
Audio sample	8 to 27	first 4 bits not used (always zero). 2's compliment. LSB = bit 12, MSB = bit 27
Validity flag	28	valid = logic 0
User data	29	used for subcode data (Q-to-W)
Channel status	30	control bits and category code
Parity bit	31	even parity for bits 4 to 30

Table 6 Description of Table 5

FUNCTION	DESCRIPTION
Sync	The sync word is formed by violation of the bi-phase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations: sync B: start of a block (384 words), word contains left sample; sync M: word contains left sample (no block start) and sync W: word contains right sample.
Audio sample	Left and right samples are transmitted alternately.
Validity flag	Audio samples are flagged (bit 28 = 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment.
User data	Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.
Channel status	The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is given in Table 7.

Table 7 Bit assignment

FUNCTION	BITS	DESCRIPTION
Control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis
Reserved mode	4 to 7	always zero
Category code	8 to 15	CD: bit 8 = logic 1, all other bits = logic 0
Clock accuracy	28 to 29	set by register A; 10 = level I; 00 = level II; 01 = level III
Remaining	16 to 27 and 30 to 191	always zero

7.10 KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel before the digital filter. The output is switched active LOW when silence has been detected for at least 250 ms, or if mute is active. Two modes are available which can be selected by register C:

1 pin kill: KILL active LOW indicates silence detected on both left and right channels.

2 pin kill: KILL active LOW indicates silence detected on left channel. V3 active LOW indicates silence detected on right channel.

7.11 The VIA interface

The SAA7377 has five pins that can be reconfigured for different applications (see Table 8).

Table 8 Pin applications

PIN NAME	PIN NUMBER	TYPE	CONTROL REGISTER ADDRESS	CONTROL REGISTER DATA	FUNCTION
V1	62	input	1100	xxx1	external off-track signal input
			–	xxx0	internal off-track signal used, input may be read via decoder status bit; selected via register 2
V2	63	input	–	–	input may be read via decoder status bit; selected via register 2
V3	42	output	1100	xx0x	KILL output for right channel
			–	x01x	output = 0
			–	x11x	output = 1
V4	41	output	1101	0000	4-line motor drive (using V4 and V5)
			–	xx01	Q-to-W subcode output
			–	xx10	output = 0
			–	xx11	output = 1
V5	40	output	1101	01xx	de-emphasis output (active HIGH)
			–	10xx	output = 0
			–	11xx	output = 1

7.12 Spindle motor control

7.12.1 MOTOR OUTPUT MODES

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by register 6, are supported:

- Pulse density, 2-line (true complement output), 1 MHz sample frequency
- PWM output, 2-line, 22.05 kHz modulation frequency
- PWM output, 4-line, 22.05 kHz modulation frequency
- CDV motor mode.

7.12.1.1 Pulse density output mode

In the pulse density mode the motor output pin (MOTO1) is the pulse density modulated motor output signal. A 50% duty factor corresponds with the motor not actuated, higher duty factors mean acceleration, lower mean braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a 1 MHz internal clock signal. Possible application diagrams are illustrated in Fig.13.

7.12.1.2 PWM output mode (2-line)

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output. The motor braking signal is pulse-width modulated on the MOTO2 output. The timing is illustrated in Fig.14. A typical application diagram is illustrated in Fig.15.

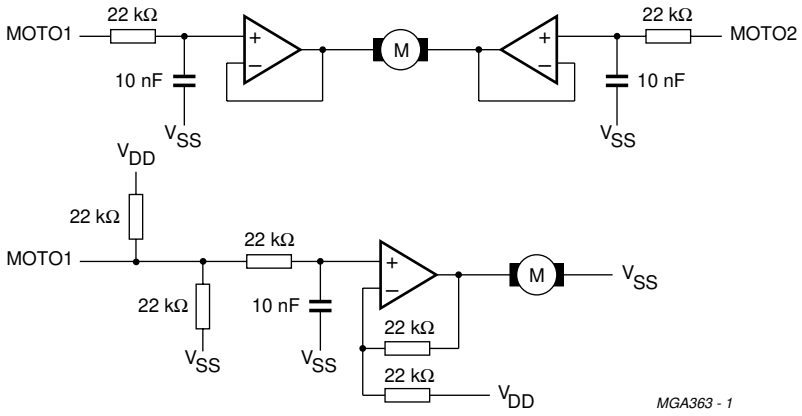

Fig.13 Motor pulse density application diagrams.

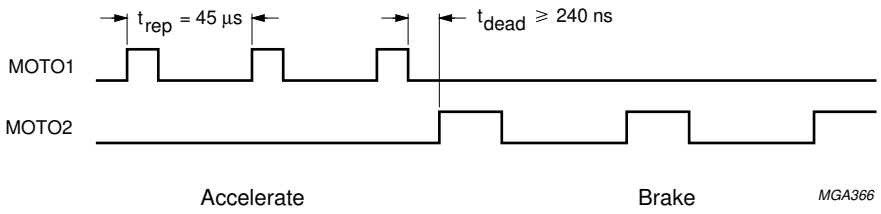

Fig.14 2-line PWM mode timing.

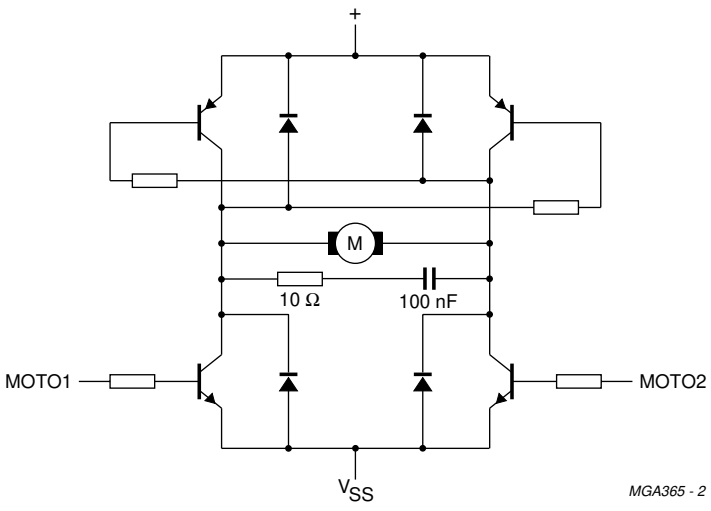

Fig.15 Motor 2-line PWM mode application diagram.

7.12.1.3 PWM output mode (4-line)

Using two extra outputs from the versatile pins interface, it is possible to use the SAA7377 with a 4-input motor bridge. The timing is illustrated in Fig.16. A typical application diagram is illustrated in Fig.17.

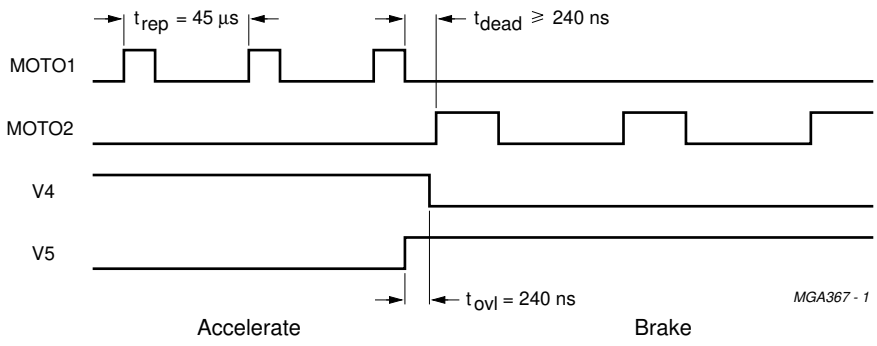

Fig.16 4-line PWM mode timing.

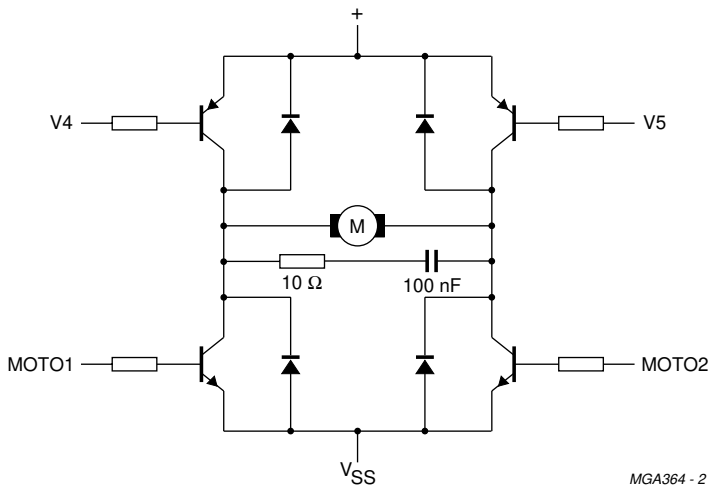

Fig.17 Motor 4-line PWM mode application diagram.

7.12.1.4 CDV/CAV output mode

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin (carrier frequency = 300 Hz). The PLL frequency signal will be put in pulse-density modulated form (carrier frequency = 4.23 MHz) on the MOTO2 pin. The integrated motor servo is disabled in this mode.

The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half full) will result in a PWM output of 60%.

7.12.2 SPINDLE MOTOR OPERATING MODES

The operation modes of the motor servo is controlled by register 1 (see Table 9).

In the SAA7377 decoder there is an anti-wind-up mode for the motor servo, selected via register 1. When the anti-wind-up mode is activated the motor servo integrator will hold if the motor output saturates.

7.12.2.1 Power limit

In start mode 1, start mode 2, stop mode 1 and stop mode 2, a fixed positive or negative voltage is applied to the motor.

This voltage can be programmed as a percentage of the maximum possible voltage, via register 6, to limit current drain during start and stop. The following power limits are possible;

100% (no power limit), 75%, 50%, or 37% of maximum.

7.12.3 LOOP CHARACTERISTICS

The gain and crossover frequencies of the motor control loop can be programmed via registers 4 and 5.
The following parameter values are possible;

Gains: 3.2, 4.0, 6.4, 8.0, 12.8, 16, 25.6 and 32

Crossover frequency f_4: 0.5 Hz, 0.7 Hz, 1.4 Hz, 2.8 Hz

Crossover frequency f_3: 0.85 Hz, 1.71 Hz, 3.42 Hz.

7.12.4 FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g. as a result of motor rotational shock), the FIFO will be automatically reset to 50% and the audio interpolator tries to conceal as much as possible to minimise the effect of data loss.

Table 9 Operating modes

MODE	DESCRIPTION
Start mode 1	The disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microcontroller.
Start mode 2	The disc is accelerated as in start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to jump mode. The motor status signals selectable via register 2 are valid.
Jump mode	Motor servo enabled but FIFO kept reset at 50%, integrator is held. The audio is muted but it is possible to read the subcode.
Jump mode 1	Similar to jump mode but motor integrator is kept at zero. Used for long jumps where there is a large change in disc speed.
Play mode	FIFO released after resetting to 50%. Audio mute released.
Stop mode 1	Disc is braked by applying a negative voltage to the motor. No decisions are involved.
Stop mode 2	The disc is braked as in stop mode 1 but the PLL will monitor the disc speed. As soon as the disc reaches 12% (or 6%, depending on the programmed brake percentage, via register E) of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to Off mode.
Off mode	Motor not steered.

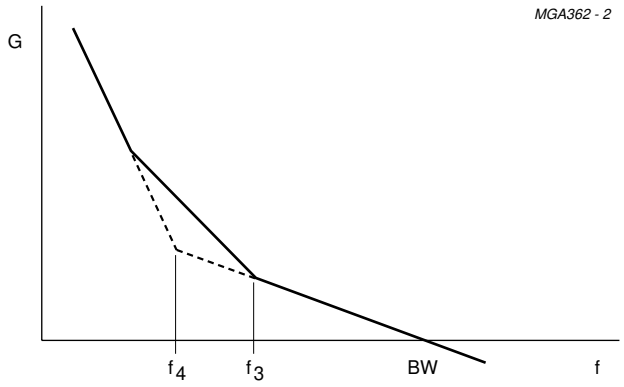

Fig.18 Motor servo mode diagram.

7.13 Servo part

7.13.1 DIODE SIGNAL PROCESSING

The photo detector in conventional two-stage three-beam compact disc systems normally contains six discrete diodes. Four of these diodes (three for single Foucault systems) carry the central aperture signal (CA) while the other two diodes (satellite diodes) carry the radial tracking information. The CA signal is processed into an HF signal (for the decoder function) and LF signal (information for the focus servo loop) before it is supplied to the SAA7377.

The analog signals from the central and satellite diodes are converted into a digital representation using analog-to-digital converters (ADCs). The ADCs are designed to convert unipolar currents into a digital code. The dynamic range of the input currents is adjustable within a given range, which is dependent on the value of the external resistor connected to pin I_{refT}. The maximum current for the central diodes and satellite diodes is given in the following formulae;

$$I_{in\,(max,\,central)} = \left(\frac{2.4 \times 10^6}{R_{IrefT}}\right)\ \mu A$$

$$I_{in\,(max,\,satellite)} = \left(\frac{1.2 \times 10^6}{R_{IrefT}}\right)\ \mu A$$

The V_{RH} voltage is internally generated by control circuitry which ensures that the V_{RH} voltage is adjusted depending on the spread of internal capacitors, using the reference current generated by the external resistor on I_{refT}. In the application V_{RL} is connected to V_{SSA1}. The maximum input currents for a range of resistors is given Table 10.

Table 10 Maximum current input

R_{IrefT} (kΩ)	DIODE INPUT CURRENT RANGE	
	D1 TO D4 (μA)	R1 AND R2 (μA)
220	10.909	5.455
240	10.000	5.000
270	8.889	4.444
300	8.000	4.000
330	7.273	3.636
360	6.667	3.333
390	6.154	3.077
430	5.581	2.791
470	5.106	2.553
510	4.706	2.353
560	4.286	2.143
620	3.871	1.935

This mode of V_{RH} automatic adjustment can be selected by the preset latch command.

Alternatively, the dynamic range of the input currents can be made dependent on the ADC reference voltages V_{RL} and V_{RH}. The maximum current for the central diodes and satellite diodes is given in the following formulae;

$$I_{in\,(max,\,central)} = f_{sys} \times (V_{RH} - V_{RL}) \times 1.0 \times 10^{-6}\ \mu A$$

$$I_{in\,(max,\,satellite)} = f_{sys} \times (V_{RH} - V_{RL}) \times 0.5 \times 10^{-6}\ \mu A$$

Where f_{sys} = 4.2336 MHz.

V_{RH} is generated internally, and there are 32 levels which can be selected under software control via the preset latch command. With this command the V_{RH} voltage can be set to 2.5 V then modified, decremented one level or incremented, by re-sending the command the required number of times. In the application V_{RL} is connected to V_{SSA1}.

7.13.2 Signal conditioning

The digital codes retrieved from the ADCs are applied to logic circuitry to obtain the various control signals. The signals from the central aperture diodes are processed to obtain a normalised focus error signal.

$$FE_n = \frac{D1 - D2}{D1 + D2} - \frac{D3 - D4}{D3 + D4}$$

where the detector set-up is assumed as shown in Fig.19.

In the event of single Foucault focusing method, the signal conditioning can be switched under software control such that the signal processing is as follows;

$$FE_n = 2 \times \frac{D1 - D2}{D1 + D2}$$

The error signal, FE_n, is further processed by a proportional integral and differential (PID) filter section.

A Focus OK (FOK) flag is generated by means of the central aperture signal and an adjustable reference level. This signal is used to provide extra protection for the track-loss (TL) generation, the focus start-up procedure and the drop out detection.

The radial or tracking error signal is generated by the satellite detector signals R1 and R2. The radial error signal can be formulated as follows;

$$RE_s = (R1 - R2) \times re\_gain + (R1 - R2) \times re\_offset$$

where the index ‘s’ indicates the automatic scaling operation which is performed on the radial error signal. This scaling is necessary to avoid non-optimum dynamic range usage in the digital representation and reduces the radial bandwidth spread. Furthermore, the radial error signal will be made free from offset during start up of the disc.

The four signals from the central aperture detectors, together with the satellite detector signals generate a track position signal (TPI) which can be formulated as follows;

TPI = sign [(D1 + D2 + D3 + D4) − (R1 + R2) × sum_gain]

Where the weighting factor sum_gain is generated internally by the SAA7377 during initialization.

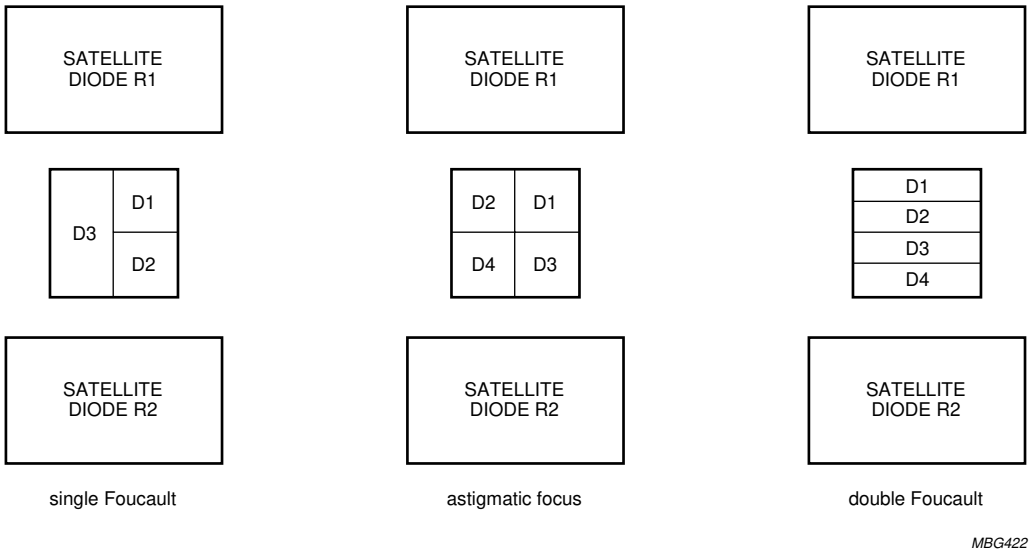

Fig.19 Detector arrangement.

7.13.3 FOCUS SERVO SYSTEM

7.13.3.1 Focus start-up

Five initially loaded coefficients influence the start-up behaviour of the focus controller. The automatically generated triangle voltage can be influenced by 3 parameters; for height (ramp_height) and DC offset (ramp_offset) of the triangle and its steepness (ramp_incr).

For protection against false focus point detections two parameters are available which are an absolute level on the CA-signal (CA_start) and a level on the FE_n signal (FE_start). When this CA level is reached the FOK signal becomes true.

If the FOK signal is true and the level on the FE_n signal is reached, the focus PID is enabled to switch on when the next zero crossing is detected in the FE_n signal.

7.13.3.2 Focus position control loop

The focus control loop contains a digital PID controller which has 5 parameters which are available to the user. These coefficients influence the integrating (foc_int), proportional (foc_lead_length, part of foc_parm3) and differentiating (foc_pole_lead, part of foc_parm1) action of the PID and a digital low-pass filter (foc_pole_noise, part of foc_parm2) following the PID. The fifth coefficient foc_gain influences the loop gain.

7.13.3.3 Drop-out detection

This detector can be influenced by one parameter (CA_drop). The FOK signal will become false and the integrator of the PID will hold if the CA signal drops below this programmable absolute CA level. When the FOK signal becomes false it is assumed, initially, to be caused by a black dot.

7.13.3.4 Focus loss detection and fast restart

Whenever FOK is false for longer than approximately 3 ms, it is assumed that the focus point is lost. A fast restart procedure is initiated which is capable of restarting the focus loop within 200 to 300 ms depending on the programmed coefficients of the microcontroller.

7.13.3.5 Focus loop gain switching

The gain of the focus control loop (foc_gain) can be multiplied by a factor of 2 or divided by a factor of 2 during normal operation. The integrator value of the PID is corrected accordingly. The differentiating (foc_pole_lead) action of the PID can be switched at the same time as the gain switching is performed.

7.13.3.6 Focus automatic gain control loop

The loop gain of the focus control loop can be corrected automatically to eliminate tolerances in the focus loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

7.13.4 RADIAL SERVO SYSTEM

7.13.4.1 Level initialization

During start-up an automatic adjustment procedure is activated to set the values of the radial error gain (re_gain), offset (re_offset) and satellite sum gain (sum_gain) for TPI level generation. The initialization procedure runs in a radial open loop situation and is ≤ 300 ms. This start-up time period may coincide with the last part of the motor start-up time period.

Automatic gain adjustment: as a result of this initialization the amplitude of the RE signal is adjusted to within ±10% around the nominal RE amplitude.

Offset adjustment: the additional offset in RE due to the limited accuracy of the start-up procedure is less than ± 50 nm.

TPI level generation: the accuracy of the initialization procedure is such that the duty factor range of TPI becomes 0.4 < duty factor < 0.6 (definition of duty factor = TPI HIGH/TPI period).

7.13.4.2 Sledge control

The microcontroller can move the sledge in both directions via the steer sledge command.

7.13.4.3 Tracking control

The actuator is controlled using a PID loop filter with user defined coefficients and gain. For stable operation between the tracks, the S-curve is extended over ± 0.75 of the track. On request from the microcontroller, S-curve extension over ± 2.25 tracks is used, automatically changing to access control when exceeding those 2.25 tracks.

Both modes of S-curve extension make use of a track-count mechanism. In this mode, track counting results in an ‘automatic return-to-zero track’, to avoid major music rhythm disturbances in the audio output for improved shock resistance.

The sledge is continuously controlled, or provided with step pulses to reduce power consumption using the filtered value of the radial PID output. Alternatively, the microcontroller can read the average voltage on the radial actuator and provide the sledge with step pulses to reduce power consumption. Filter coefficients of the continuous sledge control can be preset by the user.

7.13.4.4 Access

The access procedure is divided into two different modes (see Table 11), depending on the requested jump size.

Table 11 Access modes

ACCESS TYPE	JUMP SIZE(1)	ACCESS SPEED
Actuator jump	1 - brake_distance	decreasing velocity
Sledge jump	brake_distance - 32768	maximum power to sledge(1)

Note

1. Microcontroller presettable.

The access procedure makes use of a track counting mechanism, a velocity signal based on a fixed number of tracks passed within a fixed time interval, a velocity set point calculated from the number of tracks to go and a user programmable parameter indicating the maximum sledge performance.

If the number of tracks remaining is greater than the brake_distance then the sledge jump mode should be activated, or, the actuator jump should be performed. The requested jump size together with the required sledge breaking distance at maximum access speed defines the brake_distance value.

During the actuator jump mode, velocity control with a PI controller is used for the actuator. The sledge is then continuously controlled using the filtered value of the radial PID output. All filter parameters (for actuator and sledge) are user programmable.

In the sledge jump mode maximum power (user programmable) is applied to the sledge in the correct direction while the actuator becomes idle (the contents of the actuator integrator leaks to zero just after the sledge jump mode is initiated).

7.13.4.5 Radial automatic gain control loop

The loop gain of the radial control loop can be corrected automatically to eliminate tolerances in the radial loop. This gain control injects a signal into the loop which is used to correct the loop gain. Since this decreases the optimum performance, the gain control should only be activated for a short time (for example, when starting a new disc).

This gain control differs from the level initialization. The level initialization should be performed first. The disadvantage of using the level initialization without the gain control is that only tolerances from the front-end are reduced.

7.13.5 OFF-TRACK COUNTING

The track position signal (TPI) is a flag which is used to indicate whether the radial spot is positioned on the track, with a margin of $\pm 1/4$ of the track-pitch. In combination with the radial polarity flag (RP) the relative spot position over the tracks can be determined. These signals are, however, afflicted with some uncertainties caused by;

- Disc defects such as scratches and fingerprints
- The HF information on the disc, which is considered as noise by the detector signals.

In order to determine the spot position with sufficient accuracy, extra conditions are necessary to generate a track loss signal (TL) and an off-track counter value. These extra conditions influence the maximum speed and this implies that, internally, one of the following three counting states is selected;

1. Protected state: used in normal play situations. A good protection against false detection caused by disc defects is important in this state.
2. Slow counting state: used in low velocity track jump situations. In this state a fast response is important rather than the protection against disc defects (if the phase relationship between TL and RP of $1/2\pi$ radians is affected too much, the direction cannot then be determined accurately).
3. Fast counting state: used in high velocity track jump situations. Highest obtainable velocity is the most important feature in this state.