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DATA SHEET

SAA7706H
Car radio Digital Signal Processor (DSP)

Product specification
File under Integrated Circuits, IC01

2001 Mar 05

Philips
Semiconductors

PHILIPS

CONTENTS

Car radio Digital Signal Processor (DSP) SAA7706H

1 FEATURES

1.1 Hardware

- 5-bitstream 3rd-order sigma-delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filter
- 1-bitstream 1st-order sigma-delta ADC with anti-aliasing broadband input filter
- 4-bitstream Digital-to-Analog Converters (DACs) with 128-fold oversampling and noise shaping
- Integrated semi-digital filter; no external post filter required for DAC
- Dual media support: allowing separate front-seat and rear-seat signal sources and separate control
- Simultaneous radio and audio processing
- Digital FM stereo decoder
- Digital FM interference suppression
- RDS demodulation via separate ADC; with buffered output option
- Two mono Common-Mode Rejection Ratio (CMRR) input stages for voice signals from phone and navigation inputs
- Phone and navigation mixing at DAC front outputs
- Two stereo CMRR input stages (CD-walkman and CD-changer etc.)
- Analog single-ended TAPE and AUX input
- Separate AM-left and AM-right inputs in the event of use of external AM stereo decoder
- One digital input: I^{2}S-bus or LSB-justified format
- Two digital inputs: SPDIF format
- Co-DSP support via I^{2}S-bus or LSB-justified format
- Audio output short-circuit protected
- I^{2}C-bus controlled (including fast mode)
- MOST bus interfacing (details in separate manual)
- Phase-locked loop derives the internal clocks from one common fundamental crystal oscillator
- Combined AM/FM level input
- Pin compatible with SAA7705 and SAA7708
- All digital inputs are tolerant of 5 V input levels
- All analog inputs have high GSM immunity
- Low number of external components required
- –40 to +85 °C operating temperature range
- Easy applicable.

1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter; de-emphasis and stereo detection
- Electronic adjustments: FM or AM level, FM channel separation, Dolby®(1) level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Four channel 5-band parametric equalizer
- 9-bands mono audio spectrum analyzer
- Extended beep functions with tone sequencer for phone rings
- Large volume jumps e-power interpolated to prevent zipper noise
- Dual media support; allowing separate front-seat and rear-seat signal sources and separate control
- Dynamic loudness or bass boost
- Audio level monitor
- Tape equalization and Music Search System (MSS) detection for tape
- Dolby-B tape noise reduction (at 44.1 kHz only)
- Dynamics compression available in all modes
- CD de-emphasis processing
- Voice-over possibility for phone and navigation signals
- Improved AM signal processing
- Digital AM CQUAM stereo decoder (not in all rom_codes available)
- Digital AM interference suppression
- Soft audio mute
- RDS update processing: pause detection, mute and signal-quality sensor-freeze
- General purpose tone generator

(1) **Dolby** — Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. Dolby is a registered trade-mark of Dolby Laboratories Licensing Corporation.

- Noise generator allows for frequency response measurements
- Boot-up ROM for fast start-up
- Signal level, noise and multipath detection for AM or FM signal quality information
- AM co-channel and adjacent channel detection (not in all rom_codes available).

2 APPLICATIONS

- High-end car radio systems.

3 GENERAL DESCRIPTION

The SAA7706H performs all the signal functions in front of the power amplifiers and behind the car radio tuner AM and FM outputs and the CD, tape and phone inputs. These functions are:

- Interference absorption
- Stereo decoding for FM and AM (stereo)
- RDS-demodulation
- FM and AM weak signal processing (soft mute, sliding stereo and high cut)
- Dolby-B tape noise reduction
- CD de-emphasis function
- Audio controls for volume, balance, fader, tone and dynamics compression.

Some functions have been implemented in hardware (FM stereo decoder, RDS-demodulator and FM Interference Absorption Circuit (IAC) and are not freely programmable.

Digital audio signals from external sources with the Philips I^2S-bus and the LSB-justified 16, 18, 20 and 24 bits format or SPDIF format are accepted.

The big advantage of this SAA7706H device is the ‘dual media support’; this enables independent front seat and rear seat audio sources and control.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	operating supply voltage	all V_{DD} pins with respect to V_{SS}	3	3.3	3.6	V
I_{DDD}	supply current of the digital part	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	110	150	mA
I_{DDA}	supply current of the analog part	zero input and output signal	–	40	60	mA
P_{tot}	total power dissipation	DSP1 at 50 MHz; DSP2 at 62.9 MHz	–	540	750	mW
FM_MPX input						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)	THD < 1%; VOLFM = 00H	0.33	0.368	–	V
THD	total harmonic distortion	input signal 0.368 V (RMS) at 1 kHz; bandwidth = 19 kHz; VOLFM = 00H	–	–70	–65	dB
			–	0.03	0.056	%
S/N	signal-to-noise ratio input stereo	input signal at 1 kHz; bandwidth = 40 kHz; 0 dB reference = 0.368 V (RMS); VOLFM = 00H	75	81	–	dB
CD, TAPE, AUX and AM inputs						
$V_{i(con)(max)(rms)}$	maximum conversion input level (RMS value)	THD < 1%	0.6	0.66	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	input signal 0.55 V (RMS) at 1 kHz; bandwidth = 20 kHz	–	–85	–75	dB
S/N	signal-to-noise ratio	input signal at 1 kHz; bandwidth = 20 kHz; 0 dB reference = 0.55 V (RMS)	85	90	–	dB
FSDAC						
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio (measured with system one)	at 0 dB	–	–90	–85	dB
		at –60 dB; A-weighted	–	–37	–	dB
S/N	signal-to-noise ratio (measured with system one)	code = 0; A-weighted	–	105	–	dB
Crystal oscillator						
f_{xtal}	crystal frequency		–	11.2896	–	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7706H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT318-2

6 BLOCK DIAGRAM

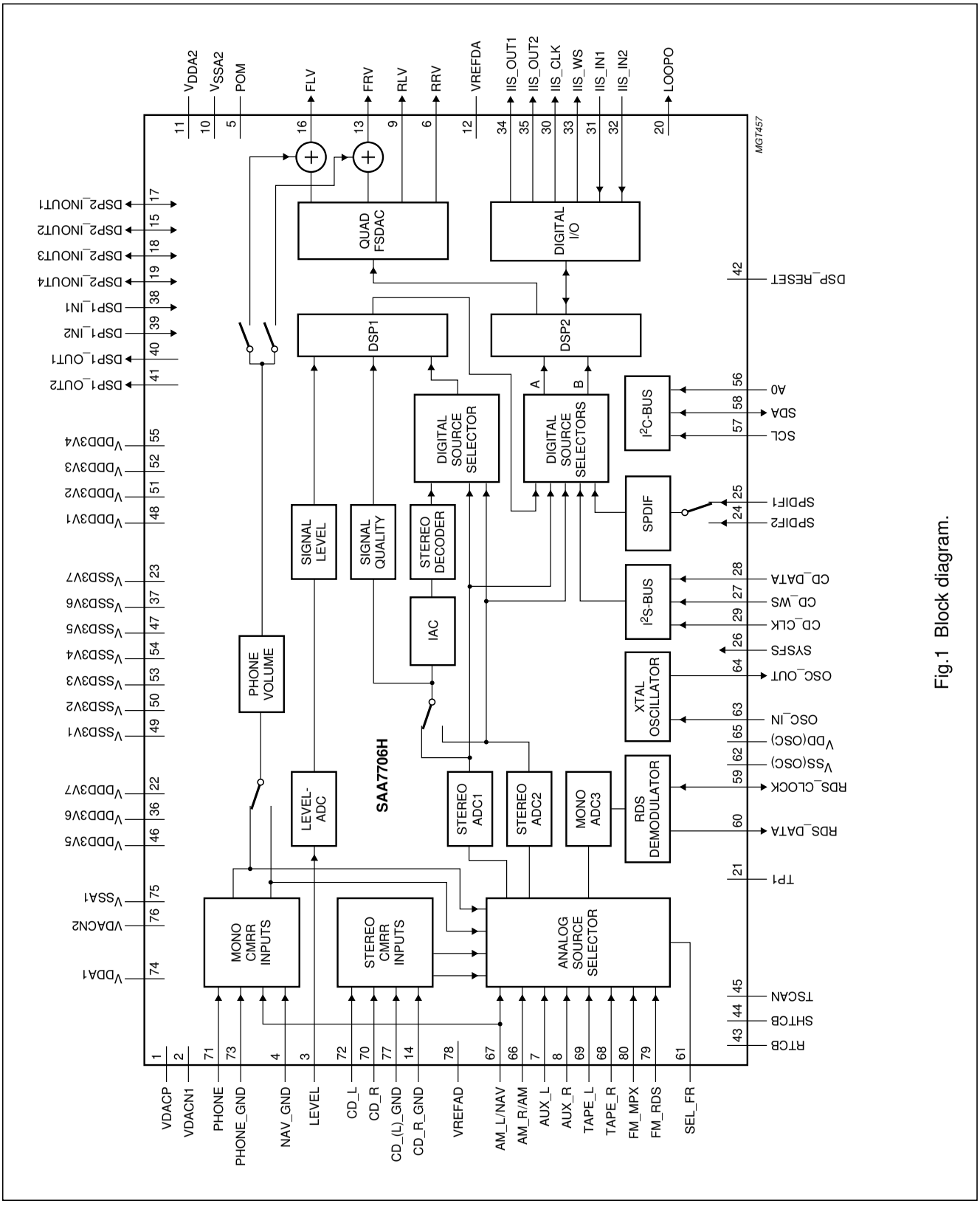


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	PIN TYPE	DESCRIPTION
VDACP	1	apio	positive reference voltage ADC1, ADC2, ADC3 and level-ADC
VDACN1	2	apio	ground reference voltage ADC1
LEVEL	3	apio gsmcap	LEVEL input pin; via this pin the level of the FM signal or level of the AM signal is fed to the DSP1; the level information is used in the DSP1 for dynamic signal processing
NAV_GND	4	apio gsmcap	common mode reference input pin of the navigation signal (pin AM_L/NAV)
POM	5	apio	power-on mute of the QFSDAC; timing is determined by an external capacitor
RRV	6	apio	rear; right audio output of the QFSDAC
AUX_L	7	apio	left channel of analog AUX input
AUX_R	8	apio	right channel of analog AUX input
RLV	9	apio	rear; left audio output of the QFSDAC
V_{SSA2}	10	vssco	ground supply analog part of the QFSDAC and SPDIF bitslicer
V_{DDA2}	11	vddco	positive supply analog part of the QFSDAC and SPDIF bitslicer
VREFDA	12	apio	voltage reference of the analog part of QFSDAC
FRV	13	apio	front; right audio output of the QFSDAC
CD_R_GND	14	apio	common-mode reference input pin for analog CD_R or TAPE_R in the event of separated ground reference pins for left and right are used
DSP2_INOUT2	15	bpts5thdt5v	flag input/output 2 of the DSP2-core (DSP2-flag) I²C-bus configurable
FLV	16	apio	front; left audio voltage output of the QFSDAC
DSP2_INOUT1	17	bpts5thdt5v	flag input/output 1 of the DSP2-core (DSP2-flag) I²C-bus configurable
DSP2_INOUT3	18	bpts5thdt5v	flag input/output 3 of the DSP2-core (DSP2-flag) I²C-bus configurable
DSP2_INOUT4	19	bpts5thdt5v	flag input/output 4 of the DSP2-core (DSP2-flag) I²C-bus configurable
LOOPO	20	bpts5tht5v	SYSCLK output ($256f_s$)
TP1	21	ipthdt5v	for test purpose only; this pin may be left open or connected to ground
V_{DDD3V7}	22	vdde	positive supply (peripheral cells only)
V_{SSD3V7}	23	vsse	ground supply (peripheral cells only)
SPDIF2	24	apio	SPDIF input 2; can be selected instead of SPDIF1 via I²C-bus bit
SPDIF1	25	apio	SPDIF input 1; can be selected instead of SPDIF2 via I²C-bus bit
SYSFS	26	ipthdt5v	system f_s clock input
CD_WS	27	ipthdt5v	digital CD-source word select input; I²S-bus or LSB-justified format
CD_DATA	28	bpts10thdt5v	digital CD-source left-right data input; I²S-bus or LSB-justified format
CD_CLK	29	ipthdt5v	digital CD-source clock input I²S-bus or LSB-justified format
IIS_CLK	30	ots10ct5v	clock output for external I²S-bus receiver; for example headphone or subwoofer
IIS_IN1	31	ipthdt5v	data 1 input for external I²S-bus transmitter; e.g. audio co-processor
IIS_IN2	32	ipthdt5v	data 2 input for external I²S-bus transmitter; e.g. audio co-processor
IIS_WS	33	ots10ct5v	word select output for external I²S-bus receiver; for example headphone or subwoofer
IIS_OUT1	34	ots10ct5v	data 1 output for external I²S-bus receiver or co-processor
IIS_OUT2	35	ots10ct5v	data 2 output for external I²S-bus receiver or co-processor

SYMBOL	PIN	PIN TYPE	DESCRIPTION
V_{DDD3V6}	36	vdde	positive supply (peripheral cells only)
V_{SSD3V6}	37	vsse	ground supply (peripheral cells only)
DSP1_IN1	38	bpts10thdt5v	flag input 1 of the DSP1-core
DSP1_IN2	39	bpts10thdt5v	flag input 2 of the DSP1-core
DSP1_OUT1	40	op4mc	flag output 1 of the DSP1-core
DSP1_OUT2	41	op4mc	flag output 2 of the DSP1-core
DSP_RESET	42	iptut5v	general reset of chip (active LOW)
RTCB	43	ipthdt5v	asynchronous reset test control block; connect to ground (internal pull-down)
SHTCB	44	ipthdt5v	shift clock test control block (internal pull-down)
TSCAN	45	ipthdt5v	scan control active high (internal pull-down)
V_{DDD3V5}	46	vdde	positive supply (peripheral cells only)
V_{SSD3V5}	47	vsse	ground supply (peripheral cells only)
V_{DDD3V1}	48	vddi	positive supply (core only)
V_{SSD3V1}	49	vssis	ground supply (core only)
V_{SSD3V2}	50	vssco	ground supply (core only)
V_{DDD3V2}	51	vddco	positive supply (core only)
V_{DDD3V3}	52	vddco	positive supply (core only)
V_{SSD3V3}	53	vssco	ground supply (core only)
V_{SSD3V4}	54	vssis	ground supply (core only)
V_{DDD3V4}	55	vddi	positive supply (core only)
A0	56	ipthdt5v	slave sub-address I^2C-bus selection or serial data input test control block
SCL	57	iptht5v	serial clock input I^2C-bus
SDA	58	iic400kt5v	serial data input/output I^2C-bus
RDS_CLOCK	59	bpts10tht5v	radio data system bit clock output or RDS external clock input I^2C-bus bit controlled
RDS_DATA	60	ops10c	radio data system data output
SEL_FR	61	iptht5v	AD input selection switch to enable high ohmic FM_MPX input at fast tuner search on FM_RDS input
$V_{SS(OSC)}$	62	vssco	ground supply (crystal oscillator only)
OSC_IN	63	apio	crystal oscillator input
OSC_OUT	64	apio	crystal oscillator output
$V_{DD(OSC)}$	65	vddco	positive supply (crystal oscillator only)
AM_R/AM	66	apio gsmcap	right channel AM audio frequency or AM input in the event of mono; analog input pin
AM_L/NAV	67	apio gsmcap	left channel AM audio frequency or input of common mode navigation signal; analog input pin
TAPE_R	68	apio gsmcap	right channel of analog TAPE input
TAPE_L	69	apio gsmcap	left channel of analog TAPE input
CD_R	70	apio gsmcap	right channel of analog CD input
PHONE	71	apio gsmcap	common mode PHONE signal, analog input pin
CD_L	72	apio gsmcap	left channel of analog CD input

SYMBOL	PIN	PIN TYPE	DESCRIPTION
PHONE_GND	73	apio gsmcap	common mode reference input pin of the PHONE signal
V_{DDA1}	74	vddco	positive supply analog (ADC1, ADC2, ADC3 and level-ADC only)
V_{SSA1}	75	vssco	ground supply analog (ADC3 and level-ADC only)
VDACN2	76	apio	ground reference voltage (ADC2)
CD_(L)_GND	77	apio gsmcap	common mode reference input pin for analog CD or TAPE or in the event of separated ground reference pins used for CD_L or TAPE_L
VREFAD	78	apio	common mode reference voltage ADC1, ADC2, ADC3 and level-ADC
FM_RDS	79	apio gsmcap	FM RDS signal; analog input pin
FM_MPX	80	apio gsmcap	FM multiplex signal; analog input pin

Table 1 Brief explanation of used pin types

PIN TYPE	EXPLANATION
apio	3-state I/O analog; I/O pad cell; actually pin type vddco
apio gsmcap	3-state I/O analog; I/O pad cell; actually pin type vddco with high GSM immunity
bpts5thdt5v	43 MHz bidirectional pad; push-pull input; 3-state output; 5 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant
bpts10tht5v	21 MHz bidirectional pad; push-pull input; 3-state output; 10 ns slew rate control; TTL; hysteresis; 5 V tolerant
bpts10thdt5v	21 MHz bidirectional pad; push-pull input; 3-state output; 10 ns slew rate control; TTL; hysteresis; pull-down; 5 V tolerant
iic400kt5v	I^2C-bus pad; 400 kHz I^2C-bus specification; TTL; 5 V tolerant
ipthtt5v	input pad buffer; TTL; hysteresis; 5 V tolerant
ipthdt5v	input pad buffer; TTL; hysteresis; pull-down; 5 V tolerant
iptut5v	input pad buffer; TTL; pull-up; 5 V tolerant
op4mc	output pad buffer; 4 mA output drive; CMOS; slew rate control; 50 MHz
ots10ct5v	output pad buffer; 3-state, 10 ns slew rate control; CMOS; 5 V tolerant
ops10c	output pad buffer; 4 mA output drive; CMOS; slew rate control; 21 MHz
vdde	V_{DD} supply peripheral only
vsse	V_{SS} supply peripheral only
vddco	V_{DD} supply to core only
vssco	V_{SS} supply to core only (vssco does not connect the substrate)
vddi	V_{DD} supply to core and peripheral
vssis	V_{SS} supply to core and peripheral; with substrate connection

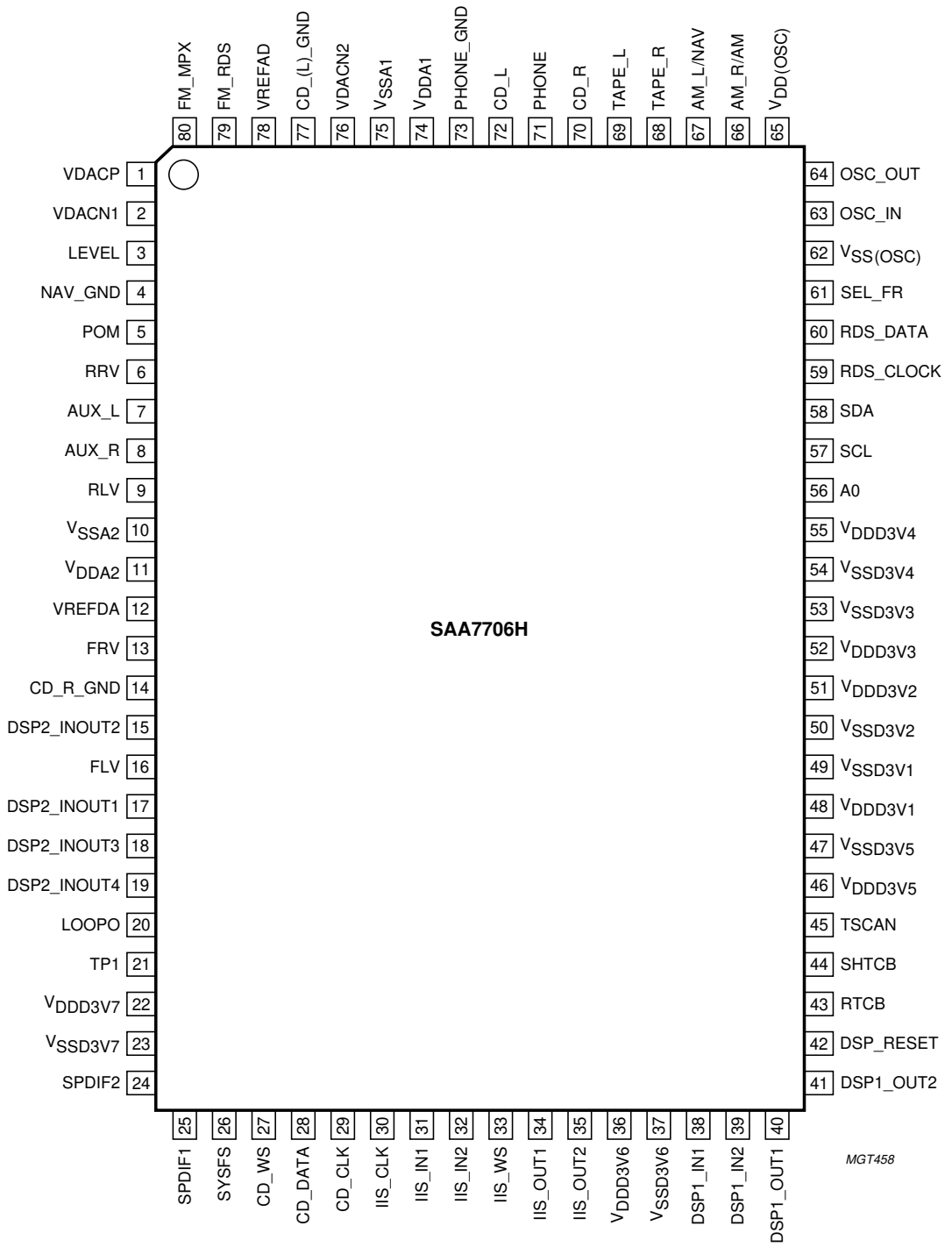


Fig.2 Pinning diagram.

8 FUNCTIONAL DESCRIPTION

8.1 Analog front-end

The analog front-end consists of two identical sigma-delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector. A mono version (ADC3) is added for handling RDS signals. Also a first-order sigma-delta ADC for tuner level information is incorporated.

The switches S1 and S2 select (see Fig.3) between the FM_MPX/FM_RDS and the CD, TAPE, AUX, AM, PHONE and NAV connection to ADC1 and ADC2. The inputs CD, TAPE, AUX, AM, PHONE and NAV can be selected with the audio input controls (AIC1/2). The ground reference (G0 and G1) can be selected to be able to handle common mode signals for CD or TAPE. The ground reference G0 is connected to an external pin and G1 is internally referenced (see Fig.4).

The PHONE and NAV inputs have their own CMRR input stage and can be redirected to ADC1/2 via the Audio Input Control (AIC). For pin compatibility with SAA7704, SAA7705 and SAA7708 the AM is combined with the NAV input. It is also possible to directly mix PHONE or NAV (controlled with MIXC) with the front FSDAC channels after volume control. The FM inputs (FM_MPX/FM_RDS) can be selected with external pin SEL_FR. The FM and RDS input sensitivity can be adjusted with VOLFM and VOLRDS via I^2C-bus.

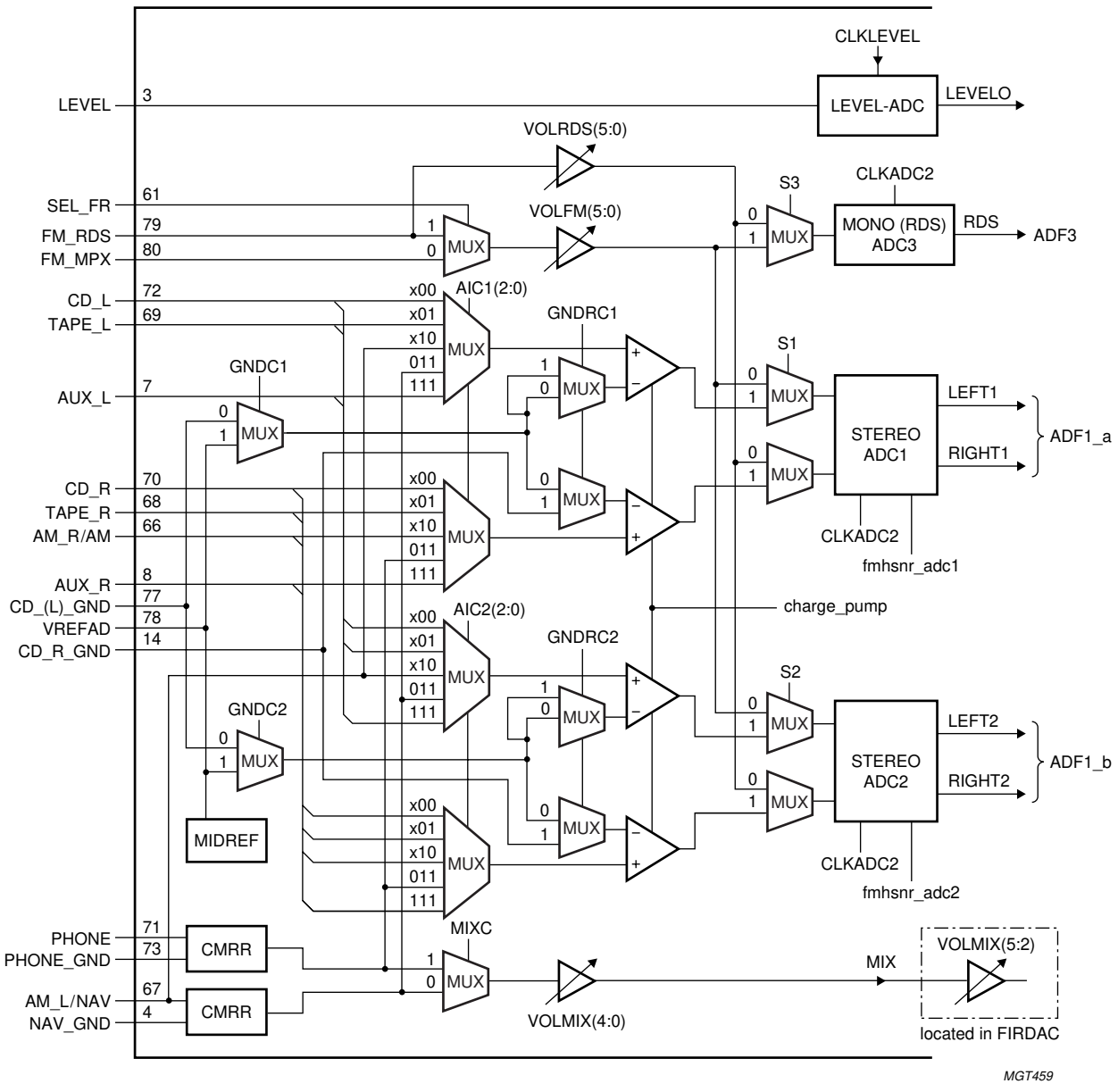


Fig.3 Analog front-end switch diagram.

8.1.1 THE REALIZATION OF COMMON MODE INPUT WITH AIC

A high common mode rejection ratio can be created by the use of the ground return pin. Pin CD_(L)_GND can be used in the case that the left and right channel have one ground return line. CD_(L)_GND and CD_R_GND can be used for separated left and right ground return lines. The ground return lines can be connected via the switch GNDC1/2 and GNDRC1/2 (see Fig.4) to the plus input of the second operational amplifier in the signal path. The signal of which a high common mode rejection ratio is required has a signal and a common signal as input. The common signal is connected to the CD_(L)_GND and/or CD_R_GND input. The actual input can be selected with audio input control AIC1/2(1:0).

In Fig.4 the CD input is selected. In this situation both signal lines going to S1/2 in front of the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio. The inputs CD_L and CD_R in this example are connected via an external resistor tap of 82 kΩ and 100 kΩ to be able to handle larger input signals. The 100 kΩ resistors are needed to provide a DC biasing of the operational amplifiers OA1 and OA2. The 1 MΩ resistor provides DC biasing of OA3 and OA4. If no external resistor tap is needed the resistors of 100 kΩ and 1 MΩ still have to provide DC biasing. Only the 82 kΩ resistor can be removed. The impedance level in combination with parasitic capacitance at input CD_L or CD_R determines for a great deal the achievable common rejection ratio.

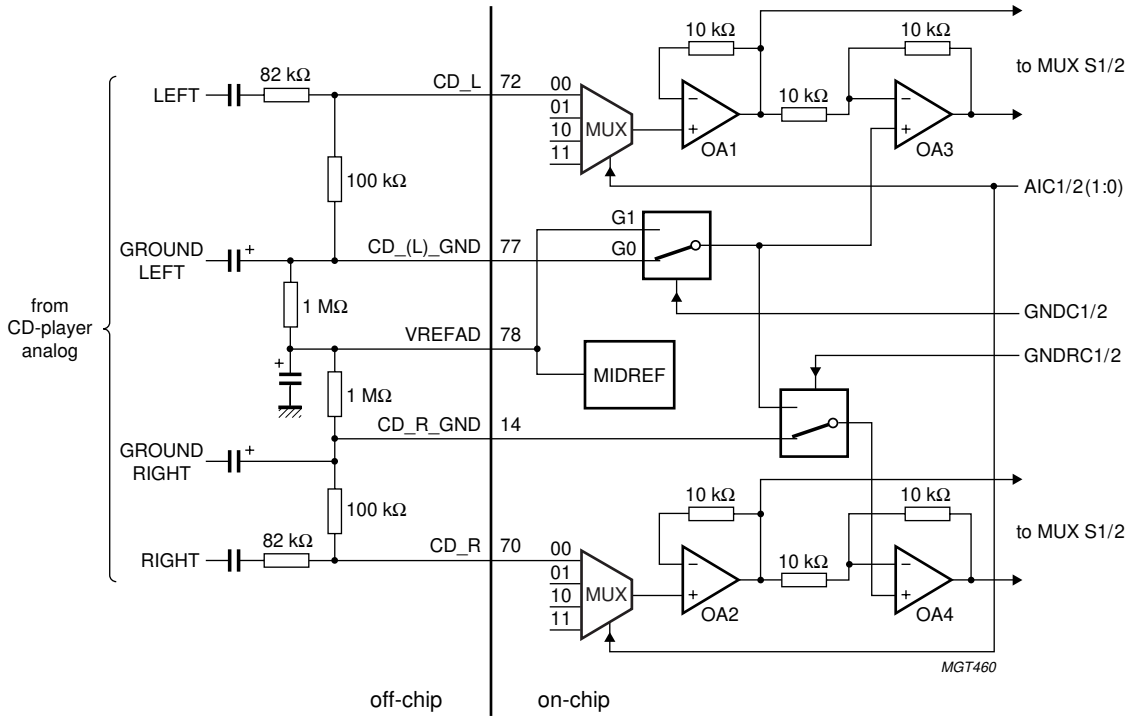


Fig.4 Example of the use of common mode analog input in combination with input resistor tap.

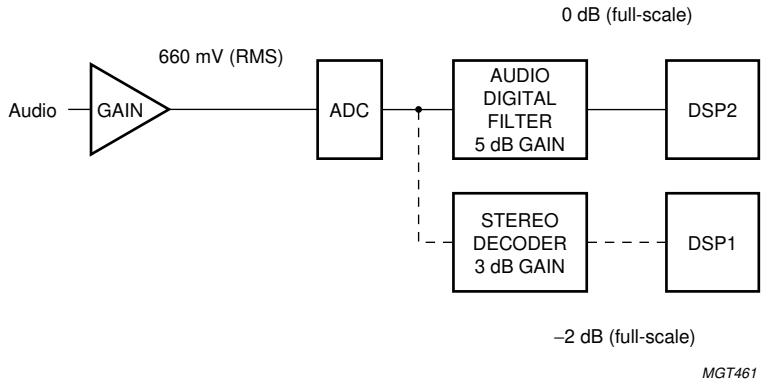


Fig.5 Audio gain through ADC and digital filter path to DSP.

8.1.2 Realization of the auxiliary input with volume control

A differential input with volume control for mixing to the front left or front right of both DAC outputs is provided. The inputs consist of a PHONE and NAV input. Both are accompanied with their ground return lines. After selection of PHONE or NAV the volume can be changed from about +18 to −22.5 dB in 27 steps and mute (MIX output). This signal can be added to the left and/or right front DAC channels.

The output signals of both input circuits can also be switched to ADC1 and/or ADC2, depending on the settings of audio input control 1 (AIC1) and audio input control 2 (AIC2), without volume control (see Fig.3).

8.1.3 Realization of the FM input control

The gain of the circuit has a maximum of 2.26 (7.08 dB). This results in an input level of 368 mV for full-scale, which means 0 dB (full-scale) at the DSP1 input via the stereo decoder (see Fig.6). The gain can be reduced in steps of 1.5 dB. When the gain is set to −3.4 dB the input level becomes 1229 mV for full-scale. This setting accounts for the 200 mV (RMS) input sensitivity at 22.5 kHz sweep and a saturation of the input at 138 kHz sweep.

RDS update: for RDS update the fast access pin SEL_FR must be made HIGH. In that case the FM_RDS signal also goes through the path that was set for FM_MPX. In this situation the signal must be obtained via the FM_RDS input and a noise sample can be retrieved. The input FM_MPX gets high-ohmic. Charging of the coupling capacitor connected to pin FM_MPX is no longer possible.

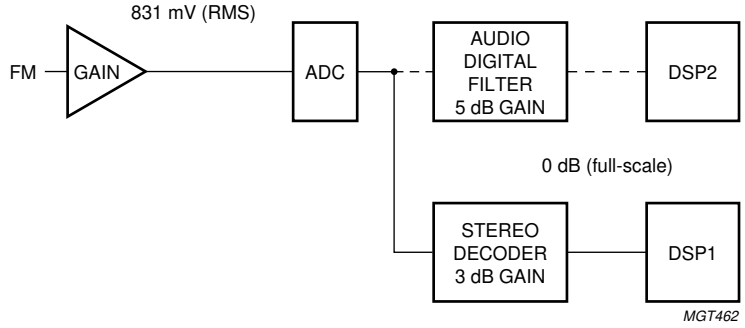


Fig.6 FM gain path through stereo decoder to DSP1.

8.1.4 PINS VDACN1, VDACN2 AND VDACP

These pins are used as negative and positive reference for the ADC1, 2, 3 and the level-ADC. They have to be directly connected to the V_{SSA1} and filtered V_{DDA1} for optimal performance (see Figs 25 and 26).

8.1.5 PIN VREFAD

Via this pin the midref voltage of the ADCs is filtered. This midref voltage is used as half supply voltage reference of the ADCs. External capacitors (connected to V_{SSA1}) prevent crosstalk between switch cap DACs of the ADCs and buffers and improves the power supply rejection ratio of all components. This pin is also used in the application as reference for the inputs TAPE and CD (see Fig.4). The voltage on pin VREFAD is determent by the voltage on pins VDACP and VDACN1 or VDACN2 and is found as:

$$V_{VREFAD} = \frac{V_{VDACP} - V_{VDACN1,2}}{2}$$

8.1.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering. These pins are V_{SSA1} for the analog ground and V_{DDA1} for the analog power supply.

8.2 The signal audio path for input signals CD, TAPE, AUX, PHONE, NAV and AM

The left and right channels are converted and down-sampled by the ADF1_a, ADF1_b. This data stream is converted into a serial format and fed to the DSP1 and DSP2 source selectors. In Figs 7 and 8 the overall and detailed frequency response curves of the analog-to-digital audio decimation path based on a 44.1 kHz sample frequency are shown.

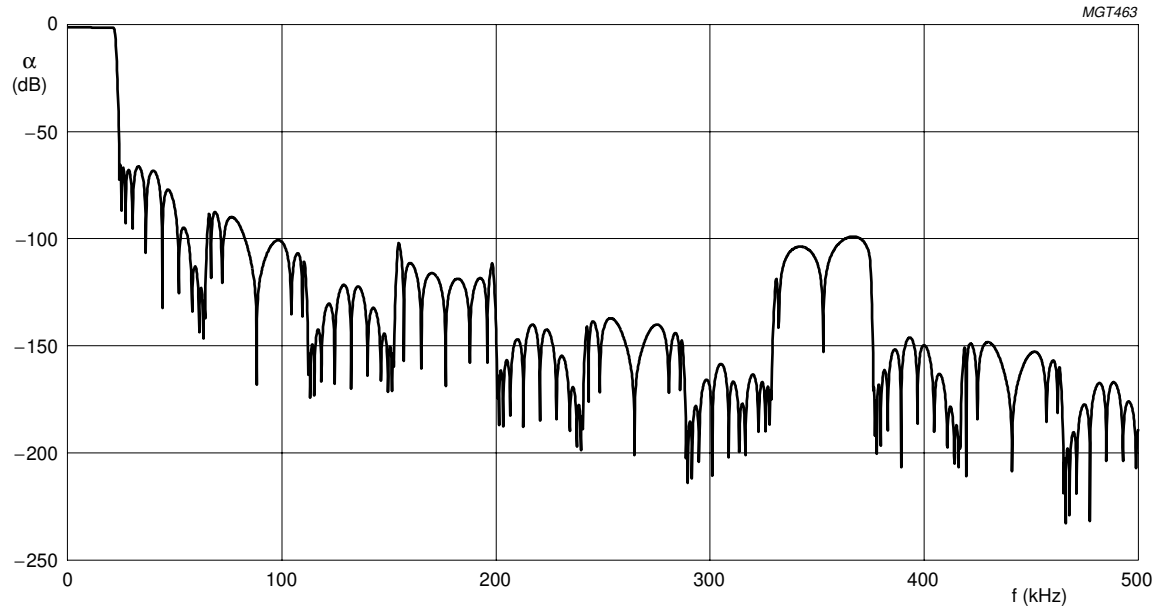


Fig.7 Overall frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

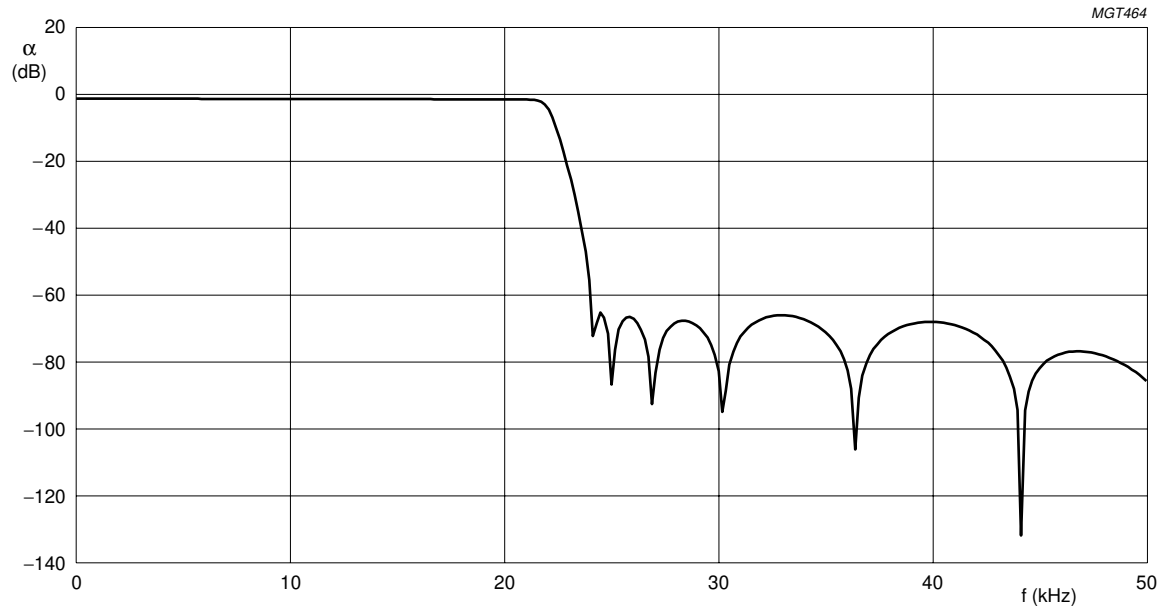


Fig.8 Detailed frequency response curve analog-to-digital audio path decimation based on a 44.1 kHz sample frequency.

8.3 Signal path for level information

For FM weak signal processing, for AM and FM purposes (absolute level and multipath) a level input is implemented (pin LEVEL). In the event of radio reception the clocking of the filters and the level-ADC is based on a 38 kHz sampling frequency. A DC input signal is converted by a bitstream sigma-delta ADC followed by a decimation filter.

The input signal has to be obtained from a radio part. The tuner must deliver the level information of either AM or FM to pin LEVEL.

The input signal for level must be in the range 0 to 3.3 V ($V_{VDACP} - V_{VDACN}$). The 9-bit level-ADC converts this input voltage in steps with a resolution better than at least 14 mV over the 3.3 V range.

The tolerance on the gain is less than 2%. The MSB is always logic 0 to represent a positive level. Input level span can be increased by an external resistor tap. The high input impedance of the level-ADC makes this possible.

The decimation filter reduces in the event of an 38 kHz based clocking regime the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz with a resulting f_s = 76 kHz. The response curve is given in Fig.9.

The level information is sub-sampled by the DSP1 to obtain a field strength and a multipath indication. These values are stored in the coefficient or data RAM. Via the I^2C-bus they can be read and used in other microcontroller programs.

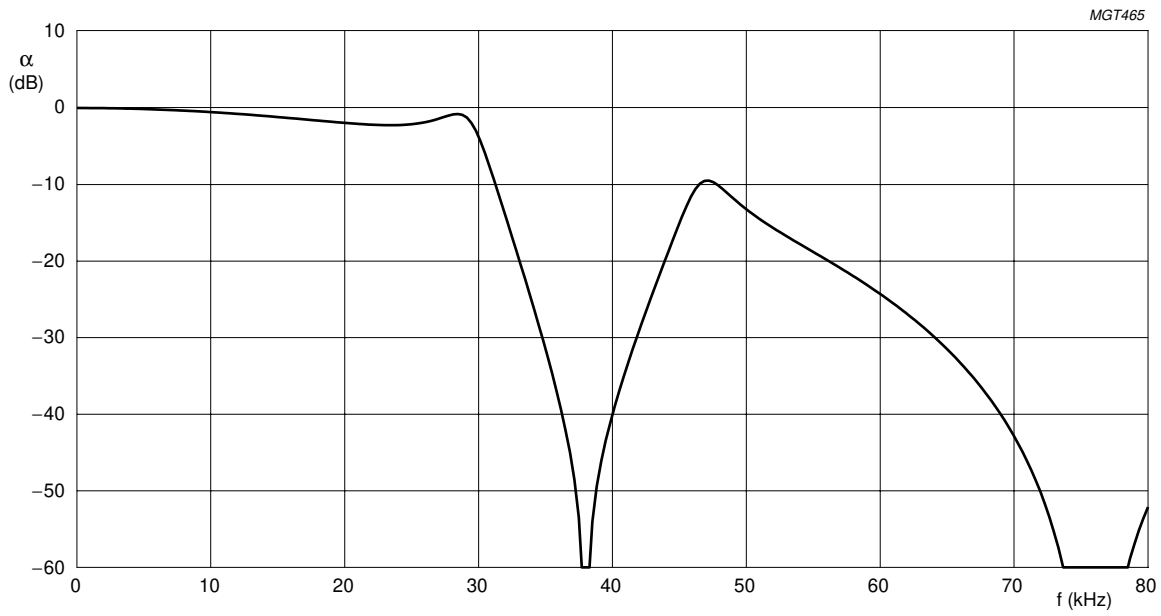


Fig.9 Frequency response level-ADC and decimal filter.

8.4 Signal path from FM_MPX input to IAC and stereo decoder

The FM_MPX signal is after selection available at one of three ADCs (ADC1, 2 and 3). The multiplex FM signal is converted to the digital domain in ADC1, 2 and 3 through a bitstream ADC. Improved performance for FM stereo can be achieved by means of adapting the noise shaper curve of the ADC to a higher bandwidth.

The first decimation takes place in two down-sample filters. These decimation filters are switched by means of the I^2C-bus bit wide_narrow in the wide or narrow band position. In the event of FM reception it must be in the narrow position.

After selection of one of the ADCs, the FM_MPX path it is followed by the IAC and the FM stereo decoder. One of the two MPX filter outputs contains the multiplex signal with a frequency range of 0 to 60 kHz. The overall low-pass frequency response of the decimation filters is shown in Fig.10.

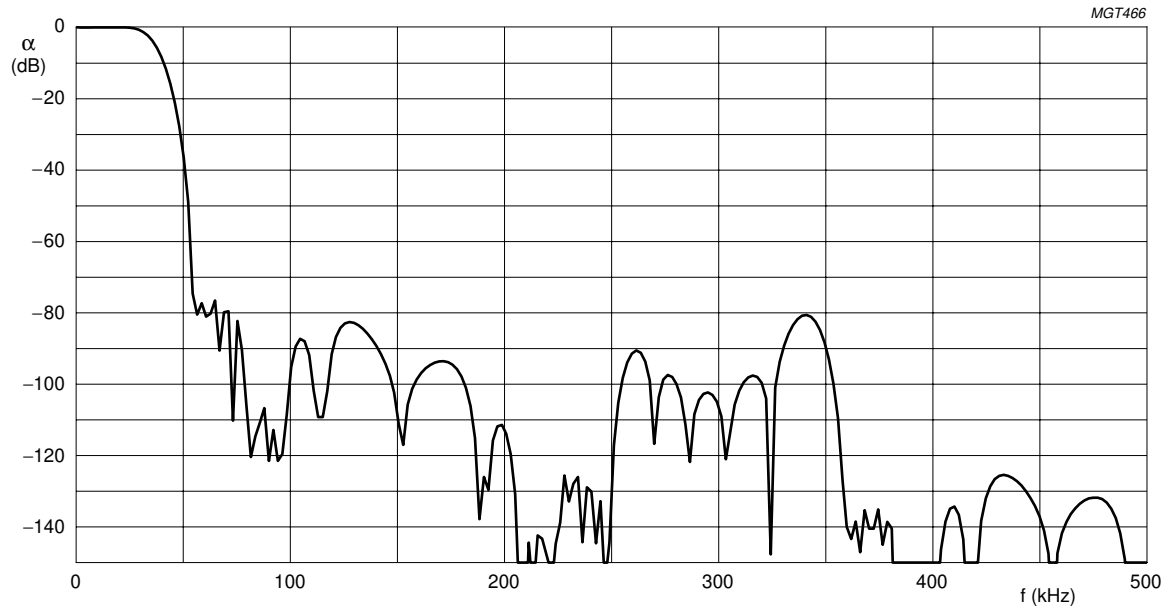


Fig.10 Overall frequency response of ADC1, ADC2 and decimation filters.

The outputs of the stereo decoder to the DSP1, which are all running on a sample frequency of 38 kHz are:

- Pilot presence indication: pilot-I. This 1-bit signal is LOW for a pilot frequency deviation <4 kHz and HIGH for a pilot frequency deviation >4 kHz and locked on a pilot tone.
- 'Left' and 'right' FM reception stereo signal: this is the 18-bit output of the stereo decoder after the matrix decoding.
- Noise level (see also Section 8.4.1): which is retrieved from the high-pass output of the MPX filter. The noise level is detected and filtered in the DSP1 and is used to optimize the FM weak signal processing.

Normally the FM_MPX input and the FM_RDS input have the same source. If the FM input contains a stereo radio channel, the pilot information is switched to the Digitally Controlled Sampling (DCS) clock generation and the DCS clock is locked to the 256 × 38 kHz of the pilot. In this case this locked frequency is also used for the RDS path ensuring the best possible performance.

Except from the above mentioned theoretical response also the non-flat frequency response of the ADC has to be compensated in the DSP1 program.

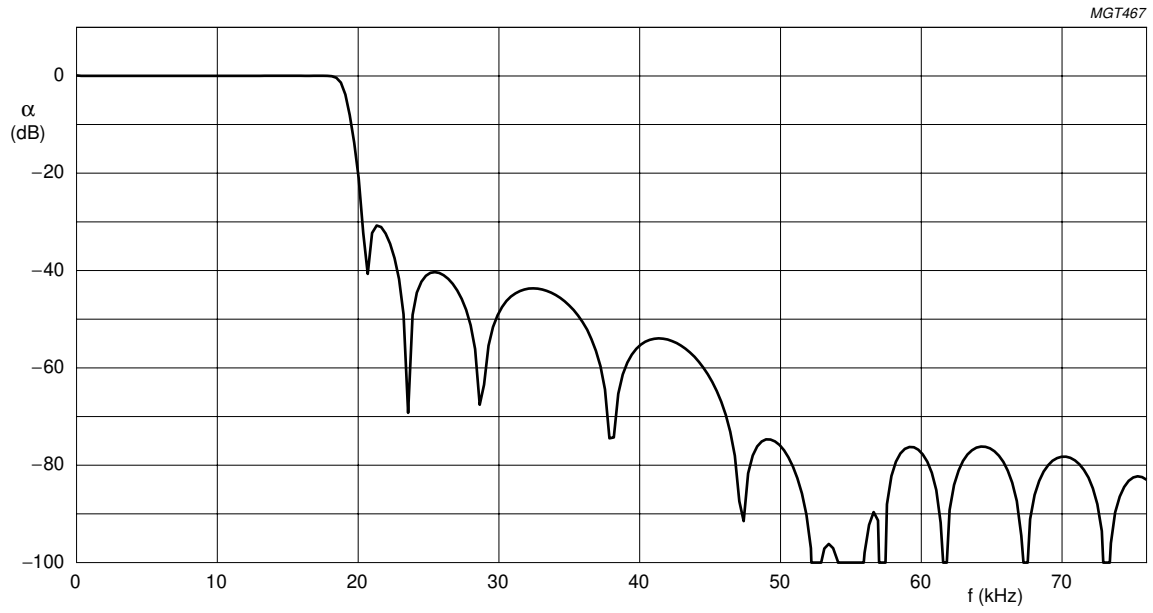
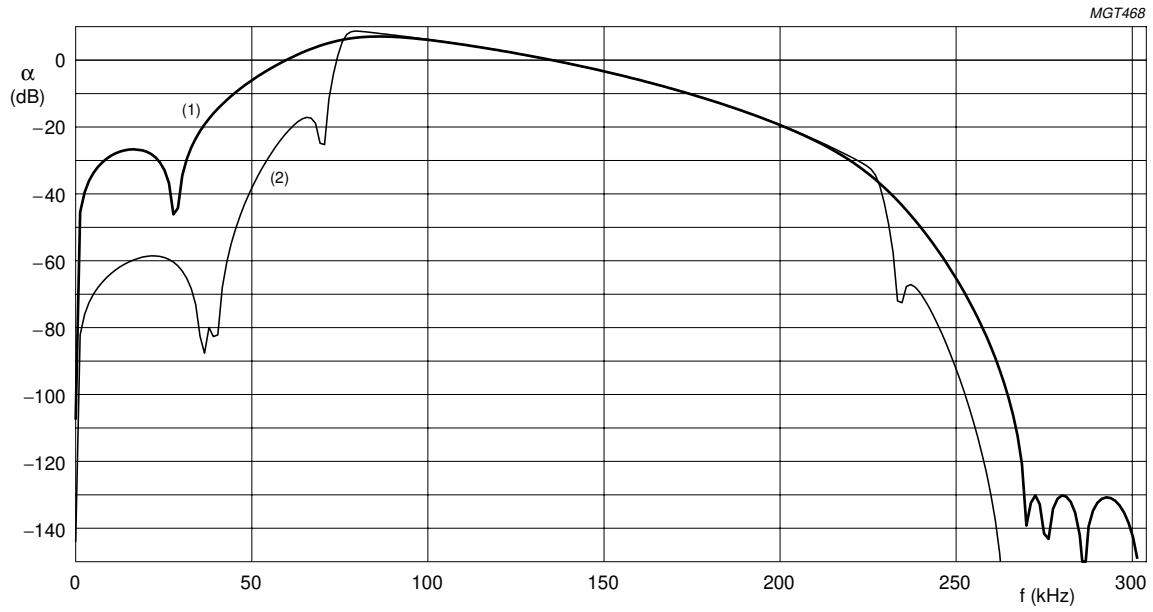


Fig.11 Transfer of MPX signal at the output of the stereo decoder.

8.4.1 NOISE LEVEL

The high-pass 1 (HP1 or narrow band noise level filter) output of the second MPX decimation filter in a band from 60 kHz to 120 kHz is detected with an envelope detector and decimated to a frequency of 38 kHz. The response time of the detector is 100 μs. Another option is the high-pass 2 (HP2 or wide band noise level filter). This output of the first MPX decimation filter is in a band from 60 to 240 kHz. It has the same properties and is also decimated to the same 38 kHz. Which of the signals is used (HP1 or HP2) is determined by the I^2C-bus bit sel_nsdec.

The resulting noise information is rectified and has a word length of 10 bits. This means that the lowest and/or the highest possible level is not used. The noise level can be detected and filtered in the DSP1-core and be used to optimize the FM weak signal processing. The transfer curves of both filters before decimation are shown in Fig.12.



(1) Noise with wide band digital filter.
(2) Noise with small band digital filter.

Fig.12 Frequency response of noise level before decimation.

8.4.2 MONO OR STEREO SWITCHING

The DCS block uses a sample rate converter to derive from the XTAL clock, via a PLL, a 512 multiple of 19 kHz (9.728 MHz). In the event of mono reception the DCS circuit generates a preset frequency of n × 19 kHz ±2 Hz. In the event of stereo reception the frequency is exactly n × 19 kHz (DCS locked to N × pilot tone). The detection of the pilot and the stereo indication is done in the DSP program.

8.4.3 THE AUTOMATIC LOCK SYSTEM

The VCO of the DCS block will be at 19 kHz ±2 Hz exact based in the event of no-pilot FM_MPX reception or in the event of only RDS reception. In the event of stereo reception the phase error is zero for a pilot tone with a frequency of exactly 19 kHz.

8.5 DCS clock

In radio mode the stereo decoder, the ADC3 and RDS demodulator, the ADC1 or ADC2 and the level decimation filters have to run synchronously to the 19 kHz pilot. Therefore a clock signal with a controlled frequency of a multiple of 19 kHz (9.728 MHz = 512 × 19 kHz) is needed.

In the SAA7706H the patented method of non-equidistant digitally controlled sampling DCS clock has been implemented. By a special dividing mechanism a frequency of 9.728 MHz from the PLL2 clock frequency of >40 MHz is generated. The dividing can be changed by means of I²C-bus bits to cope with the different input frequencies of the DCS block.

The DCS system is controlled by up or down information from the stereo decoder. In the event of mono transmissions or 44.1 kHz ADC1 or ADC2 usage the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free running on a multiple frequency of 19 kHz ±2 Hz if the correct clock setting is applied. In

tape/cd of either 38 or 44.1 kHz and AM mode the DCS clock always has to be put in preset mode with a bit in the I²C-bus memory map definitions.

8.6 The Interference Absorption Circuit (IAC)

8.6.1 General description

The IAC detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from ignition interference pulse detectors. The input signal of a second IAC detection circuit is the FM level signal (the output of the level-ADC). This detector performs optimally in lower antenna voltage circumstances. It is therefore complementary to the first detector.

The input signal of a first IAC detection circuit is the output signal of one of the down-sample paths coming from ADC1 or ADC2. This interference detector analyses the high-frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is based on probability calculations. This detector performs optimally in higher antenna voltage circumstances. On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

The characteristics of both IAC detectors can be adapted to the properties of different FM front-ends by means of the predefined coefficients in the IAC control registers. The values can be changed via the I²C-bus. Both IAC detectors can be switched on or off independently of each other. Both IAC detectors can mute the MPX signal independently of each other.

A third IAC function is the dynamic IAC circuit. This block is intended to switch off the IAC completely the moment the MPX signal has a too high frequency deviation which in the event of small IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

8.7 The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7.1 Interpolation filter

The digital filter interpolates from 1 to $64f_s$ by means of a cascade of a recursive filter and an FIR filter.

Table 2 Digital interpolation filter characteristics

ITEM	CONDITIONS	VALUE (dB)
Pass band ripple	$0 - 0.45f_s$	±0.03
Stop band	$>0.55f_s$	−50
Dynamic range	$0 - 0.45f_s$	116.5
Gain	DC	−3.5

8.7.2 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a filter stream digital-to-analog converter.

8.7.3 FUNCTION OF PIN POM

With pin POM it is possible to switch off the reference current of the DAC. The capacitor on pin POM determines the time after which this current has a soft switch-on. So at power-on the current audio signal outputs are always muted. The loading of the external capacitor is done in two stages via two different current sources. The loading starts at a current level that is lower than the current loading after the voltage on pin POM has past a particular level. This results in an almost dB-linear behaviour. This must prevent 'plop' effects during power on or off.

8.7.4 POWER-OFF PLOP SUPPRESSION

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC and the rest of the chip can be fed from a separate power supply of 3.3 V. A capacitor connected to this power supply enables to provide power to the analog part at the moment the digital voltage is switching off fast. In this event the output voltage will decrease gradually allowing the power amplifier some extra time to switch off without audible plops.

8.7.5 PIN VREFDA FOR INTERNAL REFERENCE

With two internal resistors half the supply voltage V_{DDA2} is obtained and used as an internal reference. This reference voltage is used as DC voltage for the output operational amplifiers and as reference for the DAC.

In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground, preferably close to the analog pin V_{SSA2}.

8.7.6 SUPPLY OF THE FILTER STREAM DAC

The entire analog circuitry of the DACs and the operational amplifiers are supplied by 2 supply pins: V_{DDA2} and V_{SSA2}. V_{DDA2} must have sufficient decoupling to prevent total harmonic distortion degradation and to ensure a good power supply rejection ratio. The digital part of the DAC is fully supplied from the chip core supply.

8.8 Clock circuit and oscillator

The chip has an on-chip crystal clock oscillator. The block diagram of this Pierce oscillator is shown in Fig.13. The active element needed to compensate for the loss resistance of the crystal is the block G_m. This block is placed between the external pins OSC_IN and OSC_OUT. The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the higher harmonics are as low as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from sine wave to the clock signal.

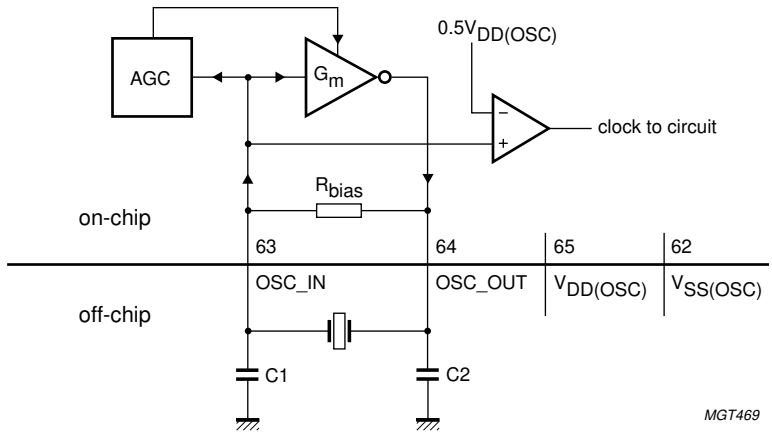


Fig.13 Block diagram oscillator circuit.

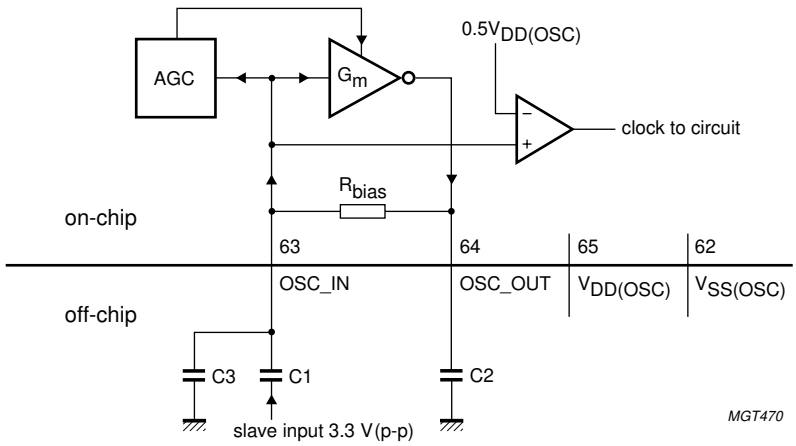


Fig.14 Block diagram of the oscillator in slave mode.

8.8.1 SUPPLY OF THE CRYSTAL OSCILLATOR

The power supply connections of the oscillator are separated from the other supply lines. This is done to minimize the feedback from the ground bounce of the chip to the oscillator circuit. Pin $V_{SS(OSC)}$ is used as ground supply and pin $V_{DD(OSC)}$ as positive supply. A series resistor plus capacitance is required for proper operating on pin $V_{DD(OSC)}$, see Figs 25 and 26. See also important remark in Section 8.10.

8.9 The phase-locked loop circuit to generate the DSPs and other clocks

There are several reasons why a PLL circuit is used to generate the clock for the DSPs:

- The PLL makes it possible to switch in the rare cases that tuning on a multiple of the DSP clock frequency occurs to a slightly higher frequency for the clock of the DSP. In this way an undisturbed reception with respect to the DSP clock frequency is possible.
- Crystals for the crystal oscillator in the range of twice the required DSP clock frequency, so approximately 100 MHz, are always third overtone crystals and must also be manufactured on customer demand. This makes these crystals expensive. The PLL1 enables the use of a crystal running in the fundamental mode and also a general available crystal can be chosen. For this circuit a 256×44.1 kHz = 11.2896 MHz crystal is chosen. This type of crystal is widely used.
- Although a multiple of the frequency of the used crystal of 11.2896 MHz falls within the FM reception band, this will not disturb the reception because the relatively low frequency crystal is driven in a controlled way and the sine wave of the crystal has in the FM reception band only very minor harmonics.

8.10 Supply of the digital part (V_{DDD3V1} to V_{DDD3V4})

The supply voltage on pins V_{DDD3V1} to V_{DDD3V4} must be for at least 10 ms earlier active than the supply voltage applied to pin $V_{DD(OSC)}$.

8.11 CL_GEN, audio clock recovery block

When an external I^2S-bus or SPDIF source is connected, the FSDAC circuitry needs an $256f_s$ related clock. This clock is recovered from either the incoming WS of the digital serial input or the WS derived from the SPDIF1/SPDIF2 input. There is also a possibility to provide the chip with an external clock, in that case it must be a $256f_s$ clock with a fixed phase relation to the source.

8.12 External control pins

8.12.1 DSP1

For external control two input pins have been implemented. The status of these pins can be changed by applying a logic level. The status is saved in the DSP1 status register. The function of each pin depends on the DSP1 program.

To control external devices two output pins are implemented. The status of these pins is controlled by the DSP program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.12.2 DSP2

For external control four configurable I/O pins have been implemented. Via the I²C-bus these four pins can be independently configured as input or output. The status of these pins can be changed by applying a logic level (input mode). The status is saved in the DSP2 status register. The function of each pin depends on the I²C-bus setting and DSP2 program.

Function of these ‘control pins’ can be found in a separate manual and is rom_code dependent.

8.13 I²C-bus control (pins SCL and SDA)

General information about the I²C-bus can be found in *“The I²C-bus and how to use it”*. This document can be ordered using the code 9398 393 40011. For the external control of the SAA7706H device a fast I²C-bus is implemented. This is a 400 kHz bus which is downward-compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)
- Instructions controlling the data flow; such as source selection, IAC control and clock speed.

The detailed description of the I²C-bus and the description of the different bits in the memory map is given in Chapter 9.

8.14 Digital serial inputs/outputs and SPDIF inputs

8.14.1 General description digital serial audio inputs/outputs

For communication with external digital sources a digital serial bus is implemented. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7706H acts as a slave, so the external source is master and supplies the clock.

The digital serial input is capable of handling multiple input formats. The input is capable of handling Philips I²S-bus and LSB-justified formats of 16, 18, 20 and 24 bits word sizes. The sampling frequency can be either 44.1 or 48 kHz. See Fig.15 for the general waveform formats of all possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is smaller than 24 bits (internal resolution of DSP2), the LSB bits will get internally a zero value; when the applied word length exceeds 24 bits then the LSBs are skipped.

It should be noted that:

- Two digital sources can not be used at the same time
- Maximum number of bit clocks per word select (WS) is limited to 64
- The word select (WS) must have a duty cycle of 50%.

8.14.2 General description SPDIF inputs (SPDIF1 and SPDIF2)

For communication with external digital sources also an SPDIF input can be used. The two SPDIF input pins can be connected via an analog multiplexer to the SPDIF receiver. It is a receiver without an analog PLL that samples the incoming SPDIF with a high frequency. In this way the data is recovered synchronously on the applied system clock.

From the SPDIF signal a three wire serial bus (e.g. I²S-bus) is made, consisting of a word select, data and bit clock line. The sample frequency f_s depends solely on the SPDIF signal input accuracy and both 44.1 and 48 kHz are supported.

This chip does not handle the user data bits, channel status bits and validity bits of the SPDIF stream, but only the audio is given at its outputs. Some rom_codes do take care of the pre-emphasis bit of the SPDIF stream.

The bits in the audio space are always decoded regardless of any status bits e.g. ‘copy protected’, ‘professional mode’ or ‘data mode’. The DAC is not muted in the event of a non-linear PCM audio, however the bit is observable via the I²C-bus. A few other channel status bits are available. There are 5 control signals available from the SPDIF input stage. These are connected to flags of DSP2. For more details see separate manual.

These 5 control signals are:

- Signals to indicate the sample frequency of the SPDIF signal: 44.1 and 48 kHz (32 kHz is not supported)
- A lock signal indicating if the SPDIF input is in lock
- The pre-emphasis bit of the SPDIF audio stream
- The pcm_audio/non-pcm_audio bit indicating if an audio or data stream is detected. The FSDAC output will not be muted in the event of a non-audio PCM stream. This status bit can be read via the I²C-bus, the microcontroller can decide to mute the DAC (via pin POM).

The design fulfils the digital audio interface specification *“IEC 60958-1 Ed2, part 1, general part IEC 60958-3 Ed2, part 3, consumer applications”*.

It should be noted that:

- The SPDIF input may only be used in the ‘consumer mode’ specified in the digital audio interface specification
- Only one of the two SPDIF sources can be used (selected) at the same time
- The FSDAC will not (automatically) be muted in the event of a non-audio stream
- Two digital sources can not be used at the same time
- Supported sample frequencies are 44.1 and 48 kHz.