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DATA SHEET

SAA7826

CD audio decoder, digital servo and filterless DAC with integrated pre-amp and laser control

Product specification Supersedes data of 2003 Aug 04 2003 Oct 01

Philips Semiconductors

PHILIPS

CONTENTS

CD audio decoder, digital servo and filterless DAC with integrated pre-amp and laser control

SAA7826

1 FEATURES

- Decoder and servo parts are based upon the SAA732X design (the original features are maintained)
- Software compatibility is maintained with the SAA732X by using a similar register structure (new features are controlled from new shadow registers)
- 1×, 2× and 4× speed
- LF (servo) signals converted to digital representations by 6 oversampling bitstream ADCs
- HF part summed from signals D1 to D4 and converted to a digital signal by a data slicer
- On-chip buffering and filtering of the diode signals from the mechanism for signal optimization
- Selectable DC offset cancellation of quiescent mechanism voltages and dark currents
- On-chip laser power control (up to 120 mA)
- Laser on/off control, including 'soft' start control (zero to nominal power in 1 ms)
- Monitor control and feedback circuit to maintain nominal output power throughout laser life
- Dynamic element matching DAC with minimum external components
- DAC performance of −80 dB Total Harmonic Distortion + Noise (THD + N) and 90 dB Signal-to-Noise Ratio (S/N) A-weighted
- Separate left and right channel digital silence detection available on the KILL pins
- Digital silence detection on internal data and loopback (external) data
- 5 versatile pins, 2 inputs and 3 outputs

ReWritable CD COMPATIBLE

I²C BUS

- Integrated CD text decoder with separate microcontroller interface
- Dedicated 4 MHz or 12 MHz clock output for microcontroller (configurable)
- Configured for N-sub monitor diode
- On-chip clock multiplier allows the use of an 8.4672 MHz crystal or ceramic resonator
- The M1 version has an EBU mute function which allows independent muting of data being transmitted over the EBU interface whilst maintaining the SPDIF frame structure.

2 GENERAL DESCRIPTION

This document covers versions M0 and M1 of the CD audio decoder IC.

The SAA7826 is a CD audio decoder IC which combines the function of the SAA732X IC with the pre-amplifier and laser control functions previously found in the TZA102X IC. The design is intended to reduce the external component count and hence the Bill Of Material (BOM).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7826HL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		1.65	1.8	1.95	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
I_{DDD}	digital supply current	n = 1 mode	–	38	–	mA
		n = 2 mode	–	39	–	mA
		n = 4 mode	–	40	–	mA
f_{xtal}	crystal frequency		–	8.4672	–	MHz
T_{amb}	ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–55	–	+125	°C
S/N_{DAC}	onboard DAC signal-to-noise ratio		–	90	–	dB

5 BLOCK DIAGRAM

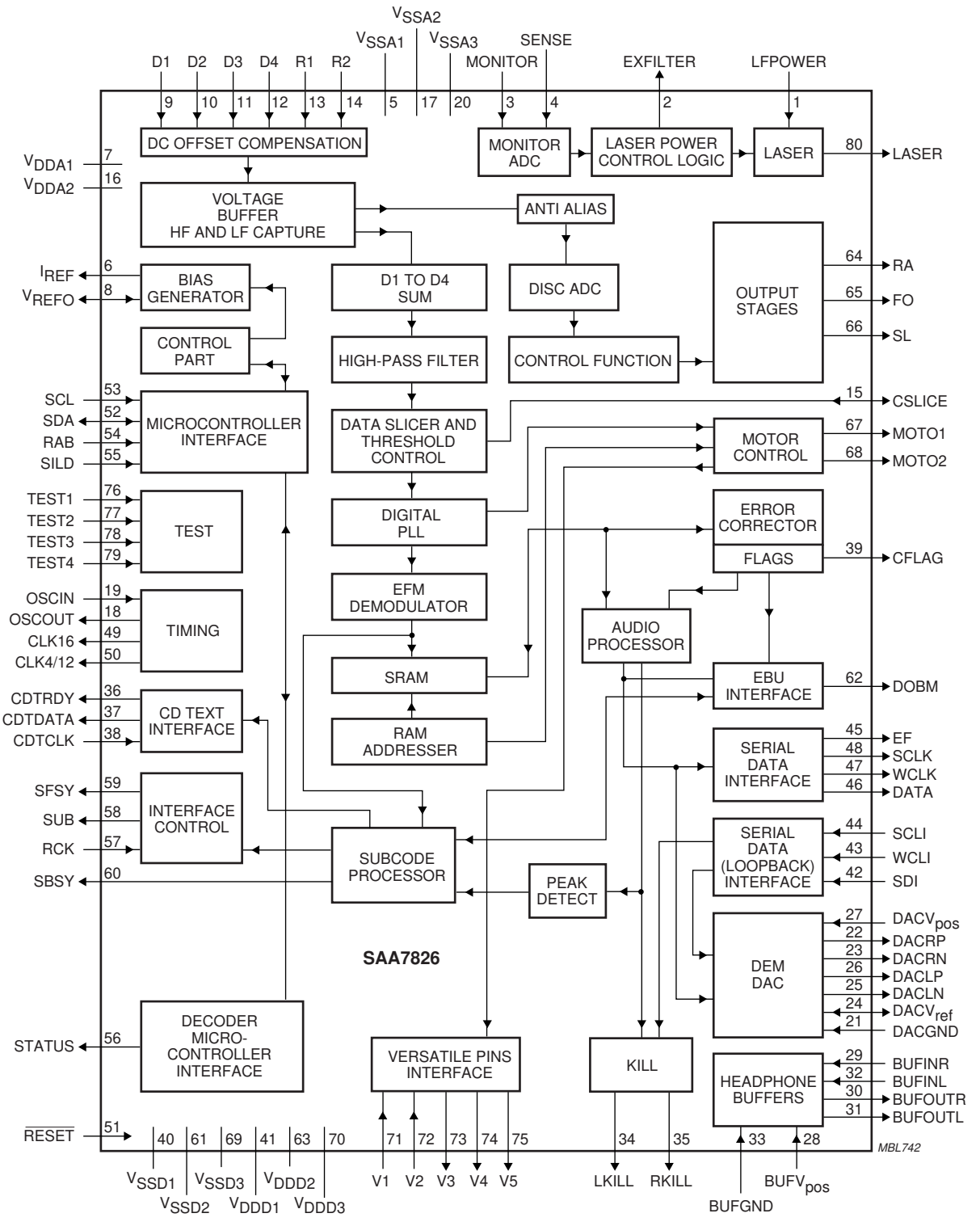


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
LFPOWER	1	I	laser power supply
EXFILTER	2	O	10 nF capacitor for laser start-up control
MONITOR	3	I	laser monitor diode
SENSE	4	I	OPU ground reference point for MONITOR measurement
V_{SSA1}	5	SUP	analog ground 1
I_{REF}	6	O	reference current output (24 kΩ resistor connected to analog ground)
V_{DDA1}	7	SUP	analog supply voltage 1
V_{REFO}	8	I/O	servo reference voltage
D1	9	I	diode voltage/current input (central diode signal input)
D2	10	I	diode voltage/current input (central diode signal input)
D3	11	I	diode voltage/current input (central diode signal input)
D4	12	I	diode voltage/current input (central diode signal input)
R1	13	I	diode voltage/current input (satellite diode signal input)
R2	14	I	diode voltage/current input (satellite diode signal input)
CSLICE	15	I/O	10 nF capacitor for adaptive HF data slicer
V_{DDA2}	16	SUP	analog supply voltage 2
V_{SSA2}	17	SUP	analog ground 2
OSCOUT	18	O	crystal/resonator output
OSCIN	19	I	crystal/resonator input
V_{SSA3}	20	SUP	analog ground 3
DACGND	21	I	audio DAC ground
DACRP	22	O	audio DAC right channel differential positive output
DACRN	23	O	audio DAC right channel differential negative output
$DACV_{ref}$	24	I/O	audio DAC decoupling point (10 μF or 100 nF to ground)
DACLN	25	O	audio DAC left channel differential negative output
DACLP	26	O	audio DAC left channel differential positive output
$DACV_{pos}$	27	I	audio DAC positive supply voltage
$BUFV_{pos}$	28	I	audio buffer positive supply voltage
BUFINR	29	I	audio buffer right input
BUFOUTR	30	O	audio buffer right output
BUFOUTL	31	O	audio buffer left output
BUFINL	32	I	audio buffer left input
BUFGND	33	I	audio buffer ground
LKILL	34	O	KILL output for left channel (configurable as open-drain)
RKILL	35	O	KILL output for right channel (configurable as open-drain)
CDTRDY	36	O	CD text output to microcontroller ready flag
CDTDATA	37	O	CD text output data to microcontroller
CDTCLK	38	I	CD text microcontroller clock input
CFLAG	39	O	correction flag output (open-drain)
V_{SSD1}	40	SUP	digital ground 1

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD1}	41	SUP	digital supply voltage 1
SDI	42	I	serial data input (loopback)
WCLI	43	I	word clock input (loopback)
SCLI	44	I	serial bit clock input (loopback)
EF	45	O	C2 error flag output
DATA	46	O	serial data output
WCLK	47	O	word clock output
SCLK	48	O	serial clock output
CLK16	49	O	16 MHz clock output
CLK4/12	50	O	configurable 4 MHz or 12 MHz clock output
$\overline{RESET}$	51	I	power-on reset input (active LOW)
SDA	52	I/O	microcontroller interface data input/output (open-drain)
SCL	53	I	microcontroller interface clock input
RAB	54	I	microcontroller interface R/W and load control input (4-wire)
SILD	55	I	microcontroller interface R/W and load control input (4-wire)
STATUS	56	O	servo interrupt request line/decoder status register/DC offset value readback output
RCK	57	I	subcode clock input
SUB	58	O	P to W subcode output
SFSY	59	O	subcode frame sync output
SBSY	60	O	subcode block sync output
V_{SSD2}	61	SUP	digital ground 2
DOBM	62	O	bi-phase mark output (externally buffered)
V_{DDD2}	63	SUP	digital supply voltage 2
RA	64	O	radial actuator output
FO	65	O	focus actuator output
SL	66	O	sledge actuator output
MOTO1	67	O	motor output 1 output
MOTO2	68	O	motor output 2 output
V_{SSD3}	69	SUP	digital ground 3
V_{DDD3}	70	SUP	digital supply voltage 3
V1	71	I	versatile pin 1 input
V2	72	I	versatile pin 2 input
V3	73	O	versatile pin 3 output
V4	74	O	versatile pin 4 output
V5	75	O	versatile pin 5 output
TEST1	76	I	test pin 1 input
TEST2	77	I	test pin 2 input
TEST3	78	I	test pin 3 input
TEST4	79	I	test pin 4 input
LASER	80	O	laser drive output

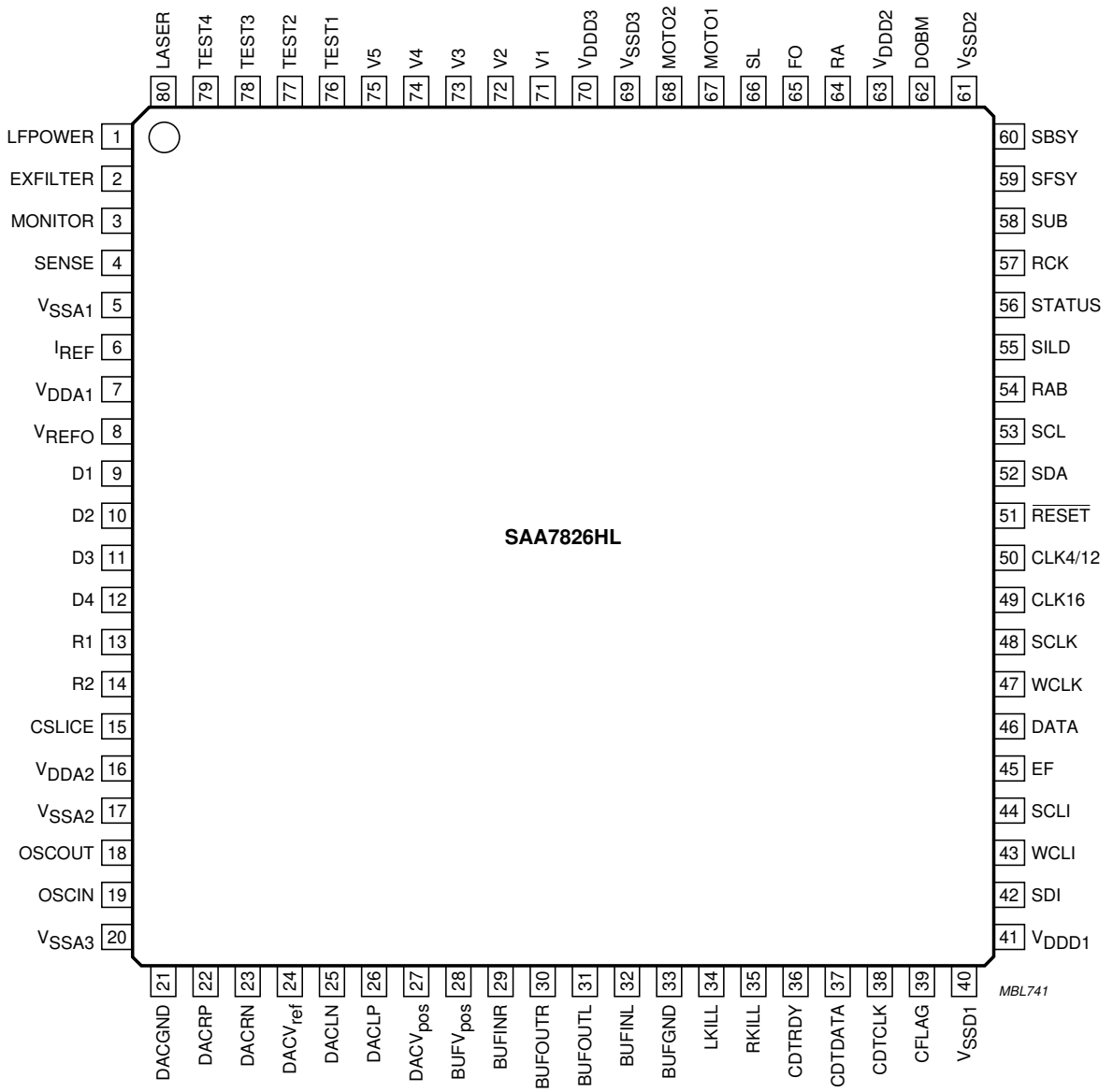


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Data acquisition and HF data path

The SAA7826 removes the need for an external diode signal pre-amplifier.

A simplified diagram of the HF data path is illustrated in Fig.3. The high-pass filter, equalizing filter, HF gain and adaptive slicer are all register programmable, thus enabling the SAA7826 to be optimized for the intended application.

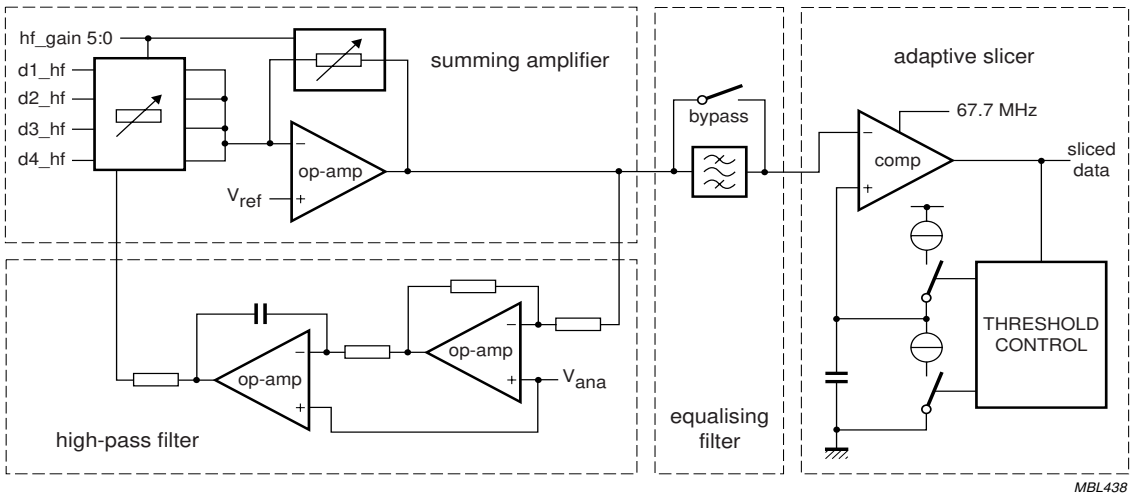


Fig.3 Simplified block diagram of the HF data path and adaptive slicer.

7.2 Decoder part

7.2.1 Principle operating modes of the decoder

The decoding part supports a full audio specification and can operate at single-speed (n = 1), double-speed (n = 2) and quad-speed (n = 4). The factor 'n' is called the overspeed factor. A simplified data flow through the decoder part is illustrated in Fig.7 for the M0 version and Fig.8 for the M1 version.

7.2.2 Decoder speed and crystal frequency

The SAA7826 is a 1×, 2× and 4× (three-speed) decoding device, with an internal Phase-Locked Loop (PLL) clock multiplier. Table 1 gives the playback speeds that are achievable in conjunction with crystal frequency, the mechanism and internal clock settings (selectable via decoder register B).

7.2.3 Lock-to-disc mode

For electronic shock absorption applications, the SAA7826 can be put into lock-to-disc mode. This allows Constant Angular Velocity (CAV) disc playback with varying input data rates from the inside to the outside of the disc.

In the lock-to-disc mode, the FIFO is blocked and the decoder will adjust its output data rate to the disc speed. Hence, the frequency of the I^2S-bus (WCLK and SCLK) clocks are dependent on the disc speed. In the lock-to-disc mode there is a limit on the maximum variation in disc speed that the SAA7826 will follow. Disc speeds must always be within 25% to 100% range of their nominal value. The lock-to-disc mode is enabled or disabled by decoder register E.

7.2.4 STANDBY MODES

The SAA7826 can be placed in two standby modes, selected by decoder register B (it should be noted that the device core is still active):

- Standby 1: CD STOP mode; most I/O functions are switched off
- Standby 2: CD PAUSE mode; audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active; this is also called a 'Hot Pause'.

In the standby modes the various pins will have the following values:

- MOTO1 and MOTO2: put in to high-impedance, PWM mode (Standby 1 and $\overline{\text{RESET}}$: operating in Standby 2); put in high-impedance, PDM mode (Standby 1 and $\overline{\text{RESET}}$: operating in Standby 2)
- Pins SCL and SDA: no interaction; normal operation continues
- Pins SCLK, WCLK, DATA, EF and DOBM: 3-state in both standby modes; normal operation continues after reset
- Pins OSCIN, OSCOUT, CLK16 and CLK4/12: no interaction; normal operation continues
- Pins V1 to V5 and CFLAG: no interaction; normal operation continues.

Table 1 Playback speeds

REGISTER B	REGISTER E	f_{xtal} = 8.4672 MHz
0XXX	0XXX	n = 1
1XXX	0XXX	n = 2; voltage mode only
0XXX	1XXX	n = 4; voltage mode only

7.3 Crystal oscillator

The crystal oscillator is a conventional 2-pin design which can also operate with ceramic resonators. The external components used around the crystal are illustrated in Fig.4 together with component values (C1 and C2) for a given crystal type in Table 2. The oscillator frequency that can be used with the SAA7826 is 8.4672 MHz.

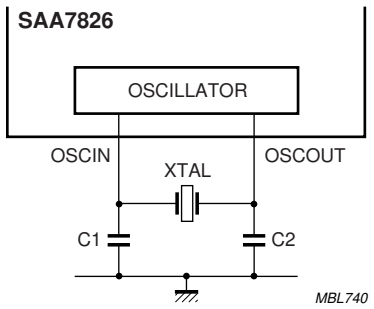


Fig.4 Crystal configuration.

Table 2 External capacitor selection based upon the crystal type

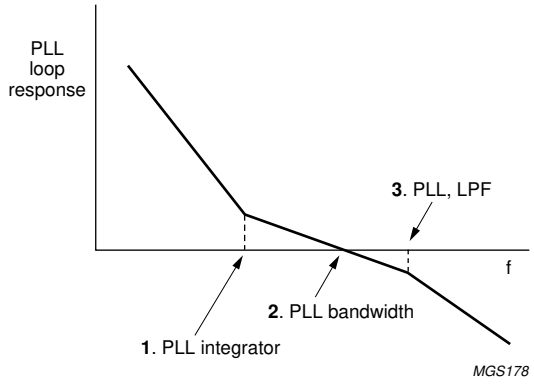
CRYSTAL LOAD CAPACITANCE (C_L)	MAXIMUM SERIES CRYSTAL RESISTANCE (R_S)	EXTERNAL LOAD CAPACITORS	
	8 MHz	C1	C2
10 pF	<300 Ω	8 pF	8 pF
20 pF	<300 Ω	27 pF	27 pF
30 pF	<300 Ω	47 pF	47 pF

7.4 Data slicer and bit clock regenerator

The SAA7826 has an integrated adaptive data slicer which is clocked at 67 MHz. The slice level is controlled by internal current sources which are switched onto and integrated by the external capacitor connected to the CSLICE pin. The currents are switched under the control of a Digital Phase-Locked loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required. The bit clock is not output. The PLL has two registers (8 and 9) for selecting bandwidth and equalization. The PLL loop response is illustrated in Fig.5.

For certain applications an off-track input is necessary. This is internally connected from the servo part (its polarity can be changed by the foc_parm1 parameter), but can be input via pin V1 if selected by register C. If this flag is HIGH, the SAA7826 assumes that its servo part is following the wrong track, and will flag all incoming HF data as incorrect.



Points 1, 2 and 3 are all programmable via decoder register 8.

Fig.5 Digital PLL loop response.

7.5 DC offset cancellation

Unwanted DC offsets can exist within the photo-diode signals and are defined as the DC present in the system when the laser diode is switched off. They arise from various sources of imperfection within the system such as leakage in the photo diodes and offsets in the Optical Pick-Up (OPU) circuitry. The SAA7826 is capable of measuring these offsets and minimizing them.

7.5.1 Offset cancellation

A number of registers are associated with the DC offset cancellation function; these registers are given in Table 3.

The measurement time of the DC offset is regulated by new shadow register C (bank 2). A longer time will yield more accurate results but will result in greater measurement durations.

New shadow register 3 (bank 3) is used to select which diode is to be measured.

7.5.2 Reading back the DC offset value

The microcontroller reads the DC offset measurements in order to calculate the correct cancellation value [for writing back to new shadow register 7 (bank 3)].

This is achieved by using the STATUS pin and setting decoder register 7 to XX10. Shadow register C (bank 3) can then be used to control the STATUS pin output; the register settings are given in Table 20.

Once the measurement time has been set and the diode selected, the STATUS pin should be set to read the DC offset ready flag [new shadow register C (bank 3) = X01X]. This signal toggles HIGH after the prescribed measurement time. Changing the diode selection results in the measurement timer being automatically reset.

The microcontroller can read back the measurement by setting the STATUS pin to output the DC offset value [new shadow register C (bank 3) = X10X].

The offset value is repeatedly streamed out through the STATUS pin and is UART compatible. It should be noted that the MSB is inverted and will require re-inverting after the offset value has been captured. Timing information for this signal is illustrated in Fig.6.

The final DC cancellation value (as calculated by the microcontroller) can then be written to new shadow register 7 (bank 3). This is a multiple write register containing the cancellation values for all six diodes.

Table 3 Registers relating to the DC offset cancellation

SHADEN BITS	SHADOW REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
10 (bank 2)	C DC offset measurement times	1100	XX00	settling time = 354 µs	reset
			XX01	settling time = 1 ms	–
			XX10	settling time = 2 ms	–
			XX11	settling time = 10 ms	–
11 (bank 3)	3 diode selection for DC offset measurement	0011	0000	select D1	reset
			0001	select D1	–
			0010	select D2	–
			0011	select D3	–
			0100	select D4	–
			0101	select R1	–
			0110	select R2	–
			0111	select D1	–
	C STATUS pin control	1100	X00X	STATUS pin outputs decoder status register information	reset
			X01X	STATUS pin outputs DC offset ready flag	–
			X10X	STATUS pin outputs DC offset value	–
	7 DC cancellation levels	0111	multi-write (9 × 4 bits)	DC cancellation values for diodes D1 to D4 and R1 and R2; see Table 20	–

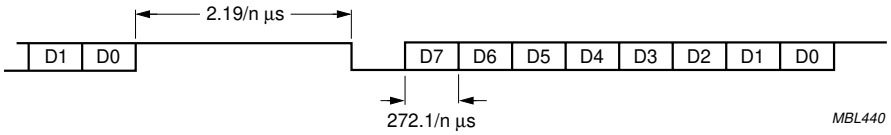


Fig.6 Serial data format for DC offset data.

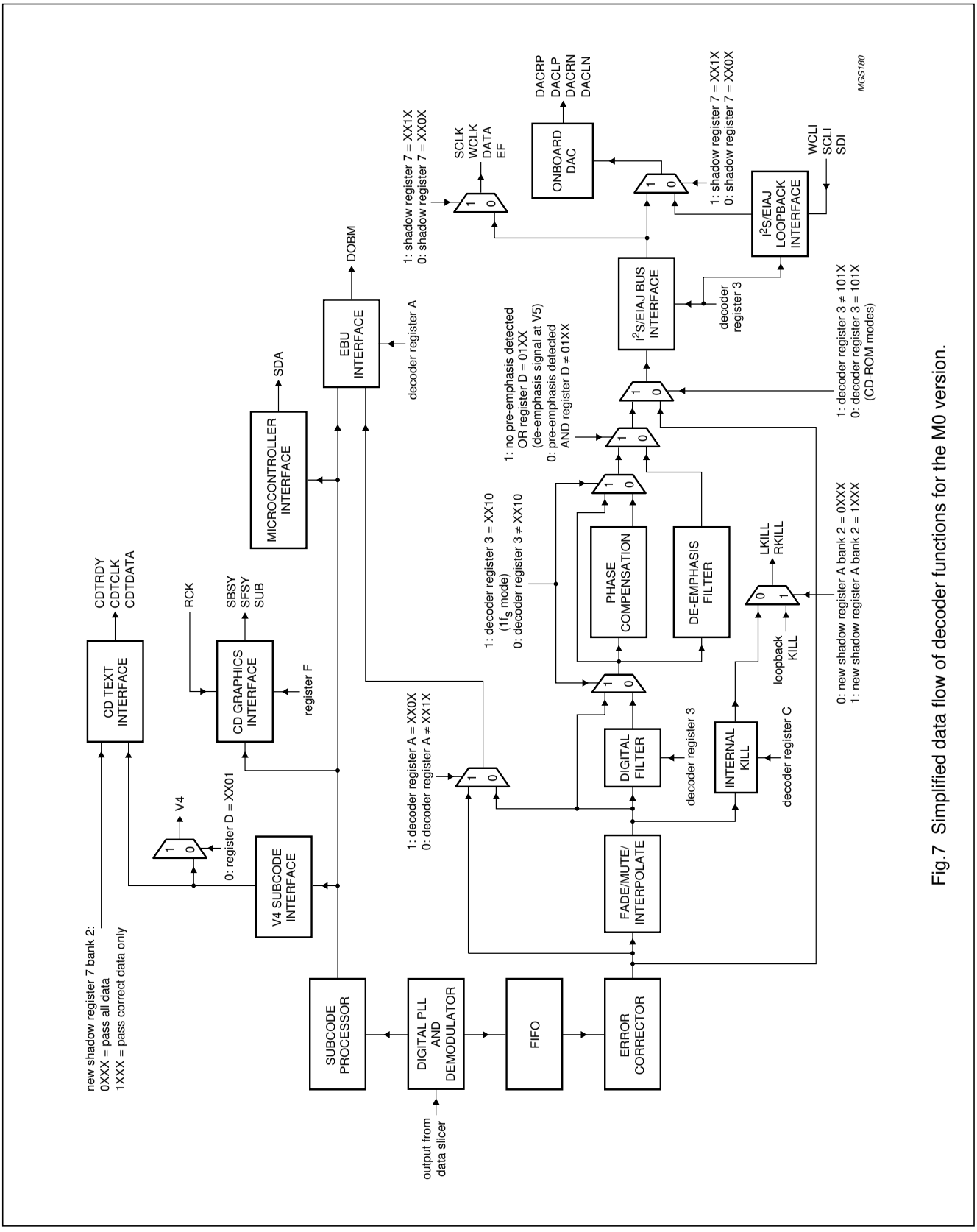


Fig.7 Simplified data flow of decoder functions for the M0 version.

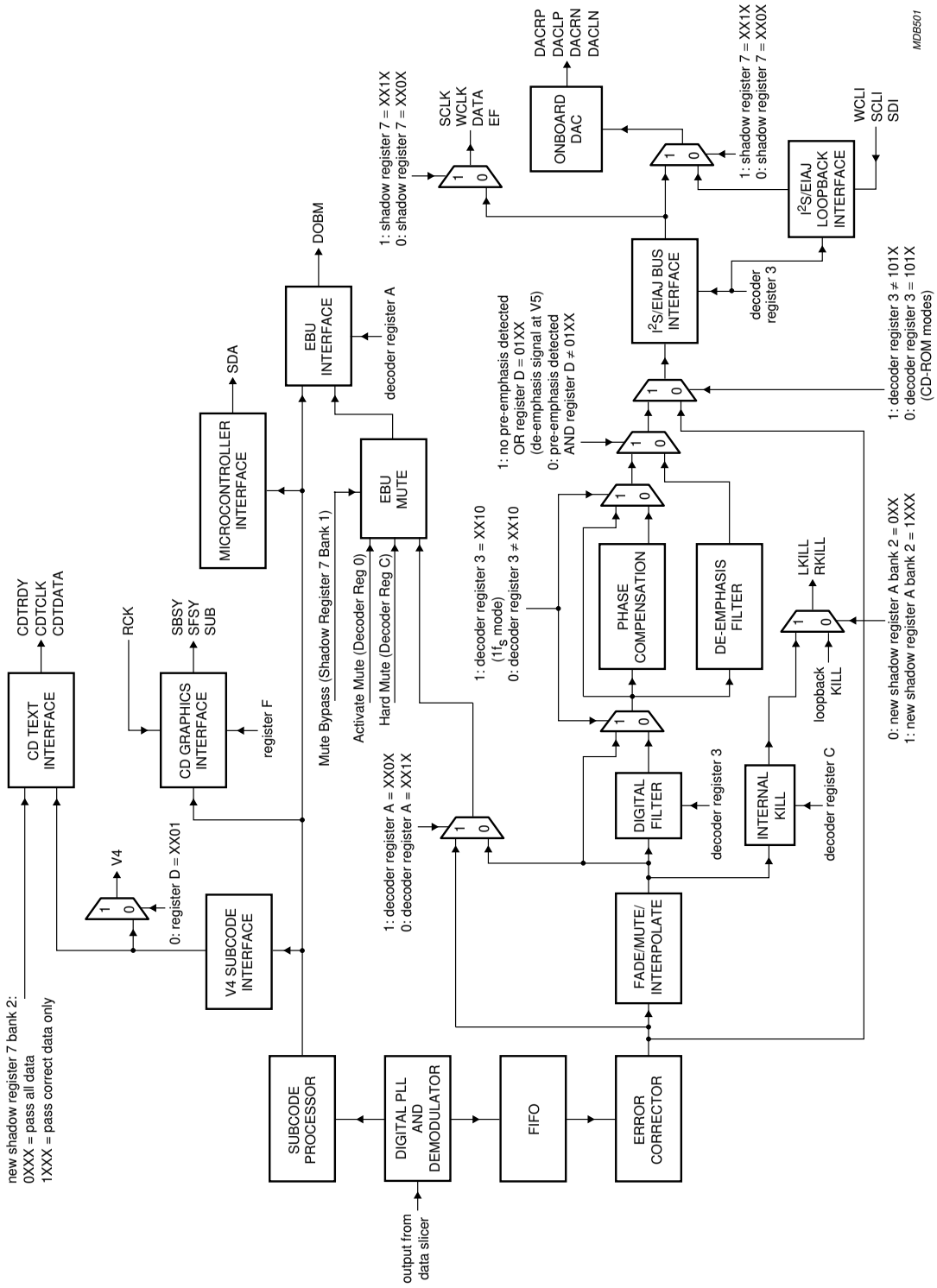


Fig.8 Simplified data flow of decoder functions for the M1 version.

7.6 Demodulator

7.6.1 Frame sync protection

A double timing system is used to protect the demodulator from erroneous sync patterns in the serial data. The master counter is only reset if:

- A sync coincidence is detected; sync pattern occurs 588 ±1 EFM clocks after the previous sync pattern
- A new sync pattern is detected within ±6 EFM clocks of its expected position.

The sync coincidence signal is also used to generate the PLL lock signal, which is active HIGH after 1 sync coincidence is found, and reset LOW if during 61 consecutive frames no sync coincidence is found. The PLL lock signal can be accessed via the SDA or STATUS pins selected by decoder registers 2, 7 and new shadow register C (bank 3).

Also incorporated in the demodulator is a Run Length 2 (RL2) correction circuit. Every symbol detected as RL2 is pushed back to RL3. To do this, the phase error of both edges of the RL2 symbol are compared and the correction is executed at the side with the highest error probability.

7.6.2 EFM demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols.

7.7 Subcode data processing

7.7.1 Q-channel processing

The 96-bit Q-channel word is accumulated in an internal buffer. The last 16 bits are used internally to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal goes LOW. SUBQREADY-I can be read via the SDA or STATUS pins, selected via decoder registers 2, 7 and new shadow register C (bank 3). Good Q-channel data may be read from pin SDA.

7.7.2 EIAJ 3 and 4-wire subcode (CD graphics) interface

Data from all the subcode channels (P-to-W) can be read via the subcode interface, which conforms to EIAJ CP-2401. The interface is enabled and configured as either a 3-wire or 4-wire interface via decoder register F.

The subcode interface output formats are illustrated in Fig.9, where the RCK signal is supplied by another device such as a CD graphics decoder.

7.7.3 V4 subcode interface

Data of subcode channels Q-to-W can be read via pin V4 if selected via decoder register D. The format is similar to RS232 and is illustrated in Fig.10. The subcode sync word is formed by a pause of (200/n) μs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q-to-W). The gap between bytes is variable between (11.3/n) μs and (90/n) μs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

7.7.4 CD text interface

R-to-W subcode data is captured and stored until a complete CD text PACK is formed. The least significant 16 bits of the PACK are used for a CRC.

The behaviour of the CD text interface is controlled by new shadow register 7 (bank 2). The interface can either flag all data (i.e. passed or failed CRC) or it can flag good data only.

The data ready flag is monitored via pin CDTRDY and is active LOW. The pulse width varies from 73/n μs, for the first three packs, to 317/n μs for the fourth pack.

When a PACK becomes available, the initial value of the CDTDATA pin indicates the CRC result (HIGH = passed; LOW = failed). The microcontroller can fetch the data by applying a clock signal (maximum frequency = 5 MHz) to pin CDTCLK and reading the subsequent bitstream on pin CDTDATA.

The 128 data bits are streamed out LSB first. A complete CD text PACK consists of 4 header bytes, 12 data bytes, and 2 CRC bytes, although the latter 2 bytes are dropped internally once the CRC calculation is complete. Refer to the *"Red Book"* for further details relating to the format of a CD text PACK

The timing diagram for the CD text interface is illustrated in Fig.11.

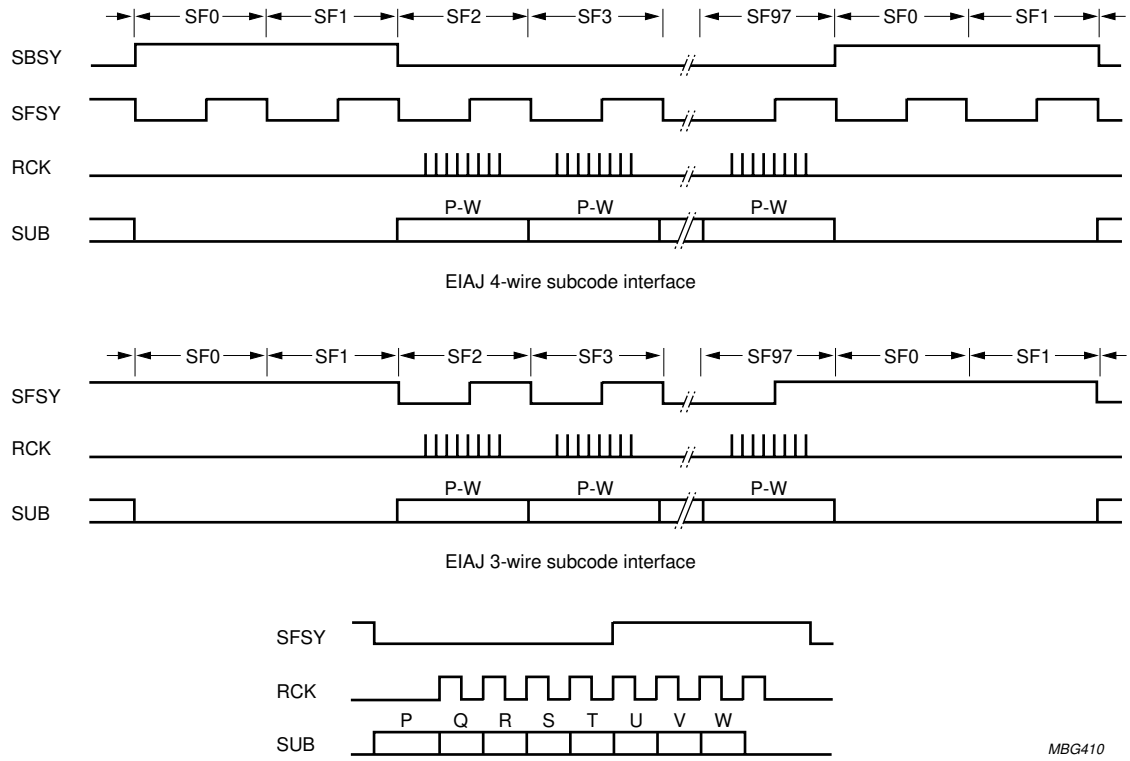
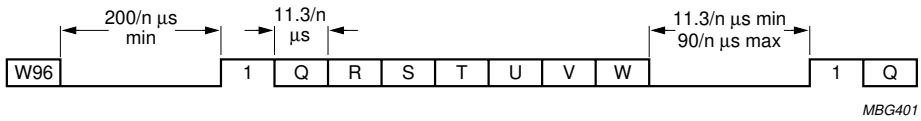
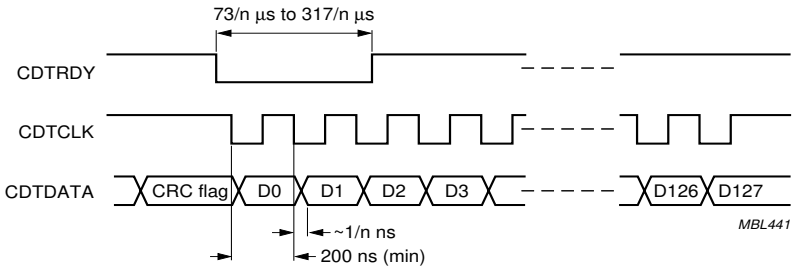


Fig.9 EIAJ subcode (CD graphics) interface format.



Where n = disc speed.

Fig.10 Subcode format and timing on pin V4.



Where n = disc speed.

Fig.11 CD text interface format and timing.

7.8 FIFO and error correction

The SAA7826 has a ±8 frame FIFO. The error corrector is a t = 2, e = 4 type, with error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. This error corrector can correct up to two errors on the C1 level and up to four errors on the C2 level.

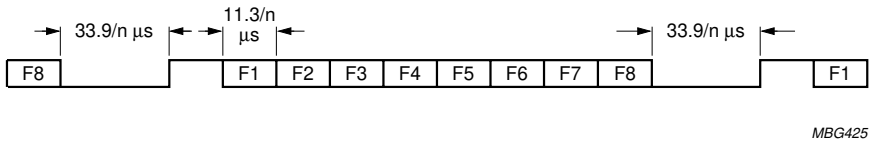
The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read after de-interleaving by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM). The EF output flags bytes in error in both audio and CD-ROM modes.

7.8.1 FLAGS OUTPUT (CFLG)

The flags output pin CFLG shows the status of the error corrector and interpolator and is updated every frame (7.35 × n kHz). In the SAA7826, 8 × 1-bit flags are present on the CFLG pin as illustrated in Fig.12. This signal shows the status of the error corrector and interpolator.

The first flag bit, F1, is the absolute time sync signal, the FIFO-passed subcode sync and relates the position of the subcode sync to the audio data (DAC output). This flag may also be used in a super FIFO or in the synchronization of different players. The output flags can be made available at bit 4 of the EBU data format (LSB of the 24-bit data word), if selected by decoder register A.



Where n = disc speed.

Fig.12 Flag output timing diagram.

Table 4 Output flags

F1	F2	F3	F4	F5	F6	F7	F8	DESCRIPTION
0	X	X	X	X	X	X	X	no absolute time sync
1	X	X	X	X	X	X	X	absolute time sync
X	0	0	X	X	X	X	X	C1 frame contained no errors
X	0	1	X	X	X	X	X	C1 frame contained 1 error
X	1	0	X	X	X	X	X	C1 frame contained 2 errors
X	1	1	X	X	X	X	X	C1 frame uncorrectable
X	X	X	0	0	X	X	0	C2 frame contained no errors
X	X	X	0	0	X	X	1	C2 frame contained 1 error
X	X	X	0	1	X	X	0	C2 frame contained 2 errors
X	X	X	0	1	X	X	1	C2 frame contained 3 errors
X	X	X	1	0	X	X	0	C2 frame contained 4 errors
X	X	X	1	1	X	X	1	C2 frame uncorrectable
X	X	X	X	X	0	0	X	no interpolations
X	X	X	X	X	0	1	X	at least one 1-sample interpolation
X	X	X	X	X	1	0	X	at least one hold and no interpolations
X	X	X	X	X	1	1	X	at least one hold and one 1-sample interpolation

7.9 Audio functions

7.9.1 De-emphasis and phase linearity

When pre-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section will control the phase of the digital oversampling filter to $\leq \pm 1°$ within the 0 to 16 kHz band. With de-emphasis the filter is not phase linear.

If the de-emphasis signal is set to be available at pin V5, selected via decoder register D, then the de-emphasis filter is bypassed.

7.9.2 Digital oversampling filter

For optimization of performance with an external DAC, the SAA7826 contains a 2 to 4 times oversampling IIR filter. The filter specification of the 4 times oversampling filter is given in Table 5.

The attenuation does not include the sample-and-hold at the external DAC output or the DAC post filter. When using the oversampling filter, the output level is scaled −0.5 dB down to avoid overflow on full-scale sine wave inputs (0 to 20 kHz).

Table 5 Filter specification

PASS BAND	STOP BAND	ATTENUATION
0 to 9 kHz	–	≤0.001 dB
19 to 20 kHz	–	≤0.03 dB
–	24 kHz	≥25 dB
–	24 to 27 kHz	≥38 dB
–	27 to 35 kHz	≥40 dB
–	35 to 64 kHz	≥50 dB
–	64 to 68 kHz	≥31 dB
–	68 kHz	≥35 dB
–	69 to 88 kHz	≥40 dB

7.9.3 Concealment

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators. If more than one consecutive non-correctable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample; see Fig.13.

In CD-ROM modes (i.e. the external DAC interface is selected to be in a CD-ROM format) concealment is not executed.

7.9.4 Mute, full-scale, attenuation and fade

A digital level controller is present on the SAA7826 which performs the functions of soft mute, full-scale, attenuation and fade; these are selected via decoder register 0:

- Mute: signal reduced to 0 in a maximum of 128 steps; 3/n ms
- Attenuation: signal scaled by −12 dB
- Full-scale: ramp signal back to 0 dB level; from mute it takes 3/n ms
- Fade: activates a 128 stage counter which allows the signal to be scaled up or down in 0.07 dB steps
  - 128 = full-scale
  - 120 = −0.5 dB (i.e. full-scale if oversampling filter is used)
  - 32 = −12 dB
  - 0 = mute.

7.9.5 Peak detector

The peak detector measures the highest audio level (absolute value) on positive peaks for left and right channels. The 8 most significant bits are output in the Q-channel data in place of the CRC bits. Bits 81 to 88 contain the left peak value (bit 88 = MSB) and bits 89 to 96 contain the right peak value (bit 96 = MSB). The values are reset after reading Q-channel data via pin SDA.

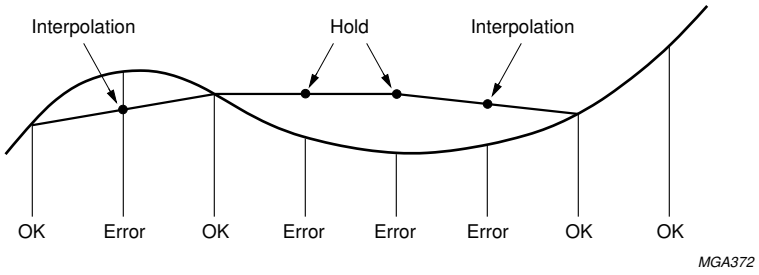


Fig.13 Concealment mechanism.

7.10 Audio DAC interface

7.10.1 INTERNAL DYNAMIC ELEMENT MATCHING DIGITAL-TO-ANALOG CONVERTER

The onboard audio DEM DAC operates at an oversampling rate of $96f_s$ and is designed for operation with an audio input at $1f_s$. The DAC is equipped with two pairs of stereo outputs for driving medium impedance line outputs and for directly driving low impedance headphones. A pair of analog inputs are provided to enable external audio sources to make use of the headphone output buffers.

Audio data from the decoder part of the SAA7826 can be routed as described in Sections 7.10.1.1 and 7.10.1.2.

Table 6 Shadow register

SHADEN BITS	SHADOW REGISTER	ADDRESS	DATA	FUNCTION	RESET
01 (bank 1)	7 control of onboard DAC	0111	0000	use external DAC or route audio data back into onboard DAC (loopback mode)	reset
			0010	route audio data directly into onboard DAC (non-loopback mode)	–

7.10.1.1 Use of internal DAC

Setting shadow register 7 to 0010 routes audio data from the decoder into the internal DAC. To enable the on-board DAC, the DAC interface format (set by register 3) must be set to 16-bit 1f_s mode, either I^2S-bus or EIAJ format. CD-ROM mode can also be used if interpolation is not required. The serial data output pins for interfacing with an external DAC (SCLK, WCLK, DATA and EF) are set to high-impedance.

7.10.1.2 Loopback external data into onboard DAC

The onboard DAC can also be set to accept serial data inputs from an external source, e.g. an Electronic Shock Absorption (ESA) IC. This is known as loopback mode and is enabled by setting shadow register 7 to 0000. This enables the serial data output pins (SCLK, WCLK, DATA and EF) so that data can be routed from the SAA7826 to an external ESA system (or external DAC).

The serial data from an external ESA IC can then also be input to the onboard DAC on the SAA7826 by utilising the serial data input interface (SCLI, SDI and WCLI).

In this mode, a wide range of data formats to the external ESA IC can be programmed as shown in Table 7.

However, the serial input on the SAA7826 always expects the input data from the ESA IC to be 16-bit 1fs and the same data format, either I2S-bus or EIAJ, as the serial output format (set by decoder register 3).

7.10.2 EXTERNAL DAC INTERFACE

Audio data from the SAA7826 can be sent to an external DAC, identical to the SAA732x series, in ‘loopback’ mode (i.e. shadow register 7 is set to 0000).

The SAA7826 is compatible with a wide range of external DACs. Eleven formats are supported which are given in Table 7. Figures 14 and 15 show the Philips I^2S-bus and the EIAJ data formats respectively. When the decoder is operated in lock-to-disc mode, the SCLK frequency depends on the disc speed factor ‘d’.

All formats are MSB first and 1f_s is 44.1 kHz. The polarity of the WCLK and the data can be inverted; selectable by decoder register 7. It should be noted that EF is only a defined output in CD-ROM and 1f_s modes.

When using an external DAC (or when using the onboard DAC in non-loopback mode), the serial data inputs to the onboard DAC (SCLI, SDI and WCLI) should be tied to ground.

Table 7 DAC interface formats

REGISTER 3	SAMPLE FREQUENCY	NUMBER OF BITS	SCLK (MHz)	FORMAT	INTERPOLATION
1010	f_s	16	2.1168 × n	CD-ROM (I^2S-bus)	no
1011	f_s	16	2.1168 × n	CD-ROM (EIAJ)	no
1110	f_s	16/18[1]	2.1168 × n	Philips I^2S-bus 16/18 bits[1]	yes
0010	f_s	16	2.1168 × n	EIAJ 16 bits	yes
0110	f_s	18	2.1168 × n	EIAJ 18 bits	yes
0000	$4f_s$	16	8.4672 × n	EIAJ 16 bits	yes
0100	$4f_s$	18	8.4672 × n	EIAJ 18 bits	yes
1100	$4f_s$	18	8.4672 × n	Philips I^2S-bus 18 bits	yes
0011	$2f_s$	16	4.2336 × n	EIAJ 16 bits	yes
0111	$2f_s$	18	4.2336 × n	EIAJ 18 bits	yes
1111	$2f_s$	18	4.2336 × n	Philips I^2S-bus 18 bits	yes

Note

1. In this mode the first 16 bits contain data, but if any of the fade, attenuate or de-emphasis filter functions are activated then the first 18 bits contain data.

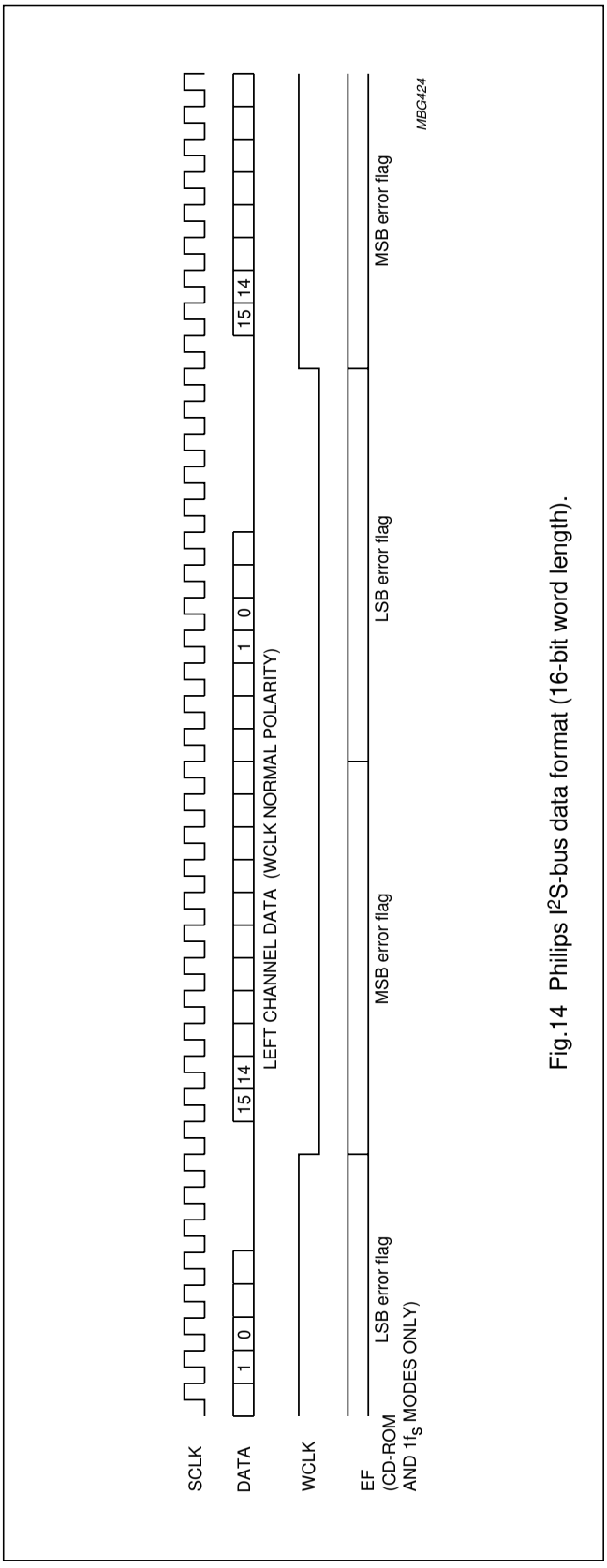


Fig.14 Philips I²S-bus data format (16-bit word length).

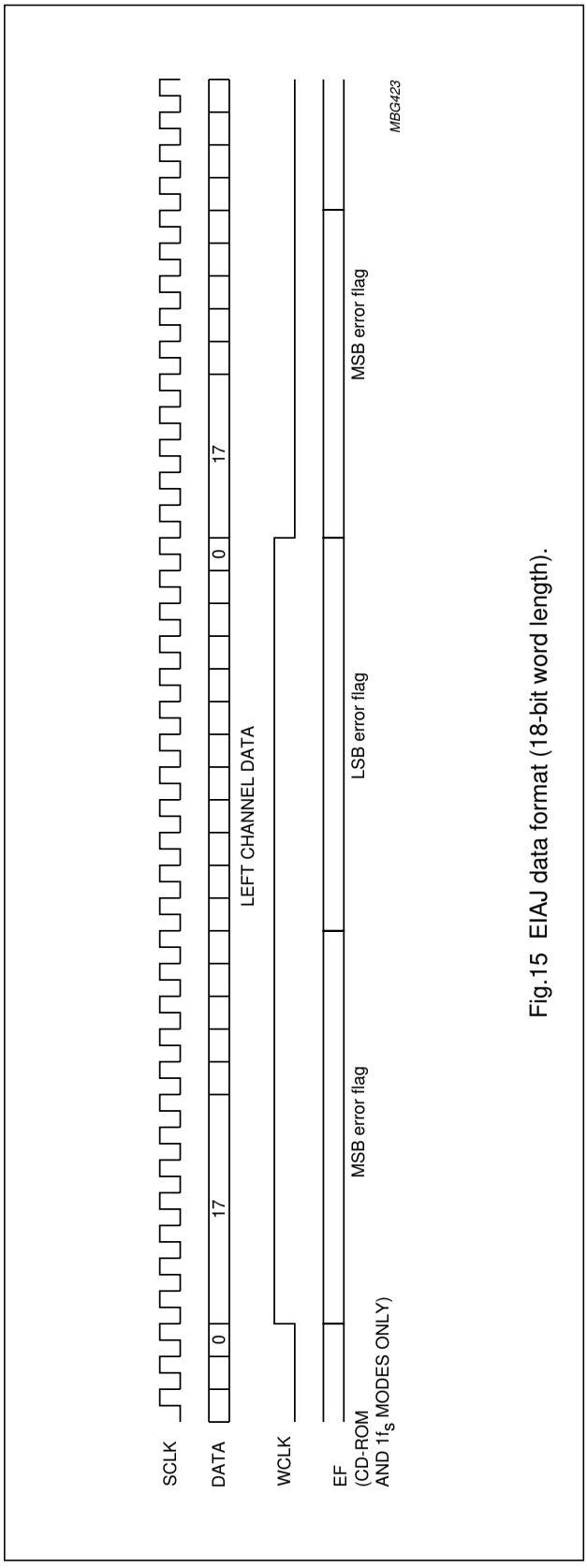


Fig.15 EIAJ data format (18-bit word length).

7.11 EBU interface

The bi-phase mark digital output signal at pin DOBM is in accordance with the format defined by the IEC 60958 specification. Three different modes can be selected via decoder register A:

- DOBM pin held LOW
- Data taken before concealment, mute and fade (must always be used for CD-ROM modes)
- Data taken after concealment, mute and fade.

An additional mute function is available via registers Shadow 7 (bank 1) and decoder register 0 and C. They provide the following:

- Hard mute: immediate mute of the audio sample in ROM mode at 1×, 2× or 4× speed
- Soft mute: 3 ms ramp up or ramp down of the audio samples in 1× audio mode
- Bypass: switches the EBU mute function out of the EBU signal path.

7.11.1 FORMAT

The digital audio output consists of 32-bit words ('subframes') transmitted in bi-phase mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384. The EBU frame format is given in Table 8.

Table 8 EBU frame format; see also Table 9

FUNCTION	BITS	DESCRIPTION
Sync	0 to 3	–
Auxiliary	4 to 7	not used; normally zero
Error flags	4	CFLG error and interpolation flags when selected by register A
Audio sample	8 to 27	first 4 bits not used (always zero); twos complement; LSB = bit 12, MSB = bit 27
Validity flag	28	valid = logic 0
User data	29	used for subcode data (Q-to-W)
Channel status	30	control bits and category code
Parity bit	31	even parity for bits 4 to 30

Table 9 Description of EBU frame function

FUNCTION	DESCRIPTION
Sync	The sync word is formed by violation of the bi-phase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The 3 different sync patterns indicate the following situations: sync B; start of a block (384 words), word contains left sample; sync M; word contains left sample (no block start) and sync W; word contains right sample.
Audio sample	Left and right samples are transmitted alternately.
Validity flag	Audio samples are flagged (bit 28 = 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment.
User data	Subcode bits Q-to-W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.
Channel status	The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is given in Table 10.

Table 10 Bit assignment

FUNCTION	BITS	DESCRIPTION
Control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3; bit 2 is logic 1 when copy permitted; bit 3 is logic 1 when recording has pre-emphasis
Reserved mode	4 to 7	always zero
Category code	8 to 15	CD: bit 8 = logic 1, all other bits = logic 0
Clock accuracy	28 to 29	set by register A; 10 = level I; 00 = level II; 01 = level III
Remaining	6 to 27 and 30 to 191	always zero

7.12 KILL features

7.12.1 THE KILL CIRCUIT

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left and right channels. This occurs in two places; prior to the digital filter (internal KILL), and in the digital DAC (loopback/external KILL). Programming bit 3 of new shadow register A (bank 2) determines whether internal or external data is used. The output is switched to active HIGH when silence has been detected for at least 270 ms, or if mute is active, or in CD-ROM mode. Two KILL modes are available which can be selected by decoder register C:

- Mono KILL: LKILL and RKILL are both active HIGH when silence is detected on left and right channels simultaneously
- Stereo KILL: LKILL and RKILL are active HIGH independently of each other when silence is detected on either channel.

7.12.2 SILENCE INJECTION

The silence inject function monitors the left and right KILL signals and forces the analog DAC into silence when KILL is asserted. This improves the internal Signal-to-Noise Ratio (S/N) by preventing any spurious noise from reaching the DAC. The silence inject function can be enabled or disabled by programming bit 2 of the new shadow register A (bank 2).

7.13 Audio features off

The audio features can be turned off (selected by decoder register E) and will affect the following functions:

- Digital filter, fade, peak detector, internal KILL circuit (although RKILL and LKILL outputs are still active) are disabled
- V5 (if selected to be the de-emphasis flag output) and the EBU outputs become undefined.

The EBU output should be set LOW prior to switching the audio features off and after switching the audio features back on; a full-scale command should be given.

7.14 The versatile pins interface

The SAA7826 has five pins that can be reconfigured for different applications.

The functions of these versatile pins are identical to the SAA732x series and can be programmed by decoder registers C, D and shadow register 3 (bank 1) as shown in Table 11.

Table 11 Pin applications

PIN NAME	PIN NUMBER	TYPE	REGISTER ADDRESS	REGISTER DATA	FUNCTION
V1	71	input	1100	XXX1	external off-track signal input
			–	XXX0	internal off-track signal used input may be read via decoder status bit; selected via register 2
V2	72	input	–	–	input may be read via decoder status bit; selected via register 2
V3	73	output	1100	00XX	output = 0
			–	01XX	output = 1
V4	74	output	1101	0000	4-line motor drive (using V4 and V5)
			–	XX01	Q-to-W subcode output
			–	XX10	output = 0
			–	XX11	output = 1
V5	75	output	1101	01XX	de-emphasis output (active HIGH)
			–	10XX	output = 0
			–	11XX	output = 1

7.15 Spindle motor control

7.15.1 MOTOR OUTPUT MODES

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal ±8 frame FIFO and disc speed information are used to calculate the motor control output signals. Several output modes, selected by decoder register 6, are supported:

- Pulse density, 2-line (true complement output), (1 × n) MHz sample frequency
- PWM output, 2-line, (22.05 × n) kHz modulation frequency
- PWM output, 4-line, (22.05 × n) kHz modulation frequency
- CDV motor mode.

7.15.1.1 Pulse density output mode

In the pulse density mode the motor output pin (MOTO1) is the pulse density modulated motor output signal.

A 50% duty factor corresponds with the motor not actuated, higher duty factors mean acceleration, lower duty factors means braking. In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a (1 × n) MHz internal clock signal.

7.15.1.2 PWM output mode (2-line)

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output. The motor braking signal is pulse-width modulated on the MOTO2 output. The timing is illustrated in Fig 16. A typical application diagram is illustrated in Fig 17.

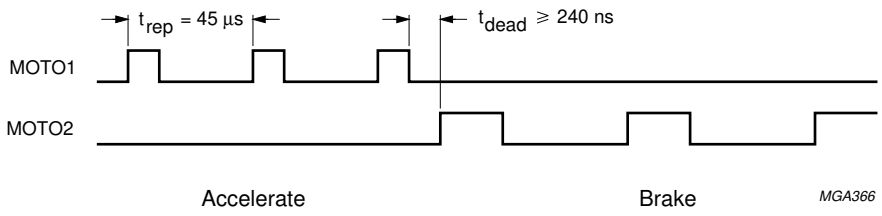


Fig.16 2-line PWM mode timing.