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TC1115

32-Bit Single-Chip Microcontroller
Advance Information

32bit

Microcontrollers



Never stop thinking.

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TC1115 Data Sheet
Advance Information

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Controller Area Network (CAN): License of Robert Bosch GmbH

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1 Summary of Features

- High Performance 32-bit TriCore™ V1.3 CPU with 4-Stage Pipeline
- Floating Point Unit (FPU)
- Dual Issue super-scalar implementation
 - MAC Instruction maximum triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- Memory Management Unit (MMU)
- On-chip Memory
 - 28-Kbyte Data Memory (SPRAM)
 - 32-Kbyte Code Memory (SPRAM)
 - 16-Kbyte Instruction Cache (ICACHE)
 - 4-Kbyte Data Cache (DCACHE)
 - 64-Kbyte SRAM Data Memory Unit (DMU)
 - 16-Kbyte Boot ROM
- On-chip Bus Systems
 - 64-bit High Performance Local Memory Bus (LMB) for fast access between caches and on-local memories and FPI Interface
 - On-chip Flexible Peripheral Interconnect Bus (FPI) for interconnections of functional units
- DMA Controller with 8 channels for data transfer operations between peripheral units and memory locations
- Two high speed Micro Link Interfaces (MLI0/1) for controller communication and emulation
- Flexible External Bus Interface Unit (EBU) to access external data memories
- One Multifunctional General Purpose Timer Unit (GPTU) with three 32-bit timer/counters
- Two Capture and Compare units (CCU60/1) for PWM signal generation, each with
 - 3-channel, 16 bit Capture and Compare unit
 - 1-channel, 16 bit Compare unit
- Three Asynchronous/Synchronous Serial Channels (ASC0/1/2) with baud-rate generator, parity, framing and overrun error detection, support FIFO and IrDA data transmission
- Two High Speed Synchronous Serial Channels (SSC0/1) with programmable data length, FIFO support and shift direction

Advance Information**Summary of Features**

- One MultiCAN module with four CAN nodes and 128 message buffers for high efficiency data handling
- Inter-IC (IIC) module with two physical IIC buses
- Digital I/O ports with 3.3 V I/O capabilities
- Level 2 On-chip Debug Support
- Power Management System
- Clock Generation Unit with PLL
- Maximum CPU and Bus clock frequency at 150 MHz without MMU and 120 MHz with MMU
- Ambient temperature under bias: -40° to +85°C
- P-LBGA-208 package

2 General Device Information

2.1 Block Diagram

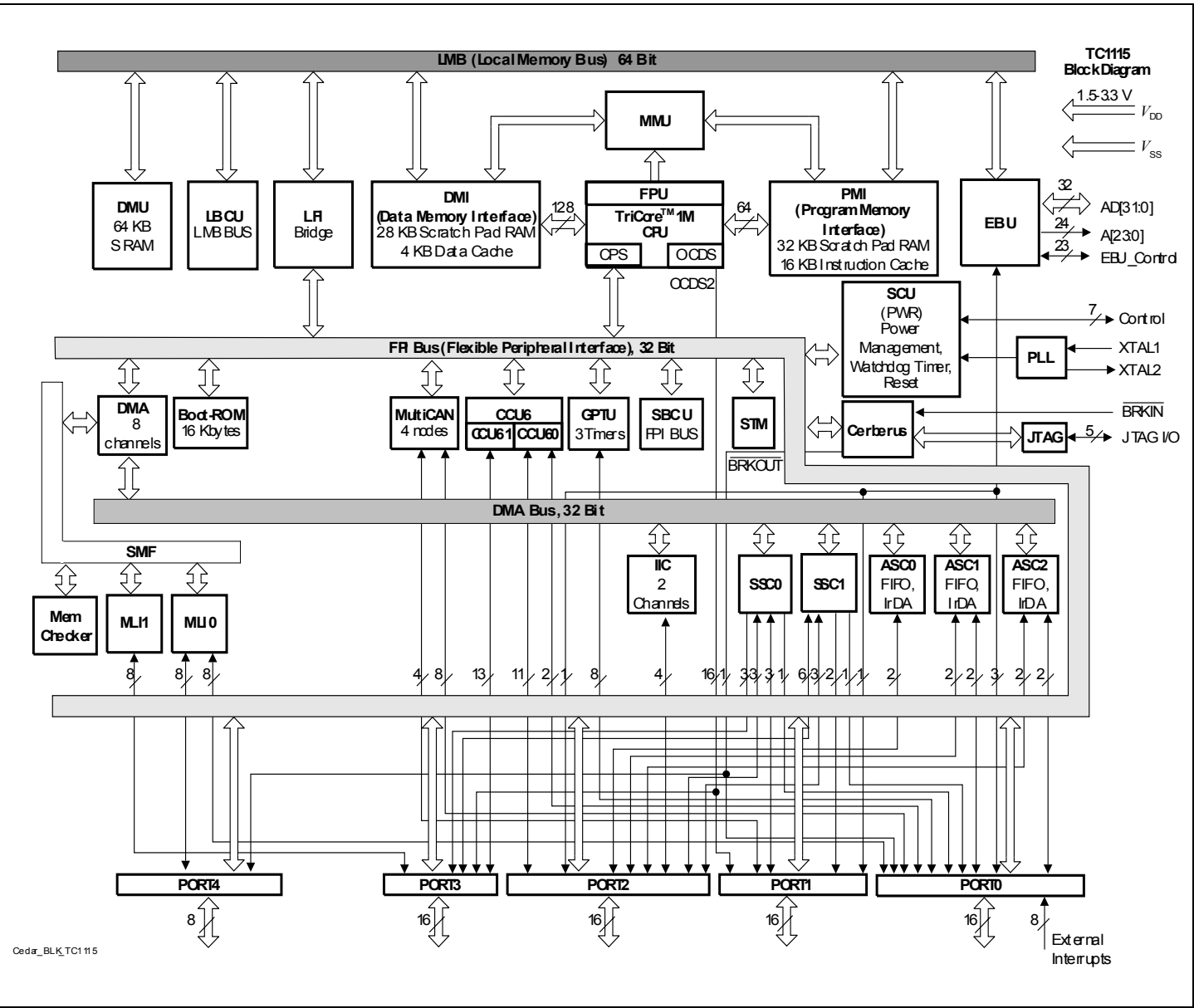


Figure 2-1 TC1115 Block Diagram

2.2 Logic Symbol

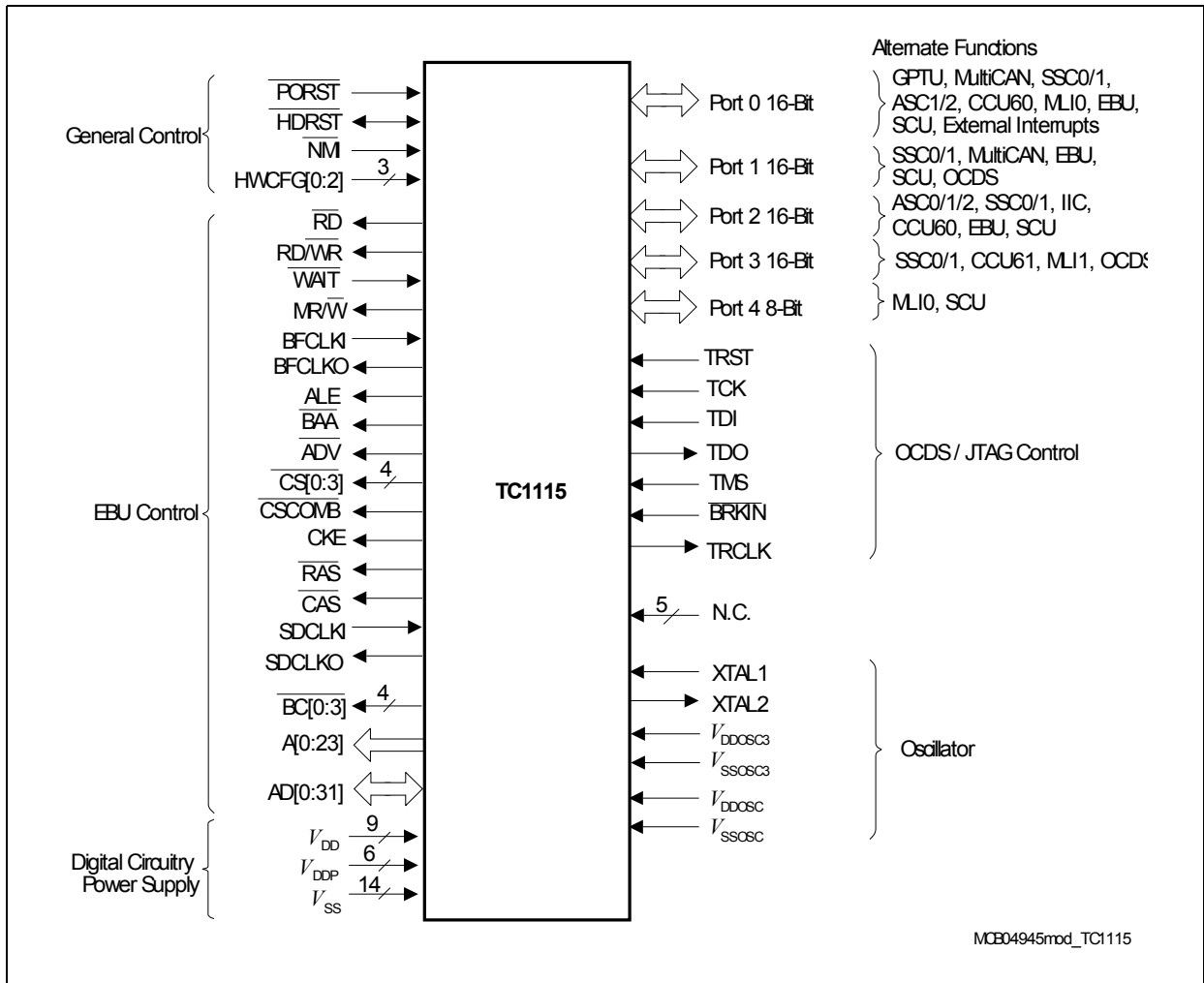


Figure 2-2 TC1115 Logic Symbol

2.3 Pin Configuration

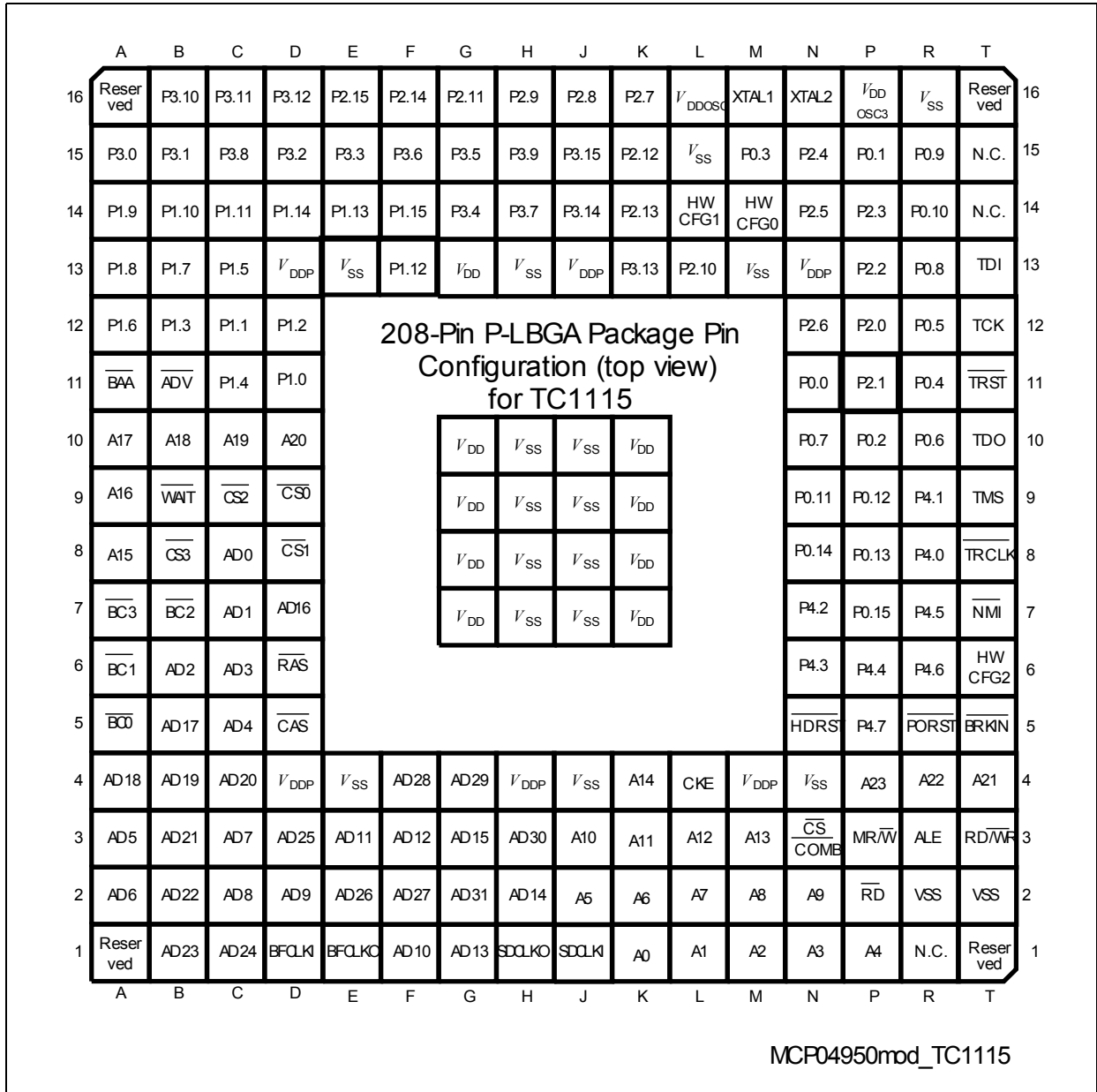


Figure 2-3 TC1115 Pins: P-BGA-208 Package (top view)

2.4 Pin Definitions and Functions
Table 2-1 Pin Definitions and Functions

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
P0		I/O		Port 0 Port 0 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for GPTU, MultiCAN, ASC1/2, SSC0/1, MLI0, EBU and SCU.
P0.0	N11	I/O	PUC	GPTU_0 GPTU input/output line 0
P0.1	P15	I/O	PUC	RXD1B ASC1 receiver input/output B
		O		TXD1B ASC1 transmitter output B
P0.2	P10	I/O	PUC	GPTU_2 GPTU input/output line 2
		I/O		RXD2B ASC2 receiver input/output B
P0.3	M15	I/O	PUC	GPTU_3 GPTU input/output line 3
		O		TXD2B ASC2 transmitter output B
P0.4	R11	I/O	PUC	GPTU_4 GPTU input/output line 4
		I		SLSI1 SSC1 Slave Select input
		O		BREQ EBU Bus Request Output
P0.5	R12	I/O	PUC	GPTU_5 GPTU input/output line 5
		I		HOLD EBU Hold Request Input
		I		CC60_T12HR CCU60 Timer 12 hardware run
		O		BRKOUT_B OCDS Break Out B
P0.6	R10	I/O	PUC	GPTU_6 GPTU input/output line 6
		I/O		HLDA EBU Hold Acknowledge Input/Output
		I		CC60_T13HR CCU60 Timer 13 hardware run
		O		SLSO0_0 SSC0 Slave Select output 0
P0.7	N10	I/O	PUC	GPTU_7 GPTU input/output line 7
		O		SLSO1_0 SSC1 Slave Select output 0
P0.8	R13	I	PUC	RXDCAN0_A CAN node 0 receiver input A
		I		REQ0 External Trigger Input 0
		O		TCLK0A MLI0 transmit channel clock output A
P0.9	R15	O	PUC	TXDCAN0_A CAN node 0 transmitter output A
		I		TREADY0A MLI0 transmit channel ready input A
		I		REQ1 External Trigger Input 1
P0.10	R14	I	PUC	RXDCAN1_A CAN node 1 receiver input A
		I		REQ2 External Trigger Input 2
		O		TVALID0A MLI0 transmit channel valid output A
P0.11	N9	O	PUC	TXDCAN1_A CAN node 1 transmitter output A
		I		REQ3 External Trigger Input 3
		O		TDATA0A MLI0 transmit channel data output A

Advance Information

General Device Information

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/PD ¹⁾	Functions
P0.12	P9	I	PUC	RXDCAN2 CAN node 2 receiver input RCLK0A MLI0 receive channel clock input A
P0.13	P8	I	PUC	REQ4 External Trigger Input 4
		O		TXDCAN2 CAN node 2 transmitter output REQ5 External Trigger Input 5
P0.14	N8	O	PUC	RREADY0A MLI0 receive channel ready output A
		I		RXDCAN3 CAN node 3 receiver input REQ6 External Trigger Input 6
P0.15	P7	I	PUC	RVALID0A MLI0 receive channel valid input A
		O		TXDCAN3 CAN node 3 transmitter output REQ7 External Trigger Input 7
		I		RDATA0A MLI0 receive channel data input A
P1		I/O		Port 1 Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for MultiCAN, CAN, OCDS L2, SSC0/1, EBU and SCU.
P1.0	D11	I	PUC	RXDCAN0_B CAN node 0 receiver input B
		O		SWCFG0 Software configuration 0 OCDSA_0 OCDS L2 Debug Line A0
P1.1	C12	I	PUC	SWCFG1 Software configuration 1
		O		TXDCAN0_B CAN node 0 transmitter output B OCDSA_1 OCDS L2 Debug Line A1
P1.2	D12	I	PUC	RXDCAN1_B CAN node 1 receiver input B
		O		SWCFG2 Software configuration 2 OCDSA_2 OCDS L2 Debug Line A2
P1.3	B12	O	PUC	TXDCAN1_B CAN node 1 transmitter output B
		I		SWCFG3 Software configuration 3 OCDSA_3 OCDS L2 Debug Line A3
P1.4	C11	O	PUC	OCDSA_4 OCDS L2 Debug Line A4
		I		SWCFG4 Software configuration 4
P1.5	C13	O	PUC	OCDSA_5 OCDS L2 Debug Line A5
		I		SWCFG5 Software configuration 5
P1.6	A12	O	PUC	OCDSA_6 OCDS L2 Debug Line A6
		I		SWCFG6 Software configuration 6

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General Device Information
Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions	
P1.7	B13	I	PUC	SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	O	PUC	SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
P1.15	F14	O	PUC	OCDSA_14	OCDS L2 Debug Line A14
		I		SLSI0	SSC0 Slave Select Input
		O		RMW	EBU Read Modify Write
		I		SWCFG15	Software configuration 15
		O		OCDSA_15	OCDS L2 Debug Line A15

Advance Information
General Device Information
Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
P2		I/O		Port 2 Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1/2, SSC0/1, CCU60, IIC, EBU and SCU.
P2.0	P12	I/O O	PUC	RXD0 ASC0 receiver input/output line CSEMU EBU Chip Select Output for Emulator Region
P2.1	P11	O I	PUC	TXD0 ASC0 transmitter output line TESTMODE Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0 SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0 SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0 SSC0 clock input/output line
P2.5	N14	O I/O	PUC	COUT60_3 CCU60 compare channel 3 output MRST1A SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O I/O	PUC	CC60_0 CCU60 input/output of capture/compare channel 0 MTSR1A SSC1 master transmit/slave receive input/output A
P2.7	K16	O	PUC	COUT60_0 CCU60 output of capture/compare channel 0
P2.8	J16	I/O I/O	PUC	SCLK1A SSC1 clock input/output line A CC60_1 CCU60 input/output of capture/compare channel 1
P2.9	H16	O I/O	PUC	RXD1A ASC1 receiver input/output line A COUT60_1 CCU60 output of capture/compare channel 1
P2.10	L13	O I/O	PUC	TXD1A ASC1 transmitter output line A CC60_2 CCU60 input/output of capture/compare channel 2
P2.11	G16	I/O O	PUC	RXD2A ASC2 receiver input/output line A COUT60_2 CCU60 output of capture/compare channel 2
P2.12	K15	O I/O I O	—	TXD2A ASC2 transmitter output line A SDA0 IIC Serial Data line 0 CTRAP0 CCU60 trap input SLSO0_3 SSC0 Slave Select output 3

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General Device Information
Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
P2.13	K14	I/O	—	SCL0 IIC clock line 0
		I		CCPOS0_0 CCU60 Hall input signal 0
		O		SLSO1_3 SSC1 Slave Select output 3
P2.14	F16	I	—	CCPOS0_1 CCU60 Hall input signal 1
		I/O		SDA1 IIC Serial Data line 1
		O		SLSO0_4 SSC0 Slave Select output 4
P2.15	E16	I	—	CCPOS0_2 CCU60 Hall input signal 2
		I/O		SCL1 IIC clock line 1
		O		SLSO1_4 SSC1 Slave Select output 4

Advance Information
General Device Information
Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
P3		I/O		Port 3 Port 3 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for MLI1, CCU61, SSC0/1 and OCDS Level 2 debug lines.
P3.0	A15	O	PUC	OCDSB_0 OCDS L2 Debug Line B0
P3.1	B15	O	PUC	COUT61_3 CCU61 compare channel 3 output
		I/O		OCDSB_1 OCDS L2 Debug Line B1 CC61_0 CCU61 input/output of capture/ compare channel 0
P3.2	D15	O	PUC	OCDSB_2 OCDS L2 Debug Line B2
		O		COUT61_0 CCU61 output of capture/compare channel 0
P3.3	E15	O	PUC	OCDSB_3 OCDS L2 Debug Line B3
		I/O		CC61_1 CCU61 input/output of capture/ compare channel 1
P3.4	G14	O	PUC	OCDSB_4 OCDS L2 Debug Line B4
		O		COUT61_1 CCU61 output of capture/compare channel 1
P3.5	G15	O	PUC	OCDSB_5 OCDS L2 Debug Line B5
		I/O		CC61_2 CCU61 input/output of capture/ compare channel 2
P3.6	F15	O	PUC	OCDSB_6 OCDS L2 Debug Line B6
		O		COUT61_2 CCU61 output of capture/compare channel 2
P3.7	H14	O	PUC	OCDSB_7 OCDS L2 Debug Line B7
		I		CTRAP1 CCU61 trap input
		O		SLSO0_5 SSC0 Slave Select output 5
P3.8	C15	O	PUC	OCDSB_8 OCDS L2 Debug Line B8
		I		CCPOS1_0 CCU61 Hall input signal 0
		O		TCLK1 MLI1 transmit channel clock output
		O		SLSO1_5 SSC1 Slave Select output 5
P3.9	H15	O	PUC	OCDSB_9 OCDS L2 Debug Line B9
		I		CCPOS1_1 CCU61 Hall input signal 1
		I		TREADY1 MLI1 transmit channel ready input
P3.10	B16	O	PUC	SLSO0_6 SSC0 Slave Select output 6
		O		OCDSB_10 OCDS L2 Debug Line B10
		I		CCPOS1_2 CCU61 Hall input signal 2
		O		TVALID1 MLI1 transmit channel valid output
		O		SLSO1_6 SSC1 Slave Select output 6

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General Device Information
Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
P3.11	C16	O	PUC	OCDSB_11 OCDS L2 Debug Line B11
		O		TDATA1 MLI1 transmit channel data output
		O		SLSO0_7 SSC0 Slave Select output 7
		I		CC61_T12HR CCU61 Timer 12 hardware run
P3.12	D16	O	PUC	OCDSB_12 OCDS L2 Debug Line B12
		I		RCLK1 MLI1 receive channel clock input
		O		SLSO1_7 SSC1 Slave Select output 7
		I		CC61_T13HR CCU61 Timer 13 hardware run
P3.13	K13	O	PUC	OCDSB_13 OCDS L2 Debug Line B13
		O		RREADY1 MLI1 receive channel ready output
		I/O		MRST1B SSC1 master receive/slave transmit input/output B
P3.14	J14	O	PUC	OCDSB_14 OCDS L2 Debug Line B14
		I		RVALID1 MLI1 receive channel valid input
		I/O		MTSR1B SSC1 master transmit/slave receive input/output B
P3.15	J15	O	PUC	OCDSB_15 OCDS L2 Debug Line B15
		I		RDATA1 MLI1 receive channel data input
		I/O		SCLK1B SSC1 clock input/output line B
P4		I/O		Port 4 Port 4 is an 8-bit bi-directional general purpose I/O port which can be alternatively used for MLI0 and SCU.
P4.0	R8	O	PUC	TCLK0B MLI0 transmit channel clock output B
P4.1	R9	I	PUC	TREADY0B MLI0 transmit channel ready input B
P4.2	N7	O	PUC	TVALID0B MLI0 transmit channel valid output B
P4.3	N6	O	PUC	TDATA0B MLI0 transmit channel data output B
P4.4	P6	I	PUC	RCLK0B MLI0 receive channel clock input B
P4.5	R7	O	PUC	RREADY0B MLI0 receive channel ready output B
P4.6	R6	I	PUC	RVALID0B MLI0 receive channel valid input B
P4.7	P5	I	PUC	RDATA0B MLI0 receive channel data input B
		O		BRKOUT_A OCDS Break Out A

Advance Information
General Device Information
Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD¹⁾	Functions
HDRST	N5	I/O	PUA	Hardware Reset Input/Reset Indication Output Assertion of this bi-directional open-drain pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for a minimum $4f_{CPU}$ clock cycles. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset for a specific period of time. For a software reset, activation of this pin is programmable.
PORST	R5	I	PUC	Power-on Reset Input A low level on \overline{PORST} causes an asynchronous reset of the entire chip. \overline{PORST} is a fully asynchronous level sensitive signal.
NMI	T7	I	PUC	Non-Maskable Interrupt Input A high-to-low transition on this pin causes an NMI-Trap request to the CPU.
TRST	T11	I	PDC	JTAG Module Reset/Enable Input A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	T12	I	PUC	JTAG Module Clock Input
TDI	T13	I	PUC	JTAG Module Serial Data Input
TDO	T10	O	—	JTAG Module Serial Data Output
TMS	T9	I	PUC	JTAG Module State Machine Control Input
TRCLK	T8	O	—	Trace Clock for OCDS_L2 Lines
HWCFG0	M14	I	PUC	Hardware Configuration Inputs The Configuration Inputs define the boot options of the TC1115 after a hardware invoked reset operation.
HWCFG1	L14	I	PUC	
HWCFG2	T6	I	PDC	
BRKIN	T5	I	PUC	OCDS Break Input A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.

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General Device Information

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
CS0	D9	O	PUC	EBU Chip Select Output Line 0
CS1	D8	O	PUC	EBU Chip Select Output Line 1
CS2	C9	O	PUC	EBU Chip Select Output Line 2
CS3	B8	O	PUC	EBU Chip Select Output Line 3 Each corresponds to a programmable region. Only one can be active at one time.
CSCOMB	N3	O	PUC	EBU Chip Select Output for combination function (Overlay Memory and Global)
SDCLKI	J1	I	—	SDRAM Clock Input (Clock Feedback)
SDCLKO	H1	O	—	SDRAM Clock Output Accesses to SDRAM devices are synchronized to this clock.
RAS	D6	O	PUC	EBU SDRAM Row Address Strobe Output
CAS	D5	O	PUC	EBU SDRAM Column Address Strobe Output
CKE	L4	O	PUC	EBU SDRAM Clock Enable Output
BFCLKI	D1	I	—	Burst Flash Clock Input (Clock Feedback)
BFCLKO	E1	O	—	Burst Flash Clock Output Accesses to Burst Flash devices are synchronized to this clock.
RD	P2	O	PUC	EBU Read Control Line Output in master mode Input in slave mode
RD/WR	T3	O	PUC	EBU Write Control Line Output in master mode Input in slave mode
WAIT	B9	I	PUC	EBU Wait Control Line
ALE	R3	O	PDC	EBU Address Latch Enable Output
MR/W	P3	O	PUC	EBU Motorola-style Read/Write Output
BAA	A11	O	PUC	EBU Burst Address Advance Output For advancing address in a Burst Flash access
ADV	B11	O	PUC	EBU Burst Flash Address Valid Output

Advance Information

General Device Information

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
EBU Address/Data Bus Input/Output Lines				
AD0	C8	I/O	PUC	EBU Address/Data Bus Line 0
AD1	C7	I/O	PUC	EBU Address/Data Bus Line 1
AD2	B6	I/O	PUC	EBU Address/Data Bus Line 2
AD3	C6	I/O	PUC	EBU Address/Data Bus Line 3
AD4	C5	I/O	PUC	EBU Address/Data Bus Line 4
AD5	A3	I/O	PUC	EBU Address/Data Bus Line 5
AD6	A2	I/O	PUC	EBU Address/Data Bus Line 6
AD7	C3	I/O	PUC	EBU Address/Data Bus Line 7
AD8	C2	I/O	PUC	EBU Address/Data Bus Line 8
AD9	D2	I/O	PUC	EBU Address/Data Bus Line 9
AD10	F1	I/O	PUC	EBU Address/Data Bus Line 10
AD11	E3	I/O	PUC	EBU Address/Data Bus Line 11
AD12	F3	I/O	PUC	EBU Address/Data Bus Line 12
AD13	G1	I/O	PUC	EBU Address/Data Bus Line 13
AD14	H2	I/O	PUC	EBU Address/Data Bus Line 14
AD15	G3	I/O	PUC	EBU Address/Data Bus Line 15
AD16	D7	I/O	PUC	EBU Address/Data Bus Line 16
AD17	B5	I/O	PUC	EBU Address/Data Bus Line 17
AD18	A4	I/O	PUC	EBU Address/Data Bus Line 18
AD19	B4	I/O	PUC	EBU Address/Data Bus Line 19
AD20	C4	I/O	PUC	EBU Address/Data Bus Line 20
AD21	B3	I/O	PUC	EBU Address/Data Bus Line 21
AD22	B2	I/O	PUC	EBU Address/Data Bus Line 22
AD23	B1	I/O	PUC	EBU Address/Data Bus Line 23
AD24	C1	I/O	PUC	EBU Address/Data Bus Line 24
AD25	D3	I/O	PUC	EBU Address/Data Bus Line 25
AD26	E2	I/O	PUC	EBU Address/Data Bus Line 26
AD27	F2	I/O	PUC	EBU Address/Data Bus Line 27
AD28	F4	I/O	PUC	EBU Address/Data Bus Line 28
AD29	G4	I/O	PUC	EBU Address/Data Bus Line 29
AD30	H3	I/O	PUC	EBU Address/Data Bus Line 30
AD31	G2	I/O	PUC	EBU Address/Data Bus Line 31
<u>BC0</u>	A5	O	PUC	EBU Byte Control Line 0
<u>BC1</u>	A6	O	PUC	EBU Byte Control Line 1
<u>BC2</u>	B7	O	PUC	EBU Byte Control Line 2
<u>BC3</u>	A7	O	PUC	EBU Byte Control Line 3

Advance Information

General Device Information

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
EBU Address Bus Input/Output Lines				
A0	K1	O	PUC	EBU Address Bus Line 0
A1	L1	O	PUC	EBU Address Bus Line 1
A2	M1	O	PUC	EBU Address Bus Line 2
A3	N1	O	PUC	EBU Address Bus Line 3
A4	P1	O	PUC	EBU Address Bus Line 4
A5	J2	O	PUC	EBU Address Bus Line 5
A6	K2	O	PUC	EBU Address Bus Line 6
A7	L2	O	PUC	EBU Address Bus Line 7
A8	M2	O	PUC	EBU Address Bus Line 8
A9	N2	O	PUC	EBU Address Bus Line 9
A10	J3	O	PUC	EBU Address Bus Line 10
A11	K3	O	PUC	EBU Address Bus Line 11
A12	L3	O	PUC	EBU Address Bus Line 12
A13	M3	O	PUC	EBU Address Bus Line 13
A14	K4	O	PUC	EBU Address Bus Line 14
A15	A8	O	PUC	EBU Address Bus Line 15
A16	A9	O	PUC	EBU Address Bus Line 16
A17	A10	O	PUC	EBU Address Bus Line 17
A18	B10	O	PUC	EBU Address Bus Line 18
A19	C10	O	PUC	EBU Address Bus Line 19
A20	D10	O	PUC	EBU Address Bus Line 20
A21	T4	O	PUC	EBU Address Bus Line 21
A22	R4	O	PUC	EBU Address Bus Line 22
A23	P4	O	PUC	EBU Address Bus Line 23
XTAL1 XTAL2	M16 N16	I O	— —	Oscillator/PLL/Clock Generator Input/Output Pins XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking of the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation, XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC3}	P16	—	—	Main Oscillator Power Supply (3.3 V)
V_{SSOSC3}	R16	—	—	Main Oscillator Ground
V_{DDOSC}	L16	—	—	Main Oscillator Power Supply (1.5 V)

Advance Information

General Device Information

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD ¹⁾	Functions
V_{SSOSC}	L15	—	—	Main Oscillator Ground
V_{DD}	G7 G8 G9 G10 G13 K7,K8 K9 K10	—	—	Core and Logic Power Supply (1.5 V)
V_{DDP}	D4 D13 H4 J13 M4 N13	—	—	Ports Power Supply (3.3 V)
V_{SS}	E4 E13 H7 H8 H9 H10 H13 J4,J7 J8,J9 J10 M13 N4 R2,T2	—	—	Ground
N.C.	A1 A16 T1,R1 T14 T15 T16	—	—	Not Connected These pins must not be connected.

1) Refers to internal pull-up or pull-down device connected and corresponding type. The notation '—' indicates that the internal pull-up or pull-down device is not enabled.

Note: P2.12 to P2.15 are always configured as open drain.

3 Functional Description

3.1 On-Chip Memories

The TC1115 provides the following on-chip memories:

- Program Memory Interface (PMI) with
 - 32-Kbyte Scratch-pad Code RAM (SPRAM)
 - 16-Kbyte Instruction Cache Memory (ICACHE)
- Data Memory Interface (DMI) with
 - 28-Kbyte Scratch-pad Data RAM (SPRAM)
 - 4-Kbyte Data Cache Memory (DCACHE)
- Data Memory Unit (DMU) with
 - 64-Kbyte SRAM
- 16-Kbyte Boot ROM (BROM)

Advance Information

Functional Description

3.2 Address Map

Table 3-1 defines the specific segment oriented address blocks of the TC1115 with its address range, size, and PMI/DMI access view. Table 3-2 shows the block address map of the Segment 15 which includes on-chip peripheral units and ports.

Table 3-1 TC1115 Block Address Map

Segment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
0 – 7	0000 0000 _H – 7FFF FFFF _H	2 GB	MMU Space	via FPI	via FPI	c a c h e d
8	8000 0000 _H – 8FFF FFFF _H	256 MB	External Memory Space mapped from Segment 10	via LMB	via LMB	
9	9000 0000 _H – 9FDF FFFF _H	256 MB	Reserved	via FPI	via FPI	
10	A000 0000 _H – AFBF FFFF _H	252 MB	External Memory Space	via LMB	via LMB	n o n- c a c h e d
	AFC0 0000 _H – AFC0 FFFF _H	64 KB	DMU Space			
	AFC1 0000 _H – AFFF FFFF _H	~4 MB	Reserved			
11	B000 0000 _H – BFFF FFFF _H	256 MB	Reserved	via FPI	via FPI	
12	C000 0000 _H – C000 FFFF _H	64 KB	DMU	via LMB	via LMB	
	C001 0000 _H – CFFF FFFF _H	~ 256 MB	Reserved			