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TC1130

32-Bit Single-Chip Microcontroller

Advance Information

Microcontrollers

Infineon technologies

Never stop thinking.

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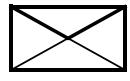

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Advance Information

32-Bit Single-Chip Microcontroller **TC1130**
TriCore™ Family

1 Summary of Features

- High Performance 32-bit TriCore™ V1.3 CPU with 4-Stage Pipeline
- Floating Point Unit (FPU)
- Dual Issue super-scalar implementation
  - MAC Instruction maximum triple issue
- Circular Buffer and bit-reverse addressing modes for DSP algorithms
- Very fast interrupt response time
- Hardware controlled context switch for task switch and interrupts
- Memory Management Unit (MMU)
- On-chip Memory
  - 28-Kbyte Data Memory (SPRAM)
  - 32-Kbyte Code Memory (SPRAM)
  - 16-Kbyte Instruction Cache (ICACHE)
  - 4-Kbyte Data Cache (DCACHE)
  - 64-Kbyte SRAM Data Memory Unit (DMU)
  - 16-Kbyte Boot ROM
- On-chip Bus Systems
  - 64-bit High Performance Local Memory Bus (LMB) for fast access between caches and on-local memories and FPI Interface
  - On-chip Flexible Peripheral Interconnect Bus (FPI) for interconnections of functional units
- DMA Controller with 8 channels for data transfer operations between peripheral units and memory locations
- Two high speed Micro Link Interfaces (MLI0/1) for controller communication and emulation
- Flexible External Bus Interface Unit (EBU) to access external data memories
- One Multifunctional General Purpose Timer Unit (GPTU) with three 32-bit timer/ counters
- Two Capture and Compare units (CCU60/1) for PWM signal generation, each with
  - 3-channel, 16 bit Capture and Compare unit
  - 1-channel, 16 bit Compare unit
- Three Asynchronous/Synchronous Serial Channels (ASC0/1/2) with baud-rate generator, parity, framing and overrun error detection, support FIFO and IrDA data transmission
- Two High Speed Synchronous Serial Channels (SSC0/1) with programmable data length, FIFO support and shift direction

- One MultiCAN module with four CAN nodes and 128 message buffers for high efficiency data handling
- Fast Ethernet Controller with 10/100 Mbit/sec MII-Based physical devices support
- USB module with compliance to USB Specification Revision 1.1, with support for 1.5 MBaud to 12 MBaud devices
- Inter-IC (IIC) module with two physical IIC buses
- Digital I/O ports with 3.3 V I/O capabilities
- Level 2 On-chip Debug Support
- Power Management System
- Clock Generation Unit with PLL
- Maximum CPU and Bus clock frequency at 150 MHz without MMU and 120 MHz with MMU
- Ambient temperature under bias: -40° to +85°C
- P-LBGA-208 package

2 General Device Information

2.1 Block Diagram

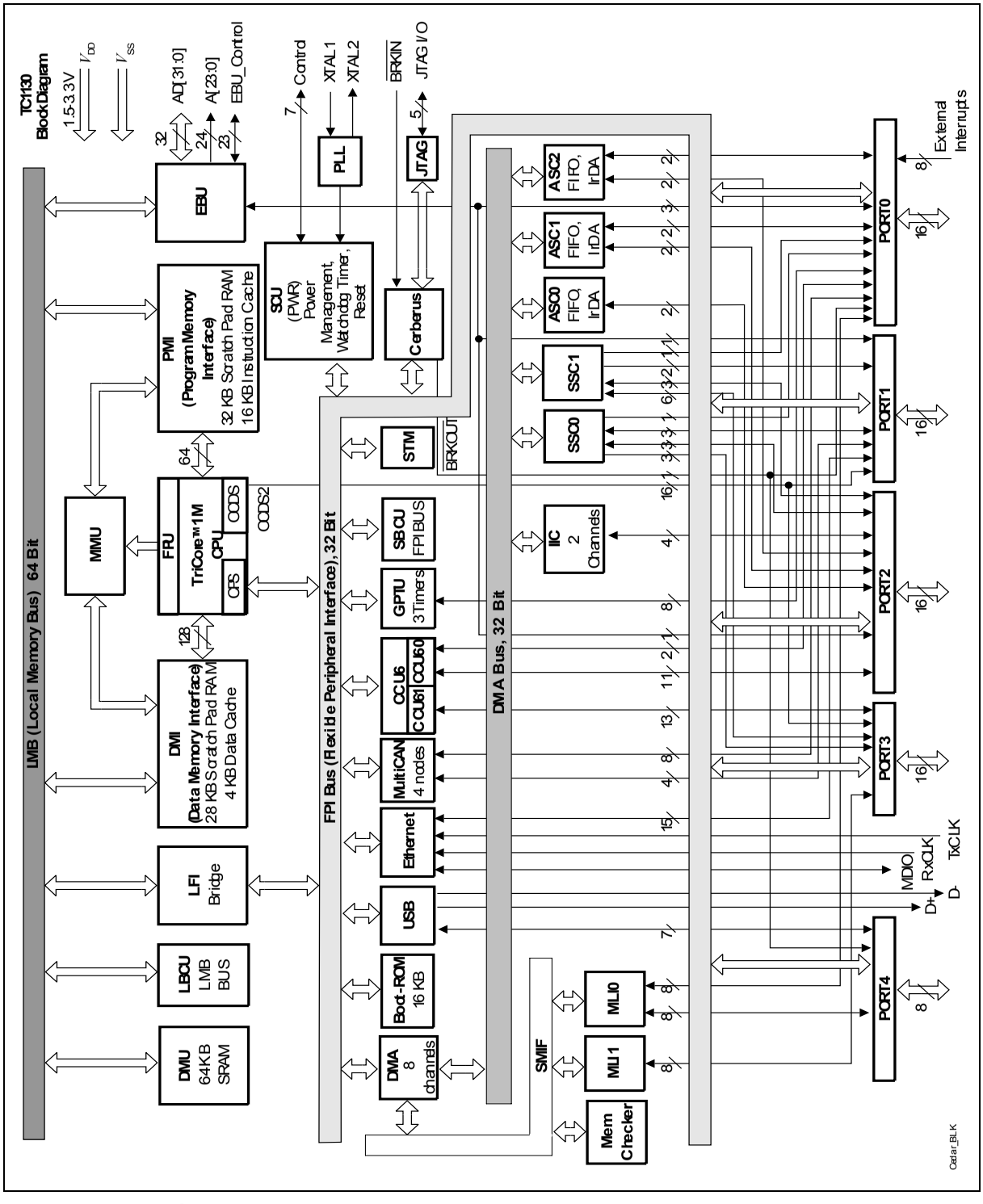

Figure 2-1 TC1130 Block Diagram

2.2 Logic Symbol

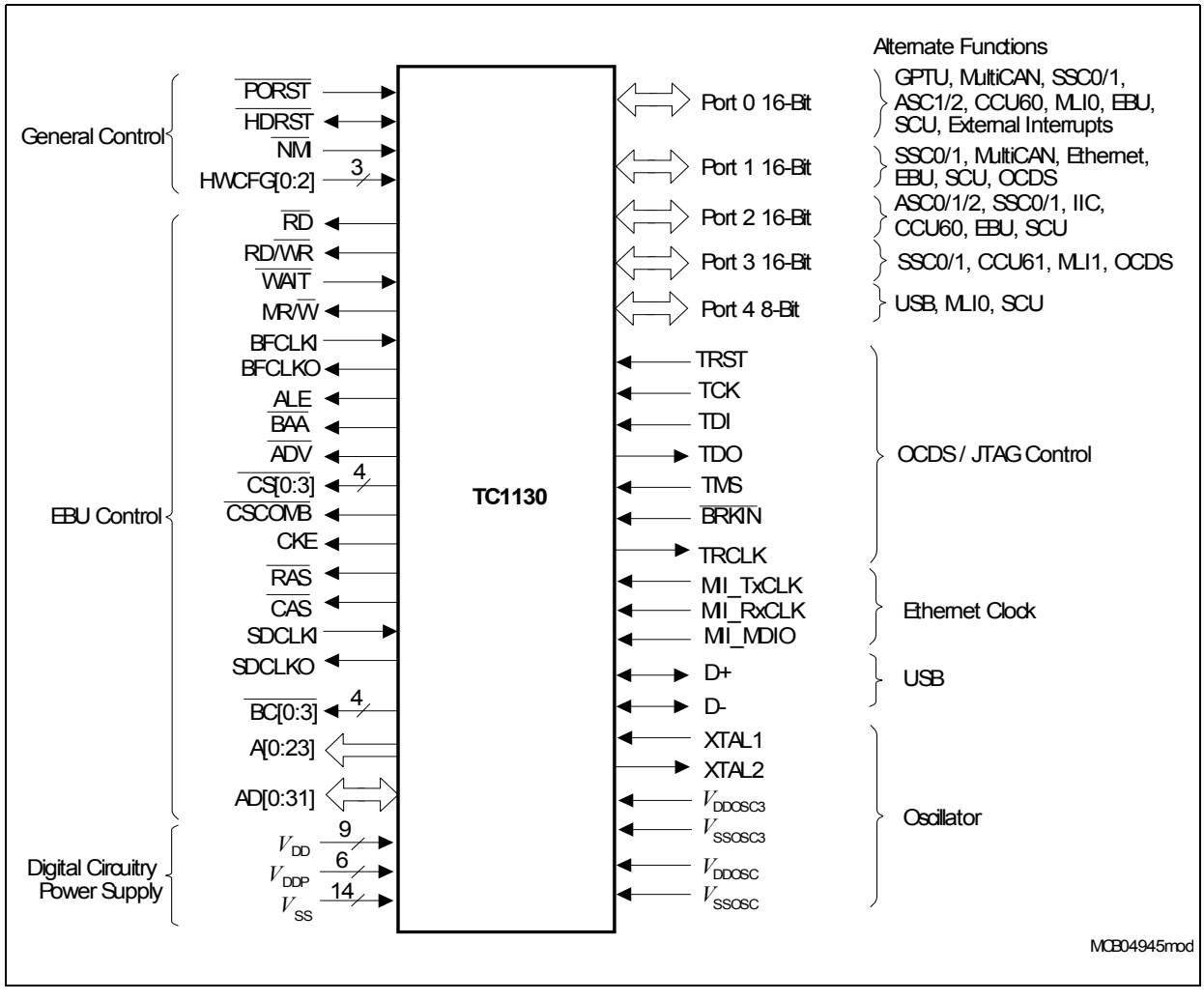

Figure 2-2 TC1130 Logic Symbol

2.3 Pin Configuration

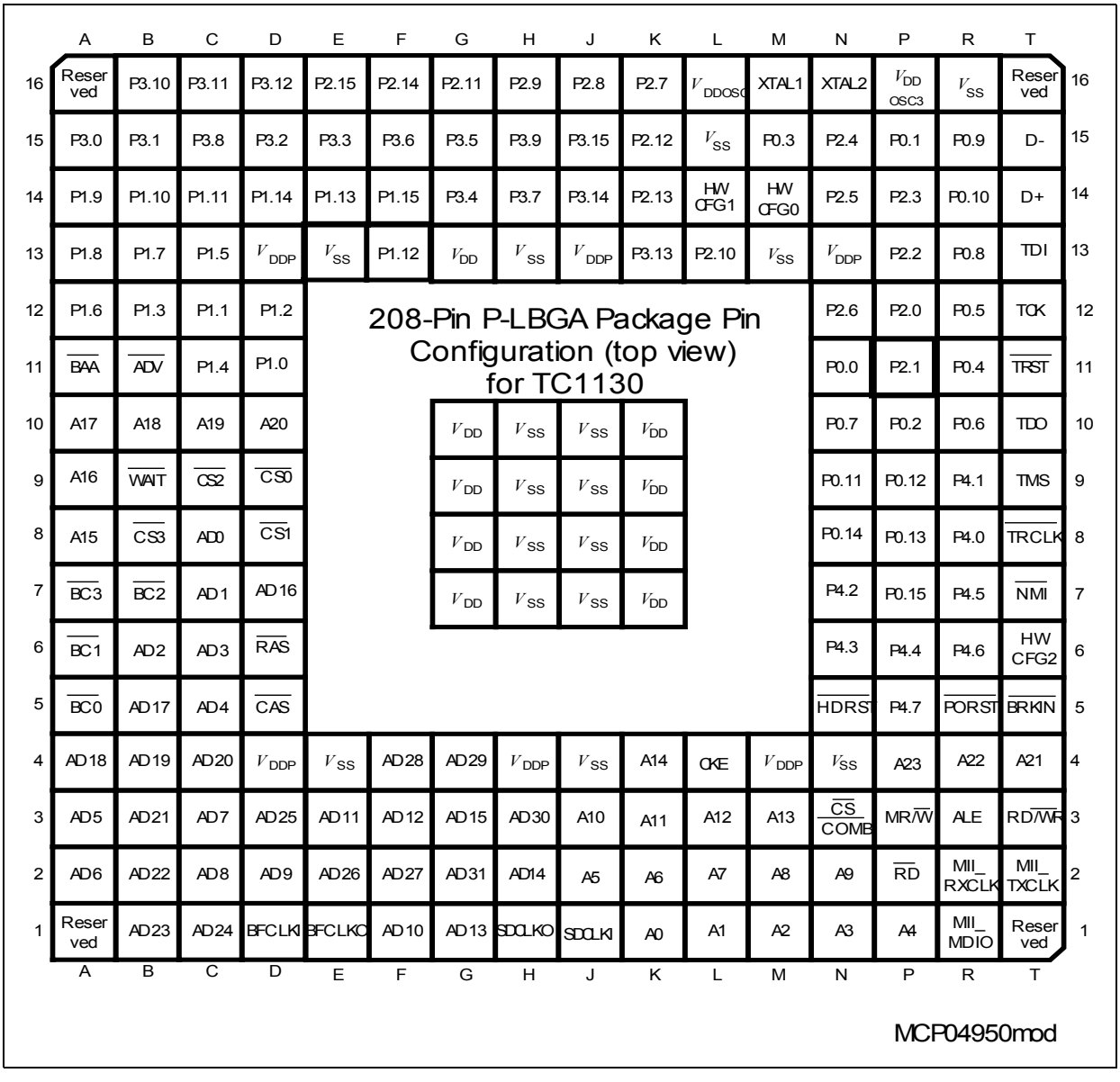

Figure 2-3 TC1130 Pins: P-BGA-208 Package (top view)

2.4 Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P0		I/O		**Port 0** Port 0 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for GPTU, MultiCAN, ASC1/2, SSC0/1, MLI0, EBU and SCU.	
P0.0	N11	I/O	PUC	GPTU_0	GPTU input/output line 0
		I/O		RXD1B	ASC1 receiver input/output B
P0.1	P15	I/O	PUC	GPTU_1	GPTU input/output line 1
		O		TXD1B	ASC1 transmitter output B
P0.2	P10	I/O	PUC	GPTU_2	GPTU input/output line 2
		I/O		RXD2B	ASC2 receiver input/output B
P0.3	M15	I/O	PUC	GPTU_3	GPTU input/output line 3
		O		TXD2B	ASC2 transmitter output B
P0.4	R11	I/O	PUC	GPTU_4	GPTU input/output line 4
		I		SLSI1	SSC1 Slave Select input
		O		BREQ	EBU Bus Request Output
P0.5	R12	I/O	PUC	GPTU_5	GPTU input/output line 5
		I		HOLD	EBU Hold Request Input
		I		CC60_T12HR	CCU60 Timer 12 hardware run
		O		BRKOUT_B	OCDS Break Out B
P0.6	R10	I/O	PUC	GPTU_6	GPTU input/output line 6
		I/O		HLDA	EBU Hold Acknowledge Input/Output
		I		CC60_T13HR	CCU60 Timer 13 hardware run
		O		SLSO0_0	SSC0 Slave Select output 0
P0.7	N10	I/O	PUC	GPTU_7	GPTU input/output line 7
		O		SLSO1_0	SSC1 Slave Select output 0
P0.8	R13	I	PUC	RXDCAN0_A	CAN node 0 receiver input A
		I		REQ0	External Trigger Input 0
		O		TCLK0A	MLI0 transmit channel clock output A
P0.9	R15	O	PUC	TXDCAN0_A	CAN node 0 transmitter output A
		I		TREADY0A	MLI0 transmit channel ready input A
		I		REQ1	External Trigger Input 1
P0.10	R14	I	PUC	RXDCAN1_A	CAN node 1 receiver input A
		I		REQ2	External Trigger Input 2
		O		TVALID0A	MLI0 transmit channel valid output A
P0.11	N9	O	PUC	TXDCAN1_A	CAN node 1 transmitter output A
		I		REQ3	External Trigger Input 3
		O		TDATA0A	MLI0 transmit channel data output A

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P0.12	P9	I	PUC	RXDCAN2	CAN node 2 receiver input
		I		RCLK0A	MLI0 receive channel clock input A
		I		REQ4	External Trigger Input 4
P0.13	P8	O	PUC	TXDCAN2	CAN node 2 transmitter output
		I		REQ5	External Trigger Input 5
		O		RREADY0A	MLI0 receive channel ready output A
P0.14	N8	I	PUC	RXDCAN3	CAN node 3 receiver input
		I		REQ6	External Trigger Input 6
		I		RVALID0A	MLI0 receive channel valid input A
P0.15	P7	O	PUC	TXDCAN3	CAN node 3 transmitter output
		I		REQ7	External Trigger Input 7
		I		RDATA0A	MLI0 receive channel data input A

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1		I/O		**Port 1** Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for Ethernet controller, MultiCAN, CAN, OCDS L2, SSC0/1, EBU and SCU.	
P1.0	D11	O	PUC	MII_TXD0	Ethernet controller transmit data output line 0
		I		RXDCAN0_B	CAN node 0 receiver input B
		I		SWCFG0	Software configuration 0
		O		OCDSA_0	OCDS L2 Debug Line A0
P1.1	C12	O	PUC	MII_TXD1	Ethernet controller transmit data output line 1
		I		SWCFG1	Software configuration 1
		O		TXDCAN0_B	CAN node 0 transmitter output B
		O		OCDSA_1	OCDS L2 Debug Line A1
P1.2	D12	O	PUC	MII_TXD2	Ethernet controller transmit data output line 2
		I		RXDCAN1_B	CAN node 1 receiver input B
		I		SWCFG2	Software configuration 2
		O		OCDSA_2	OCDS L2 Debug Line A2
P1.3	B12	O	PUC	MII_TXD3	Ethernet controller transmit data output line 3
		O		TXDCAN1_B	CAN node 1 transmitter output B
		I		SWCFG3	Software configuration 3
		O		OCDSA_3	OCDS L2 Debug Line A3
P1.4	C11	O	PUC	MII_TXER	Ethernet controller transmit error output line
		I		SWCFG4	Software configuration 4
		O		OCDSA_4	OCDS L2 Debug Line A4
P1.5	C13	O	PUC	MII_TXEN	Ethernet controller transmit enable output line
		I		SWCFG5	Software configuration 5
		O		OCDSA_5	OCDS L2 Debug Line A5
P1.6	A12	O	PUC	MII_MDC	Ethernet controller management data clock output line
		I		SWCFG6	Software configuration 6
		O		OCDSA_6	OCDS L2 Debug Line A6

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1.7	B13	I	PUC	MII_RXDV	Ethernet Controller receive data valid input line
		I		SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	MII_CRS	Ethernet Controller carrier input line
		I		SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	MII_COL	Ethernet Controller collision input line
		I		SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	MII_RXD0	Ethernet Controller receive data input line 0
		I		SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	MII_RXD1	Ethernet Controller receive data input line 1
		I		SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	MII_RXD2	Ethernet Controller receive data input line 2
		I		SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	MII_RXD3	Ethernet Controller receive data input line 3
		I		SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	I	PUC	MII_RXER	Ethernet Controller receive error input line
		O		SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14
P1.15	F14	I	PUC	SLSI0	SSC0 Slave Select Input
		O		RMW	EBU Read Modify Write
		I		SWCFG15	Software configuration 15
		O		OCDSA_15	OCDS L2 Debug Line A15

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P2		I/O		**Port 2** Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1/2, SSC0/1, CCU60, IIC, EBU and SCU.	
P2.0	P12	I/O	PUC	RXD0	ASC0 receiver input/output line
		O		CSEMU	EBU Chip Select Output for Emulator Region
P2.1	P11	O	PUC	TXD0	ASC0 transmitter output line
		I		TESTMODE	Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0	SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0	SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0	SSC0 clock input/output line
P2.5	N14	O	PUC	COUT60_3	CCU60 compare channel 3 output
		I/O		MRST1A	SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O	PUC	CC60_0	CCU60 input/output of capture compare channel 0
		I/O		MTSR1A	SSC1 master transmit/slave receive input/output A
P2.7	K16	O	PUC	COUT60_0	CCU60 output of capture/compare channel 0
		I/O		SCLK1A	SSC1 clock input/output line A
P2.8	J16	I/O	PUC	CC60_1	CCU60 input/output of capture/ compare channel 1
		I/O		RXD1A	ASC1 receiver input/output line A
P2.9	H16	O	PUC	COUT60_1	CCU60 output of capture/compare channel 1
		O		TXD1A	ASC1 transmitter output line A
P2.10	L13	I/O	PUC	CC60_2	CCU60 input/output of capture/ compare channel 2
		I/O		RXD2A	ASC2 receiver input/output line A
P2.11	G16	O	PUC	COUT60_2	CCU60 output of capture/compare channel 2
		O		TXD2A	ASC2 transmitter output line A
P2.12	K15	I/O	—	SDA0	IIC Serial Data line 0
		I		CTRAP0	CCU60 trap input
		O		SLSO0_3	SSC0 Slave Select output 3

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P2.13	K14	I/O	—	SCL0	IIC clock line 0
		I		CCPOS0_0	CCU60 Hall input signal 0
		O		SLSO1_3	SSC1 Slave Select output 3
P2.14	F16	I	—	CCPOS0_1	CCU60 Hall input signal 1
		I/O		SDA1	IIC Serial Data line 1
		O		SLSO0_4	SSC0 Slave Select output 4
P2.15	E16	I	—	CCPOS0_2	CCU60 Hall input signal 2
		I/O		SCL1	IIC clock line 1
		O		SLSO1_4	SSC1 Slave Select output 4

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P3		I/O		**Port 3** Port 3 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for MLI1, CCU61, SSC0/1 and OCDS Level 2 debug lines.
P3.0	A15	O	PUC	OCDSB_0 OCDS L2 Debug Line B0
		O		COUT61_3 CCU61 compare channel 3 output
P3.1	B15	O	PUC	OCDSB_1 OCDS L2 Debug Line B1
		I/O		CC61_0 CCU61 input/output of capture/ compare channel 0
P3.2	D15	O	PUC	OCDSB_2 OCDS L2 Debug Line B2
		O		COUT61_0 CCU61 output of capture/compare channel 0
P3.3	E15	O	PUC	OCDSB_3 OCDS L2 Debug Line B3
		I/O		CC61_1 CCU61 input/output of capture/ compare channel 1
P3.4	G14	O	PUC	OCDSB_4 OCDS L2 Debug Line B4
		O		COUT61_1 CCU61 output of capture/compare channel 1
P3.5	G15	O	PUC	OCDSB_5 OCDS L2 Debug Line B5
		I/O		CC61_2 CCU61 input/output of capture/ compare channel 2
P3.6	F15	O	PUC	OCDSB_6 OCDS L2 Debug Line B6
		O		COUT61_2 CCU61 output of capture/compare channel 2
P3.7	H14	O	PUC	OCDSB_7 OCDS L2 Debug Line B7
		I		CTRAP1 CCU61 trap input
		O		SLSO0_5 SSC0 Slave Select output 5
P3.8	C15	O	PUC	OCDSB_8 OCDS L2 Debug Line B8
		I		CCPOS1_0 CCU61 Hall input signal 0
		O		TCLK1 MLI1 transmit channel clock output
		O		SLSO1_5 SSC1 Slave Select output 5
P3.9	H15	O	PUC	OCDSB_9 OCDS L2 Debug Line B9
		I		CCPOS1_1 CCU61 Hall input signal 1
		I		TREADY1 MLI1 transmit channel ready input
		O		SLSO0_6 SSC0 Slave Select output 6
P3.10	B16	O	PUC	OCDSB_10 OCDS L2 Debug Line B10
		I		CCPOS1_2 CCU61 Hall input signal 2
		O		TVALID1 MLI1 transmit channel valid output
		O		SLSO1_6 SSC1 Slave Select output 6

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P3.11	C16	O	PUC	OCDSB_11	OCDS L2 Debug Line B11
		O		TDATA1	MLI1 transmit channel data output
		O		SLSO0_7	SSC0 Slave Select output 7
		I		CC61_T12HR	CCU61 Timer 12 hardware run
P3.12	D16	O	PUC	OCDSB_12	OCDS L2 Debug Line B12
		I		RCLK1	MLI1 receive channel clock input
		O		SLSO1_7	SSC1 Slave Select output 7
		I		CC61_T13HR	CCU61 Timer 13 hardware run
P3.13	K13	O	PUC	OCDSB_13	OCDS L2 Debug Line B13
		O		RREADY1	MLI1 receive channel ready output
		I/O		MRST1B	SSC1 master receive/slave transmit input/output B
P3.14	J14	O	PUC	OCDSB_14	OCDS L2 Debug Line B14
		I		RVALID1	MLI1 receive channel valid input
		I/O		MTSR1B	SSC1 master transmit/slave receive input/output B
P3.15	J15	O	PUC	OCDSB_15	OCDS L2 Debug Line B15
		I		RDATA1	MLI1 receive channel data input
		I/O		SCLK1B	SSC1 clock input/output line B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P4		I/O		**Port 4** Port 4 is an 8-bit bi-directional general purpose I/O port which can be alternatively used for USB, MLI0 and SCU.
P4.0	R8	I	PUC	USBCLK 48 MHz input clock
		O		TCLK0B MLI0 transmit channel clock output B
P4.1	R9	I	PUC	RCVI USB data input
		I		TREADY0B MLI0 transmit channel ready input B
P4.2	N7	I	PUC	VPI USB D+ CMOS level mirror of differential signal
		O		TVALID0B MLI0 transmit channel valid output B
P4.3	N6	I	PUC	VMI USB D- CMOS level mirror of differential signal
		O		TDATA0B MLI0 transmit channel data output B
P4.4	P6	O	PUC	VPO USB D+ CMOS level output
		I		RCLK0B MLI0 receive channel clock input B
P4.5	R7	O	PUC	VMO USB D- CMOS level output
		O		RREADY0B MLI0 receive channel ready output B
P4.6	R6	O	PUC	USBOE Direction select for transmit or receive
		I		RVALID0B MLI0 receive channel valid input B
P4.7	P5	I	PUC	RDATA0B MLI0 receive channel data input B
		O		BRKOUT_A OCDS Break Out A
HDRST	N5	I/O	PUA	**Hardware Reset Input/Reset Indication Output** Assertion of this bi-directional open-drain pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for a minimum 4 f_{CPU} clock cycles. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset for a specific period of time. For a software reset, activation of this pin is programmable.
PORST	R5	I	PUC	**Power-on Reset Input** A low level on PORST causes an asynchronous reset of the entire chip. PORST is a fully asynchronous level sensitive signal.
NMI	T7	I	PUC	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes an NMI-Trap request to the CPU.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
$\overline{\text{TRST}}$	T11	I	PDC	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	T12	I	PUC	**JTAG Module Clock Input**
TDI	T13	I	PUC	**JTAG Module Serial Data Input**
TDO	T10	O	—	**JTAG Module Serial Data Output**
TMS	T9	I	PUC	**JTAG Module State Machine Control Input**
$\overline{\text{TRCLK}}$	T8	O	—	**Trace Clock for OCDS_L2 Lines**
HWCFG0 **HWCFG1** **HWCFG2**	M14 L14 T6	I I I	PUC PUC PDC	**Hardware Configuration Inputs** The Configuration Inputs define the boot options of the TC1130 after a hardware invoked reset operation.
$\overline{\text{BRKIN}}$	T5	I	PUC	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
MII_ TXCLK	T2	I	PDC	**Ethernet Controller Transmit Clock** MII_TXD[3:0] and MII_TXEN are driven off the rising edge of the MII_TXCLK by the core and sampled by the PHY on the rising edge of the MII_TXCLK.
MII_ RXCLK	R2	I	PDC	**Ethernet Controller Receive Clock** MII_RXCLK is a continuous clock. Its frequency is 25 MHz for 100 Mbit/sec operation, and 2.5 MHz for 10 Mbit/sec. MII_RXD[3:0], MII_RXDV and MII_EXER are driven by the PHY off the falling edge of MII_RXCLK and sampled on the rising edge of MII_RXCLK.
MII_ MDIO	R1	I/O	PDA	**Ethernet Controller Management Data Input/ Output** When a read command is being executed, the data that is clocked out of the PHY will be presented on the input line. When the Core is clocking control or data onto the MII_MDIO line, the signal will carry the information.
D+	T14	I/O	—	**USB D+ Data Line**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
D-	T15	I/O	—	**USB D- Data Line**
$\overline{CS0}$ **$\overline{CS1}$** **$\overline{CS2}$** **$\overline{CS3}$**	D9 D8 C9 B8	O O O O	PUC PUC PUC PUC	**EBU Chip Select Output Line 0** **EBU Chip Select Output Line 1** **EBU Chip Select Output Line 2** **EBU Chip Select Output Line 3** Each corresponds to a programmable region. Only one can be active at one time.
$\overline{CSCOMB}$	N3	O	PUC	**EBU Chip Select Output for combination function (Overlay Memory and Global)**
SDCLKI	J1	I	—	**SDRAM Clock Input (Clock Feedback)**
SDCLKO	H1	O	—	**SDRAM Clock Output** Accesses to SDRAM devices are synchronized to this clock.
$\overline{RAS}$	D6	O	PUC	**EBU SDRAM Row Address Strobe Output**
$\overline{CAS}$	D5	O	PUC	**EBU SDRAM Column Address Strobe Output**
CKE	L4	O	PUC	**EBU SDRAM Clock Enable Output**
BFCLKI	D1	I	—	**Burst Flash Clock Input (Clock Feedback)**
BFCLKO	E1	O	—	**Burst Flash Clock Output** Accesses to Burst Flash devices are synchronized to this clock.
$\overline{RD}$	P2	O	PUC	**EBU Read Control Line** Output in master mode Input in slave mode
RD/$\overline{WR}$	T3	O	PUC	**EBU Write Control Line** Output in master mode Input in slave mode
$\overline{WAIT}$	B9	I	PUC	**EBU Wait Control Line**
ALE	R3	O	PDC	**EBU Address Latch Enable Output**
MR/$\overline{W}$	P3	O	PUC	**EBU Motorola-style Read/Write Output**
$\overline{BAA}$	A11	O	PUC	**EBU Burst Address Advance Output** For advancing address in a Burst Flash access
$\overline{ADV}$	B11	O	PUC	**EBU Burst Flash Address Valid Output**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address/Data Bus Input/Output Lines
AD0	C8	I/O	PUC	EBU Address/Data Bus Line 0
AD1	C7	I/O	PUC	EBU Address/Data Bus Line 1
AD2	B6	I/O	PUC	EBU Address/Data Bus Line 2
AD3	C6	I/O	PUC	EBU Address/Data Bus Line 3
AD4	C5	I/O	PUC	EBU Address/Data Bus Line 4
AD5	A3	I/O	PUC	EBU Address/Data Bus Line 5
AD6	A2	I/O	PUC	EBU Address/Data Bus Line 6
AD7	C3	I/O	PUC	EBU Address/Data Bus Line 7
AD8	C2	I/O	PUC	EBU Address/Data Bus Line 8
AD9	D2	I/O	PUC	EBU Address/Data Bus Line 9
AD10	F1	I/O	PUC	EBU Address/Data Bus Line 10
AD11	E3	I/O	PUC	EBU Address/Data Bus Line 11
AD12	F3	I/O	PUC	EBU Address/Data Bus Line 12
AD13	G1	I/O	PUC	EBU Address/Data Bus Line 13
AD14	H2	I/O	PUC	EBU Address/Data Bus Line 14
AD15	G3	I/O	PUC	EBU Address/Data Bus Line 15
AD16	D7	I/O	PUC	EBU Address/Data Bus Line 16
AD17	B5	I/O	PUC	EBU Address/Data Bus Line 17
AD18	A4	I/O	PUC	EBU Address/Data Bus Line 18
AD19	B4	I/O	PUC	EBU Address/Data Bus Line 19
AD20	C4	I/O	PUC	EBU Address/Data Bus Line 20
AD21	B3	I/O	PUC	EBU Address/Data Bus Line 21
AD22	B2	I/O	PUC	EBU Address/Data Bus Line 22
AD23	B1	I/O	PUC	EBU Address/Data Bus Line 23
AD24	C1	I/O	PUC	EBU Address/Data Bus Line 24
AD25	D3	I/O	PUC	EBU Address/Data Bus Line 25
AD26	E2	I/O	PUC	EBU Address/Data Bus Line 26
AD27	F2	I/O	PUC	EBU Address/Data Bus Line 27
AD28	F4	I/O	PUC	EBU Address/Data Bus Line 28
AD29	G4	I/O	PUC	EBU Address/Data Bus Line 29
AD30	H3	I/O	PUC	EBU Address/Data Bus Line 30
AD31	G2	I/O	PUC	EBU Address/Data Bus Line 31
$\overline{\text{BC0}}$	A5	O	PUC	**EBU Byte Control Line 0**
$\overline{\text{BC1}}$	A6	O	PUC	**EBU Byte Control Line 1**
$\overline{\text{BC2}}$	B7	O	PUC	**EBU Byte Control Line 2**
BC3	A7	O	PUC	**EBU Byte Control Line 3**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address Bus Input/Output Lines
A0	K1	O	PUC	EBU Address Bus Line 0
A1	L1	O	PUC	EBU Address Bus Line 1
A2	M1	O	PUC	EBU Address Bus Line 2
A3	N1	O	PUC	EBU Address Bus Line 3
A4	P1	O	PUC	EBU Address Bus Line 4
A5	J2	O	PUC	EBU Address Bus Line 5
A6	K2	O	PUC	EBU Address Bus Line 6
A7	L2	O	PUC	EBU Address Bus Line 7
A8	M2	O	PUC	EBU Address Bus Line 8
A9	N2	O	PUC	EBU Address Bus Line 9
A10	J3	O	PUC	EBU Address Bus Line 10
A11	K3	O	PUC	EBU Address Bus Line 11
A12	L3	O	PUC	EBU Address Bus Line 12
A13	M3	O	PUC	EBU Address Bus Line 13
A14	K4	O	PUC	EBU Address Bus Line 14
A15	A8	O	PUC	EBU Address Bus Line 15
A16	A9	O	PUC	EBU Address Bus Line 16
A17	A10	O	PUC	EBU Address Bus Line 17
A18	B10	O	PUC	EBU Address Bus Line 18
A19	C10	O	PUC	EBU Address Bus Line 19
A20	D10	O	PUC	EBU Address Bus Line 20
A21	T4	O	PUC	EBU Address Bus Line 21
A22	R4	O	PUC	EBU Address Bus Line 22
A23	P4	O	PUC	EBU Address Bus Line 23
XTAL1	M16	I	—	**Oscillator/PLL/Clock Generator Input/Output Pins**
XTAL2	N16	O	—	XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking of the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation, XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC3}	P16	—	—	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC3}	R16	—	—	**Main Oscillator Ground**
V_{DDOSC}	L16	—	—	**Main Oscillator Power Supply (1.5 V)**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
V_{SSOSC}	L15	—	—	**Main Oscillator Ground**
V_{DD}	G7 G8 G9 G10 G13 K7,K8 K9 K10	—	—	**Core and Logic Power Supply (1.5 V)**
V_{DDP}	D4 D13 H4 J13 M4 N13	—	—	**Ports Power Supply (3.3 V)**
V_{SS}	E4 E13 H7 H8 H9 H10 H13 J4,J7 J8,J9 J10 M13 N4	—	—	**Ground**
N.C.	A1 A16 T1 T16	—	—	**Not Connected** These pins must not be connected.

1) Refers to internal pull-up or pull-down device connected and corresponding type. The notation '—' indicates that the internal pull-up or pull-down device is not enabled.

Note: P2.12 to P2.15 are always configured as open drain.