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# XC164SM

16-Bit Single-Chip Microcontroller  
with C166SV2 Core

# 16bit

Microcontrollers



Never stop thinking

**Edition 2007-03**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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16-Bit Single-Chip Microcontroller  
with C166SV2 Core

Microcontrollers



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**XC164SM**

**Revision History: V1.2, 2007-03**

Previous Version(s):

V1.1, 2006-08

V1.0, 2005-11

<b>Page</b>	<b>Subjects (major changes since last revision)</b>
<b>6</b>	Design steps of the derivatives differentiated.
<b>50</b>	Power consumption of the derivatives differentiated.
<b>51</b>	Figure 10 adapted.
<b>52</b>	Figure 12 adapted.
<b>62</b>	Packages of the derivatives differentiated.
<b>63</b>	Thermal resistances of the derivatives differentiated.
all	“Preliminary” removed

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## **1 Summary of Features**

For a quick overview or reference, the XC164SM's properties are listed here in a condensed way.

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication ( $16 \times 16$  bit), Background Division ( $32 / 16$  bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with up to 63 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 ... 1:10), or via Prescaler (factors 1:1 ... 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 0/2/4 Kbytes<sup>1)</sup> On-Chip Data SRAM (DSRAM)
  - 2 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 32/64/128<sup>1)</sup> Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 14-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55  $\mu$ s or 2.15  $\mu$ s)
  - 16-Channel General Purpose Capture/Compare Unit (CAPCOM2)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip Real Time Clock, Driven by the Main Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

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1) Depends on the respective derivative. See [Table 1 “XC164SM Derivative Synopsis” on Page 6](#).

---

**Summary of Features**

- Up to 47 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader
- On-Chip Debug Support via JTAG Interface
- 64-Pin Green LQFP Package for the -16F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)
- 64-Pin TQFP Package for the -4F/8F derivatives, 0.5 mm (19.7 mil) pitch (RoHS compliant)

**Ordering Information**

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC164SM please refer to your responsible sales representative or your local distributor.

This document describes several derivatives of the XC164SM group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC164SM** throughout this document.



**Summary of Features**

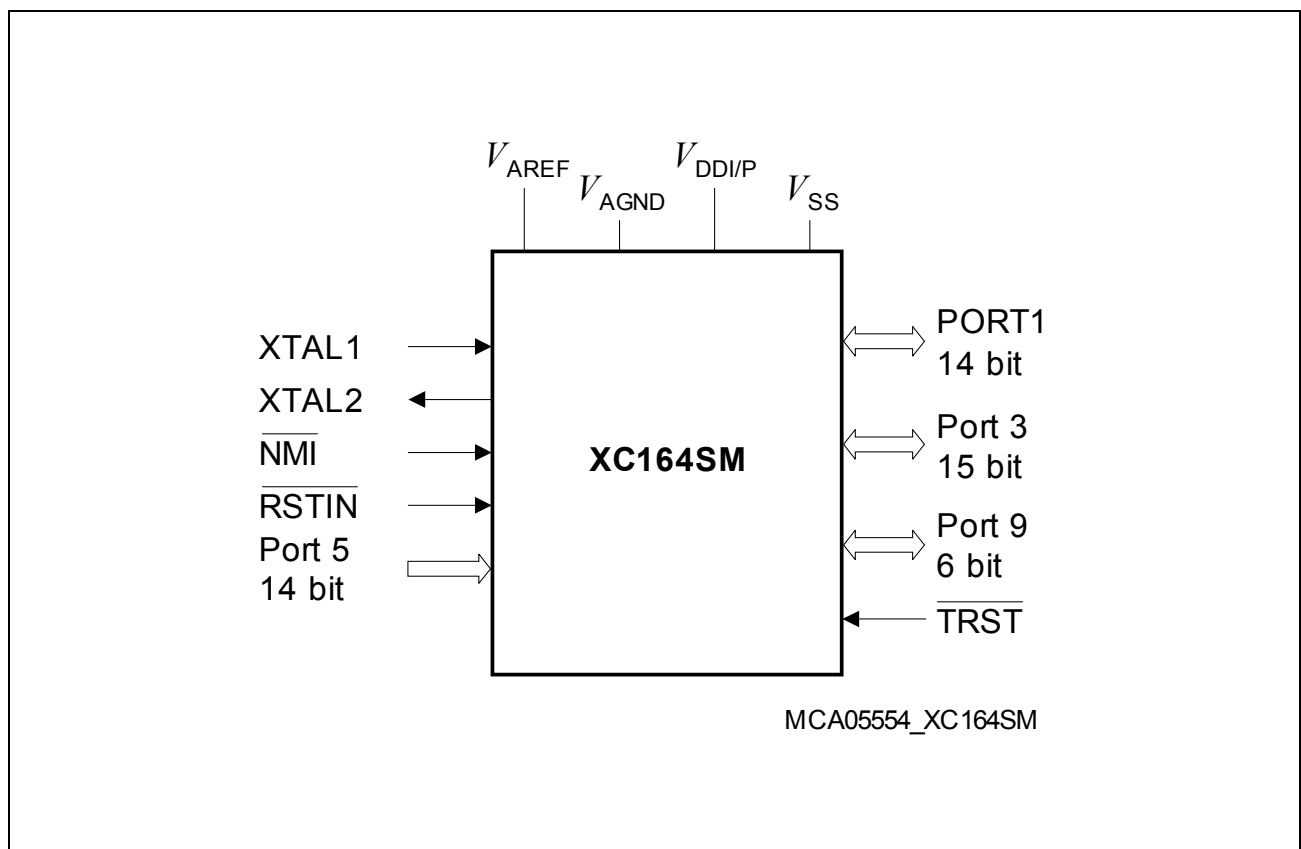
**Table 1 XC164SM Derivative Synopsis**

<b>Derivative<sup>1)</sup></b>	<b>Temp. Range</b>	<b>Program Memory</b>	<b>On-Chip RAM</b>	<b>Interfaces</b>
SAF-XC164SM-16F40F SAF-XC164SM-16F20F	-40 to 85 °C	128 Kbytes Flash	2 Kbytes DPRAM, 4 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1
SAF-XC164SM-8F40F SAF-XC164SM-8F20F	-40 to 85 °C	64 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes DSRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1
SAF-XC164SM-4F40F SAF-XC164SM-4F20F	-40 to 85 °C	32 Kbytes Flash	2 Kbytes DPRAM, 2 Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1

1) This Data Sheet is valid for:  
 devices starting with and including design step BA for the -16F derivatives, and for  
 devices starting with and including design step AA for -4F/8F derivatives.

## 2 General Device Information

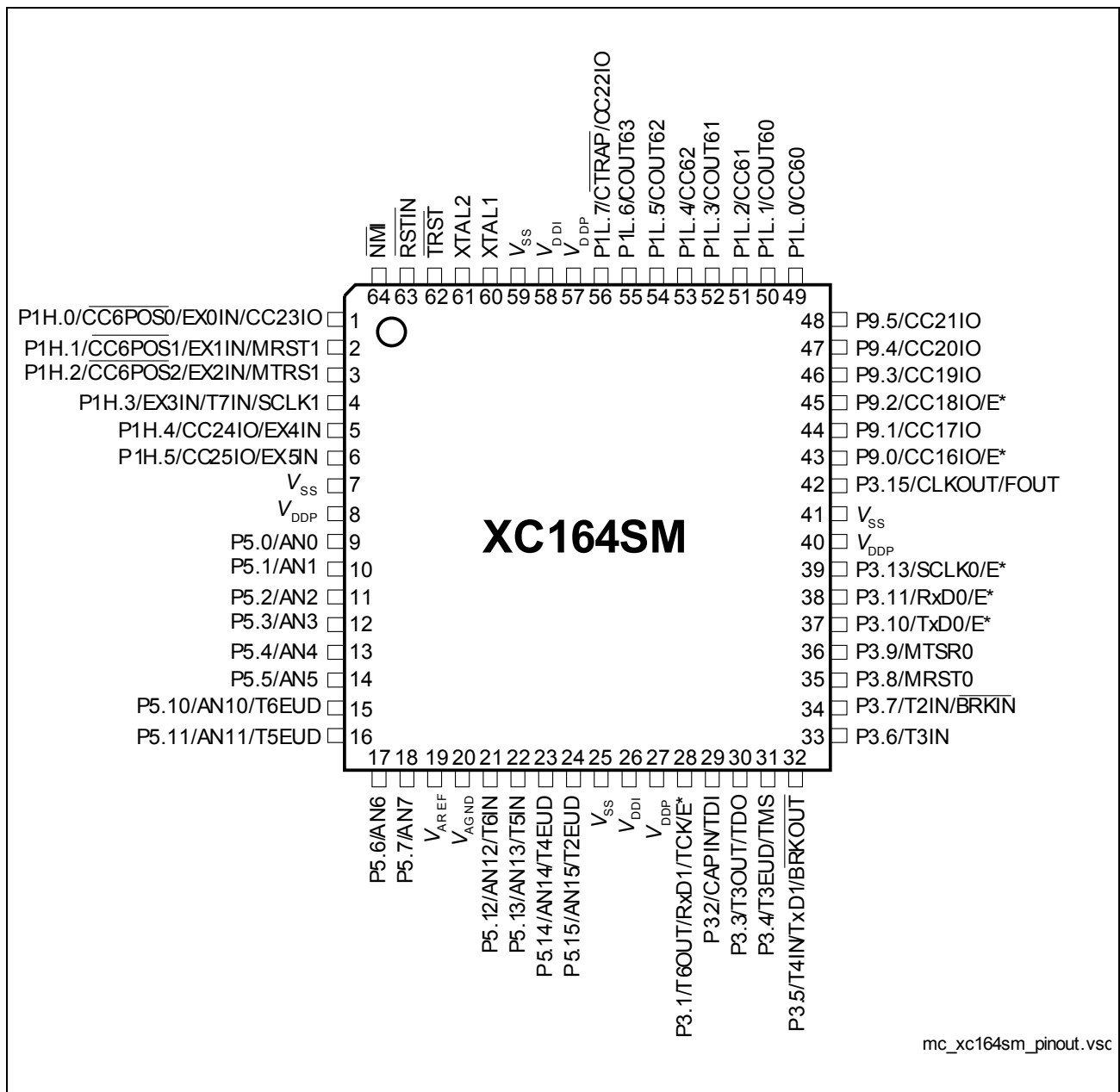
The XC164SM derivatives are high-performance members of the Infineon XC166 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 40 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program Flash, program RAM, and data RAM.



**Figure 1**      **Logic Symbol**

## 2.1 Pin Configuration and Definition

The pins of the XC164SM are described in detail in [Table 2](#), including all their alternate functions. [Figure 2](#) summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E\* marks pins to be used as alternate external interrupt inputs.



**Figure 2 Pin Configuration (top view)**

**Table 2 Pin Definitions and Functions**

<b>Sym- bol</b>	<b>Pin Num.</b>	<b>Input Outp.</b>	<b>Function</b>
$\overline{\text{RSTIN}}$	63	I	<p>Reset Input with Schmitt-Trigger characteristics. A low-level at this pin while the oscillator is running resets the XC164SM. A spike filter suppresses input pulses &lt; 10 ns. Input pulses &gt; 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.</p> <p><i>Note: The reset duration must be sufficient to let the hardware configuration signals settle.</i></p> <p><i>External circuitry must guarantee low-level at the <math>\overline{\text{RSTIN}}</math> pin at least until both power supply voltages have reached the operating range.</i></p>
$\overline{\text{NMI}}$	64	I	<p>Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the <math>\overline{\text{NMI}}</math> pin must be low in order to force the XC164SM into power down mode. If <math>\overline{\text{NMI}}</math> is high, when PWRDN is executed, the part will continue to run in normal mode.</p> <p>If not used, pin NMI should be pulled high externally.</p>
<b>Port 9</b>	43-48	IO	<p>Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:</p>
P9.0	43	I/O	<p>CC16IO: (CAPCOM2) CC16 Capture Inp./Compare Outp., EX5IN: (Fast External Interrupt 5) Input (alternate pin A)</p>
P9.1	44	I/O	<p>CC17IO: (CAPCOM2) CC17 Capture Inp./Compare Outp.,</p>
P9.2	45	I/O	<p>CC18IO: (CAPCOM2) CC18 Capture Inp./Compare Outp., EX4IN: (Fast External Interrupt 4) Input (alternate pin A)</p>
P9.3	46	I/O	<p>CC19IO: (CAPCOM2) CC19 Capture Inp./Compare Outp.,</p>
P9.4	47	I/O	<p>CC20IO: (CAPCOM2) CC20 Capture Inp./Compare Outp.</p>
P9.5	48	I/O	<p>CC21IO: (CAPCOM2) CC21 Capture Inp./Compare Outp.</p> <p><i>Note: At the end of an external reset P9.4 and P9.5 also may input startup configuration values</i></p>

**Table 2 Pin Definitions and Functions (cont'd)**

Symbol	Pin Num.	Input Outp.	Function
<b>Port 5</b>	9-18, 21-24	I	Port 5 is a 14-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	9	I	AN0
P5.1	10	I	AN1
P5.2	11	I	AN2
P5.3	12	I	AN3
P5.4	13	I	AN4
P5.5	14	I	AN5
P5.10	15	I	AN10 (T6EUD): GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	16	I	AN11 (T5EUD): GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.6	17	I	AN6
P5.7	18	I	AN7
P5.12	21	I	AN12 (T6IN): GPT2 Timer T6 Count/Gate Input
P5.13	22	I	AN13 (T5IN): GPT2 Timer T5 Count/Gate Input
P5.14	23	I	AN14 (T4EUD): GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	24	I	AN15 (T2EUD): GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.
<u>TRST</u>	62	I	<u>Test-System Reset Input</u> . For normal system operation, pin <u>TRST</u> should be held low. A high level at this pin at the rising edge of <u>RSTIN</u> enables the hardware configuration and <u>activates</u> the XC164SM's debug system. In this case, pin <u>TRST</u> must be driven low once to reset the debug system.

**General Device Information**

**Table 2 Pin Definitions and Functions (cont'd)**

Symbol	Pin Num.	Input Outp.	Function
<b>Port 3</b>	28-39, 42	IO	Port 3 is a 13-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:
P3.1	28	O I/O I I	T6OUT: [GPT2] Timer T6 Toggle Latch Output, RxD1: [ASC1] Data Input (Async.) or Inp./Outp. (Sync.), EX1IN: [Fast External Interrupt 1] Input (alternate pin A), TCK: [Debug System] JTAG Clock Input
P3.2	29	I I	CAPIN: [GPT2] Register CAPREL Capture Input, TDI: [Debug System] JTAG Data In
P3.3	30	O O	T3OUT: [GPT1] Timer T3 Toggle Latch Output, TDO: [Debug System] JTAG Data Out
P3.4	31	I I	T3EUD: [GPT1] Timer T3 External Up/Down Control Input, TMS: [Debug System] JTAG Test Mode Selection
P3.5	32	I O O	T4IN: [GPT1] Timer T4 Count/Gate/Reload/Capture Inp. TxD1: [ASC0] Clock/Data Output (Async./Sync.), BRKOUT: [Debug System] Break Out
P3.6	33	I	T3IN: [GPT1] Timer T3 Count/Gate Input
P3.7	34	I I	T2IN: [GPT1] Timer T2 Count/Gate/Reload/Capture Inp. BRKIN: [Debug System] Break In
P3.8	35	I/O	MRST0: [SSC0] Master-Receive/Slave-Transmit In/Out.
P3.9	36	I/O	MTSR0: [SSC0] Master-Transmit/Slave-Receive Out/In.
P3.10	37	O I	TxD0: [ASC0] Clock/Data Output (Async./Sync.), EX2IN: [Fast External Interrupt 2] Input (alternate pin B)
P3.11	38	I/O I	RxD0: [ASC0] Data Input (Async.) or Inp./Outp. (Sync.), EX2IN: [Fast External Interrupt 2] Input (alternate pin A)
P3.13	39	I/O I	SCLK0: [SSC0] Master Clock Output / Slave Clock Input., EX3IN: [Fast External Interrupt 3] Input (alternate pin A)
P3.15	42	O O	CLKOUT: System Clock Output (= CPU Clock), FOUT: Programmable Frequency Output

**General Device Information**

**Table 2 Pin Definitions and Functions (cont'd)**

<b>Sym- bol</b>	<b>Pin Num.</b>	<b>Input Outp.</b>	<b>Function</b>
<b>PORT1</b>	1-6, 49-56	IO	PORT1 consists of one 8-bit and one 6-bit bidirectional I/O port P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. The following PORT1 pins also serve for alt. functions:
P1L.0	49	I/O	CC60: [CAPCOM6] Input / Output of Channel 0
P1L.1	50	O	COOUT60: [CAPCOM6] Output of Channel 0
P1L.2	51	I/O	CC61: [CAPCOM6] Input / Output of Channel 1
P1L.3	52	O	COOUT61: [CAPCOM6] Output of Channel 1
P1L.4	53	I/O	CC62: [CAPCOM6] Input / Output of Channel 2
P1L.5	54	O	COOUT62: [CAPCOM6] Output of Channel 2
P1L.6	55	O	COOUT63: Output of 10-bit Compare Channel
P1L.7	56	I	CTR $\overline{A}$ P: [CAPCOM6] Trap Input CTR $\overline{A}$ P is an input pin with an internal pull-up resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
P1H.0	1	I/O	CC22IO: [CAPCOM2] CC22 Capture Inp./Compare Outp.
		I	CC6POS0: [CAPCOM6] Position 0 Input, EX0IN: [Fast External Interrupt 0] Input (default pin),
P1H.1	2	I/O	CC23IO: [CAPCOM2] CC23 Capture Inp./Compare Outp.
		I	CC6POS1: [CAPCOM6] Position 1 Input, EX1IN: [Fast External Interrupt 1] Input (default pin),
P1H.2	3	I/O	MRST1: [SSC1] Master-Receive/Slave-Transmit In/Out.
		I	CC6POS2: [CAPCOM6] Position 2 Input, EX2IN: [Fast External Interrupt 2] Input (default pin),
P1H.3	3	I/O	MTSR1: [SSC1] Master-Transmit/Slave-Receive Out/Inp.
		I	T7IN: [CAPCOM2] Timer T7 Count Input,
P1H.4	5	I/O	SCLK1: [SSC1] Master Clock Output / Slave Clock Input,
		I	EX3IN: [Fast External Interrupt 3] Input (default pin),
P1H.5	6	I/O	CC24IO: [CAPCOM2] CC24 Capture Inp./Compare Outp.,
		I	EX4IN: [Fast External Interrupt 4] Input (default pin)
P1H.5	6	I/O	CC25IO: [CAPCOM2] CC25 Capture Inp./Compare Outp.,
		I	EX5IN: [Fast External Interrupt 5] Input (default pin)
			<i>Note: At the end of an external reset P1H.4 and P1H.5 also may input startup configuration values</i>

**General Device Information**

**Table 2 Pin Definitions and Functions (cont'd)**

<b>Sym- bol</b>	<b>Pin Num.</b>	<b>Input Outp.</b>	<b>Function</b>
XTAL2 XTAL1	61 60	O I	<p>XTAL2: Output of the oscillator amplifier circuit            XTAL1: Input to the oscillator amplifier and input to the internal clock generator            To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.</p> <p><i>Note: Input pin XTAL1 belongs to the core voltage domain. Therefore, input voltages must be within the range defined for <math>V_{DDI}</math>.</i></p>
$V_{AREF}$	19	–	Reference voltage for the A/D converter
$V_{AGND}$	20	–	Reference ground for the A/D converter
$V_{DDI}$	26, 58	–	<p>Digital Core Supply Voltage (On-Chip Modules):            +2.5 V during normal operation and idle mode.            Please refer to the <a href="#">Operating Condition Parameters</a></p>
$V_{DDP}$	8, 27, 40, 57	–	<p>Digital Pad Supply Voltage (Pin Output Drivers):            +5 V during normal operation and idle mode.            Please refer to the <a href="#">Operating Condition Parameters</a></p>
$V_{SS}$	7, 25, 41, 59	–	<p><b>Digital Ground</b>            Connect decoupling capacitors to adjacent <math>V_{DD}/V_{SS}</math> pin pairs as close as possible to the pins.            All <math>V_{SS}</math> pins must be connected to the ground-line or ground-plane.</p>



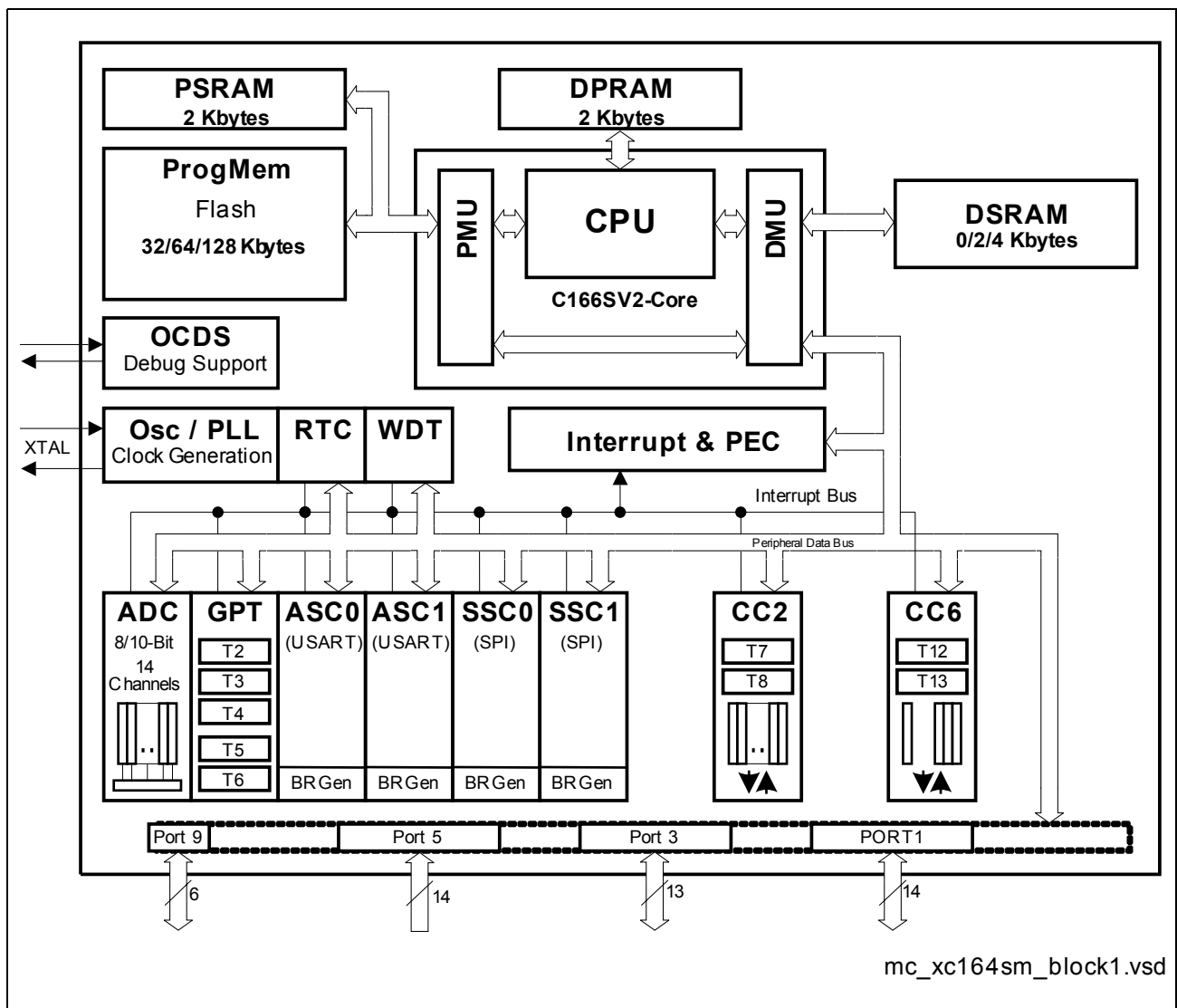
### 3 Functional Description

The architecture of the XC164SM combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources (see [Figure 3](#)).

This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC164SM.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC164SM.



**Figure 3 Block Diagram**

### 3.1 Memory Subsystem and Organization

The memory space of the XC164SM is configured in a von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed byte wise or word wise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM. The system bus allows concurrent two-way communication for maximum transfer performance.

**32/64/128 Kbytes of on-chip Flash memory<sup>1)</sup>** store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors and up to three 32-Kbyte sectors. Each sector can be separately write protected<sup>2)</sup>, erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.

Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

**2 Kbytes of on-chip Program SRAM (PSRAM)** are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

**0/2/4 Kbytes<sup>1)</sup> of on-chip Data SRAM (DSRAM)** are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses. DSRAM is not available in the XC164SM-4F derivatives.

**2 Kbytes of on-chip Dual-Port RAM (DPRAM)** are provided as a storage for user defined variables, for the system stack, general purpose register banks. A register bank

1) Depends on the respective derivative. See [Table 1 “XC164SM Derivative Synopsis” on Page 6](#).

2) Each two 8-Kbyte sectors are combined for write-protection purposes.

**Functional Description**

can consist of up to 16 word wide (R0 to R15) and/or byte wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

**1024 bytes (2 × 512 bytes)** of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

**Table 3 XC164SM Memory Map**

Address Area	Start Loc.	End Loc.	Area Size <sup>1)</sup>	Notes
Flash register space	FF'F000 <sub>H</sub>	FF'FFFF <sub>H</sub>	4 Kbytes	<sup>2)</sup>
Reserved (Acc. trap)	F8'0000 <sub>H</sub>	FF'FFFF <sub>H</sub>	508 Kbytes	–
Reserved for PSRAM	E0'0800 <sub>H</sub>	F7'FFFF <sub>H</sub>	< 1.5 Mbytes	Minus PSRAM
Program SRAM	E0'0000 <sub>H</sub>	E0'07FF <sub>H</sub>	2 Kbytes	–
Reserved for pr. mem.	C2'0000 <sub>H</sub>	DF'FFFF <sub>H</sub>	< 2 Mbytes	Minus Flash
Program Flash	C0'0000 <sub>H</sub>	C1'FFFF <sub>H</sub>	128 Kbytes	XC164SM-16F
	C0'0000 <sub>H</sub>	C0'FFFF <sub>H</sub>	64 Kbytes	XC164SM-8F
	C0'0000 <sub>H</sub>	C0'7FFF <sub>H</sub>	32 Kbytes	XC164SM-4F
Reserved	20'0000 <sub>H</sub>	BF'FFFF <sub>H</sub>	< 10 Mbytes	
Reserved	01'0000 <sub>H</sub>	1F'FFFF <sub>H</sub>	< 2 Mbytes	Minus segment 0
SFR area	00'FE00 <sub>H</sub>	00'FFFF <sub>H</sub>	0.5 Kbyte	–
Dual-Port RAM	00'F600 <sub>H</sub>	00'FDFF <sub>H</sub>	2 Kbytes	–
Reserved for DPRAM	00'F200 <sub>H</sub>	00'F5FF <sub>H</sub>	1 Kbyte	–
ESFR area	00'F000 <sub>H</sub>	00'F1FF <sub>H</sub>	0.5 Kbyte	–
XSFR area	00'E000 <sub>H</sub>	00'EFFF <sub>H</sub>	4 Kbytes	–
Reserved	00'D000 <sub>H</sub>	00'DFFF <sub>H</sub>	6 Kbytes	–
Data SRAM	00'C000 <sub>H</sub>	00'CFFF <sub>H</sub>	4 Kbytes	<sup>3)</sup>
Reserved for DSRAM	00'8000 <sub>H</sub>	00'BFFF <sub>H</sub>	16 Kbytes	–
Reserved	00'0000 <sub>H</sub>	00'7FFF <sub>H</sub>	32 Kbytes	–

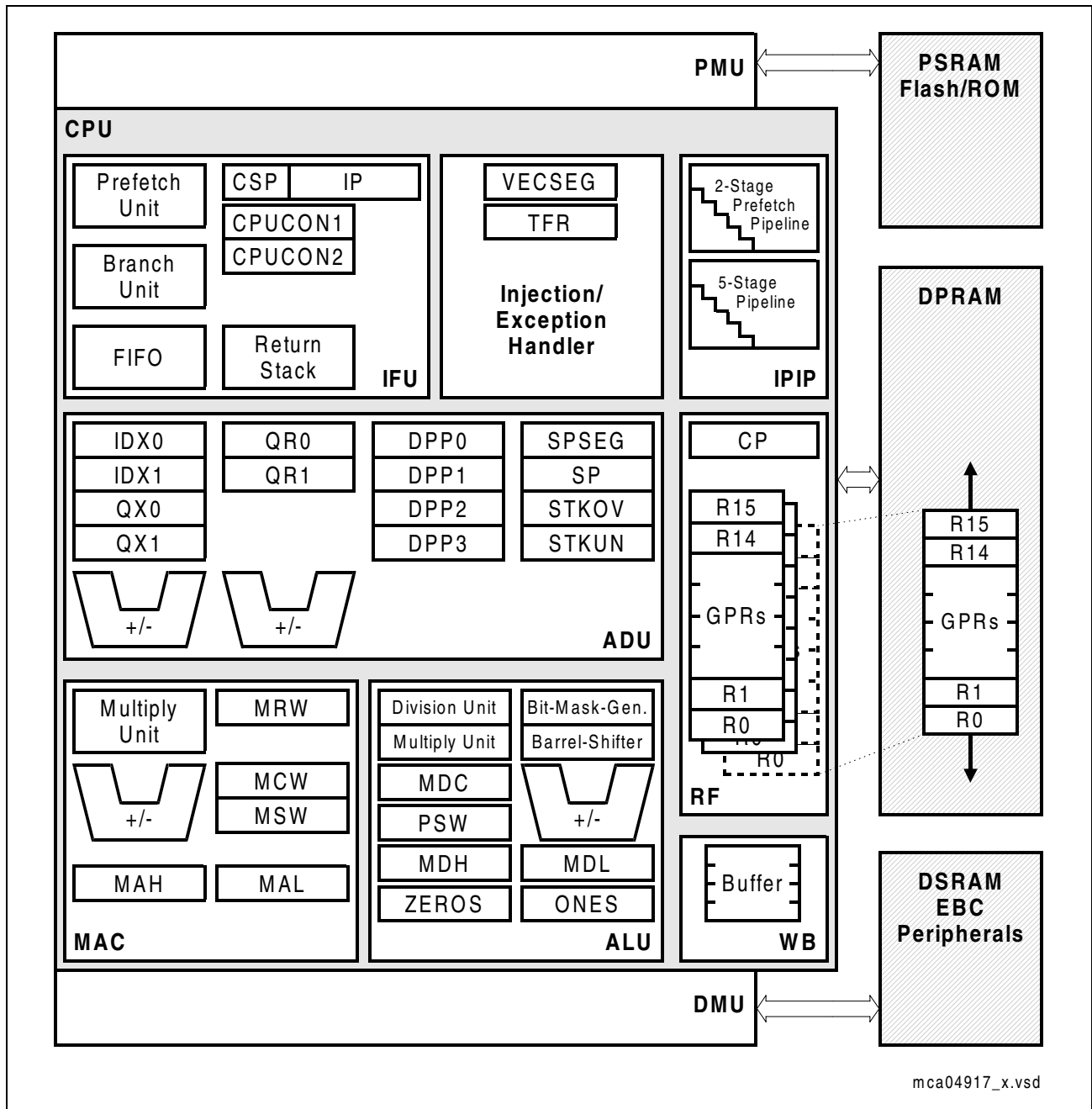
1) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

2) Not defined register locations return a trap code (1E9B<sub>H</sub>).

3) Depends on the respective derivative. See [Table 1 "XC164SM Derivative Synopsis" on Page 6](#).

### 3.2 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.



**Figure 4 CPU Block Diagram**

Based on these hardware provisions, most of the XC164SM's instructions can be executed in just one machine cycle which requires 25 ns at 40 MHz CPU clock. For

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**Functional Description**

example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a 32-/16-bit division is started within 4 cycles, while the remaining 15 cycles are executed in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164SM instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

### 3.3 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164SM is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164SM supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164SM has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

**Table 4** shows all of the possible XC164SM interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

*Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).*

**Functional Description**
**Table 4 XC164SM Interrupt Nodes**

Source of Interrupt or PEC Service Request	Control Register	Vector Location <sup>1)</sup>	Trap Number
EX0IN	CC1_CC8IC	xx'0060 <sub>H</sub>	18 <sub>H</sub> / 24 <sub>D</sub>
EX1IN	CC1_CC9IC	xx'0064 <sub>H</sub>	19 <sub>H</sub> / 25 <sub>D</sub>
EX2IN	CC1_CC10IC	xx'0068 <sub>H</sub>	1A <sub>H</sub> / 26 <sub>D</sub>
EX3IN	CC1_CC11IC	xx'006C <sub>H</sub>	1B <sub>H</sub> / 27 <sub>D</sub>
EX4IN	CC1_CC12IC	xx'0070 <sub>H</sub>	1C <sub>H</sub> / 28 <sub>D</sub>
EX5IN	CC1_CC13IC	xx'0074 <sub>H</sub>	1D <sub>H</sub> / 29 <sub>D</sub>
CAPCOM Register 16	CC2_CC16IC	xx'00C0 <sub>H</sub>	30 <sub>H</sub> / 48 <sub>D</sub>
CAPCOM Register 17	CC2_CC17IC	xx'00C4 <sub>H</sub>	31 <sub>H</sub> / 49 <sub>D</sub>
CAPCOM Register 18	CC2_CC18IC	xx'00C8 <sub>H</sub>	32 <sub>H</sub> / 50 <sub>D</sub>
CAPCOM Register 19	CC2_CC19IC	xx'00CC <sub>H</sub>	33 <sub>H</sub> / 51 <sub>D</sub>
CAPCOM Register 20	CC2_CC20IC	xx'00D0 <sub>H</sub>	34 <sub>H</sub> / 52 <sub>D</sub>
CAPCOM Register 21	CC2_CC21IC	xx'00D4 <sub>H</sub>	35 <sub>H</sub> / 53 <sub>D</sub>
CAPCOM Register 22	CC2_CC22IC	xx'00D8 <sub>H</sub>	36 <sub>H</sub> / 54 <sub>D</sub>
CAPCOM Register 23	CC2_CC23IC	xx'00DC <sub>H</sub>	37 <sub>H</sub> / 55 <sub>D</sub>
CAPCOM Register 24	CC2_CC24IC	xx'00E0 <sub>H</sub>	38 <sub>H</sub> / 56 <sub>D</sub>
CAPCOM Register 25	CC2_CC25IC	xx'00E4 <sub>H</sub>	39 <sub>H</sub> / 57 <sub>D</sub>
CAPCOM Register 26	CC2_CC26IC	xx'00E8 <sub>H</sub>	3A <sub>H</sub> / 58 <sub>D</sub>
CAPCOM Register 27	CC2_CC27IC	xx'00EC <sub>H</sub>	3B <sub>H</sub> / 59 <sub>D</sub>
CAPCOM Register 28	CC2_CC28IC	xx'00F0 <sub>H</sub>	3C <sub>H</sub> / 60 <sub>D</sub>
CAPCOM Register 29	CC2_CC29IC	xx'0110 <sub>H</sub>	44 <sub>H</sub> / 68 <sub>D</sub>
CAPCOM Register 30	CC2_CC30IC	xx'0114 <sub>H</sub>	45 <sub>H</sub> / 69 <sub>D</sub>
CAPCOM Register 31	CC2_CC31IC	xx'0118 <sub>H</sub>	46 <sub>H</sub> / 70 <sub>D</sub>
CAPCOM Timer 7	CC2_T7IC	xx'00F4 <sub>H</sub>	3D <sub>H</sub> / 61 <sub>D</sub>
CAPCOM Timer 8	CC2_T8IC	xx'00F8 <sub>H</sub>	3E <sub>H</sub> / 62 <sub>D</sub>
GPT1 Timer 2	GPT12E_T2IC	xx'0088 <sub>H</sub>	22 <sub>H</sub> / 34 <sub>D</sub>
GPT1 Timer 3	GPT12E_T3IC	xx'008C <sub>H</sub>	23 <sub>H</sub> / 35 <sub>D</sub>
GPT1 Timer 4	GPT12E_T4IC	xx'0090 <sub>H</sub>	24 <sub>H</sub> / 36 <sub>D</sub>
GPT2 Timer 5	GPT12E_T5IC	xx'0094 <sub>H</sub>	25 <sub>H</sub> / 37 <sub>D</sub>
GPT2 Timer 6	GPT12E_T6IC	xx'0098 <sub>H</sub>	26 <sub>H</sub> / 38 <sub>D</sub>

**Functional Description**
**Table 4 XC164SM Interrupt Nodes (cont'd)**

Source of Interrupt or PEC Service Request	Control Register	Vector Location <sup>1)</sup>	Trap Number
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C <sub>H</sub>	27 <sub>H</sub> / 39 <sub>D</sub>
A/D Conversion Complete	ADC_CIC	xx'00A0 <sub>H</sub>	28 <sub>H</sub> / 40 <sub>D</sub>
A/D Overrun Error	ADC_EIC	xx'00A4 <sub>H</sub>	29 <sub>H</sub> / 41 <sub>D</sub>
ASC0 Transmit	ASC0_TIC	xx'00A8 <sub>H</sub>	2A <sub>H</sub> / 42 <sub>D</sub>
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C <sub>H</sub>	47 <sub>H</sub> / 71 <sub>D</sub>
ASC0 Receive	ASC0_RIC	xx'00AC <sub>H</sub>	2B <sub>H</sub> / 43 <sub>D</sub>
ASC0 Error	ASC0_EIC	xx'00B0 <sub>H</sub>	2C <sub>H</sub> / 44 <sub>D</sub>
ASC0 Autobaud	ASC0_ABIC	xx'017C <sub>H</sub>	5F <sub>H</sub> / 95 <sub>D</sub>
SSC0 Transmit	SSC0_TIC	xx'00B4 <sub>H</sub>	2D <sub>H</sub> / 45 <sub>D</sub>
SSC0 Receive	SSC0_RIC	xx'00B8 <sub>H</sub>	2E <sub>H</sub> / 46 <sub>D</sub>
SSC0 Error	SSC0_EIC	xx'00BC <sub>H</sub>	2F <sub>H</sub> / 47 <sub>D</sub>
PLL/OWD	PLLIC	xx'010C <sub>H</sub>	43 <sub>H</sub> / 67 <sub>D</sub>
ASC1 Transmit	ASC1_TIC	xx'0120 <sub>H</sub>	48 <sub>H</sub> / 72 <sub>D</sub>
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178 <sub>H</sub>	5E <sub>H</sub> / 94 <sub>D</sub>
ASC1 Receive	ASC1_RIC	xx'0124 <sub>H</sub>	49 <sub>H</sub> / 73 <sub>D</sub>
ASC1 Error	ASC1_EIC	xx'0128 <sub>H</sub>	4A <sub>H</sub> / 74 <sub>D</sub>
ASC1 Autobaud	ASC1_ABIC	xx'0108 <sub>H</sub>	42 <sub>H</sub> / 66 <sub>D</sub>
End of PEC Subchannel	EOPIC	xx'0130 <sub>H</sub>	4C <sub>H</sub> / 76 <sub>D</sub>
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134 <sub>H</sub>	4D <sub>H</sub> / 77 <sub>D</sub>
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138 <sub>H</sub>	4E <sub>H</sub> / 78 <sub>D</sub>
CAPCOM6 Emergency	CCU6_EIC	xx'013C <sub>H</sub>	4F <sub>H</sub> / 79 <sub>D</sub>
CAPCOM6	CCU6_IC	xx'0140 <sub>H</sub>	50 <sub>H</sub> / 80 <sub>D</sub>
SSC1 Transmit	SSC1_TIC	xx'0144 <sub>H</sub>	51 <sub>H</sub> / 81 <sub>D</sub>
SSC1 Receive	SSC1_RIC	xx'0148 <sub>H</sub>	52 <sub>H</sub> / 82 <sub>D</sub>
SSC1 Error	SSC1_EIC	xx'014C <sub>H</sub>	53 <sub>H</sub> / 83 <sub>D</sub>
RTC	RTC_IC	xx'0174 <sub>H</sub>	5D <sub>H</sub> / 93 <sub>D</sub>
Unassigned node	–	xx'0040 <sub>H</sub>	10 <sub>H</sub> / 16 <sub>D</sub>
Unassigned node	–	xx'0044 <sub>H</sub>	11 <sub>H</sub> / 17 <sub>D</sub>
Unassigned node	–	xx'0048 <sub>H</sub>	12 <sub>H</sub> / 18 <sub>D</sub>
Unassigned node	–	xx'004C <sub>H</sub>	13 <sub>H</sub> / 19 <sub>D</sub>



**Functional Description**
**Table 4 XC164SM Interrupt Nodes (cont'd)**

Source of Interrupt or PEC Service Request	Control Register	Vector Location <sup>1)</sup>	Trap Number
Unassigned node	–	xx'0050 <sub>H</sub>	14 <sub>H</sub> / 20 <sub>D</sub>
Unassigned node	–	xx'0054 <sub>H</sub>	15 <sub>H</sub> / 21 <sub>D</sub>
Unassigned node	–	xx'0058 <sub>H</sub>	16 <sub>H</sub> / 22 <sub>D</sub>
Unassigned node	–	xx'005C <sub>H</sub>	17 <sub>H</sub> / 23 <sub>D</sub>
Unassigned node	–	xx'0078 <sub>H</sub>	1E <sub>H</sub> / 30 <sub>D</sub>
Unassigned node	–	xx'007C <sub>H</sub>	1F <sub>H</sub> / 31 <sub>D</sub>
Unassigned node	–	xx'0080 <sub>H</sub>	20 <sub>H</sub> / 32 <sub>D</sub>
Unassigned node	–	xx'0084 <sub>H</sub>	21 <sub>H</sub> / 33 <sub>D</sub>
Unassigned node	–	xx'00FC <sub>H</sub>	3F <sub>H</sub> / 63 <sub>D</sub>
Unassigned node	–	xx'0100 <sub>H</sub>	40 <sub>H</sub> / 64 <sub>D</sub>
Unassigned node	–	xx'0104 <sub>H</sub>	41 <sub>H</sub> / 65 <sub>D</sub>
Unassigned node	–	xx'012C <sub>H</sub>	4B <sub>H</sub> / 75 <sub>D</sub>
Unassigned node	–	xx'0150 <sub>H</sub>	54 <sub>H</sub> / 84 <sub>D</sub>
Unassigned node	–	xx'0154 <sub>H</sub>	55 <sub>H</sub> / 85 <sub>D</sub>
Unassigned node	–	xx'0158 <sub>H</sub>	56 <sub>H</sub> / 86 <sub>D</sub>
Unassigned node	–	xx'015C <sub>H</sub>	57 <sub>H</sub> / 87 <sub>D</sub>
Unassigned node	–	xx'0160 <sub>H</sub>	58 <sub>H</sub> / 88 <sub>D</sub>
Unassigned node	–	xx'0164 <sub>H</sub>	59 <sub>H</sub> / 89 <sub>D</sub>
Unassigned node	–	xx'0168 <sub>H</sub>	5A <sub>H</sub> / 90 <sub>D</sub>
Unassigned node	–	xx'016C <sub>H</sub>	5B <sub>H</sub> / 91 <sub>D</sub>
Unassigned node	–	xx'0170 <sub>H</sub>	5C <sub>H</sub> / 92 <sub>D</sub>

- 1) Register VECSEG defines the segment where the vector table is located to. Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

**Functional Description**

The XC164SM also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

**Table 5** shows all of the possible exceptions or error conditions that can arise during run-time:

**Table 5 Hardware Trap Summary**

Exception Condition	Trap Flag	Trap Vector	Vector Location <sup>1)</sup>	Trap Number	Trap Priority
Reset Functions: • Hardware Reset • Software Reset • W-dog Timer Overflow	–	RESET RESET RESET	xx'0000 <sub>H</sub> xx'0000 <sub>H</sub> xx'0000 <sub>H</sub>	00 <sub>H</sub> 00 <sub>H</sub> 00 <sub>H</sub>	III III III
Class A Hardware Traps: • Non-Maskable Interrupt • Stack Overflow • Stack Underflow • Software Break	NMI STKOF STKUF SOFTBRK	NMITRAP STOTRAP STUTRAP SBRKTRAP	xx'0008 <sub>H</sub> xx'0010 <sub>H</sub> xx'0018 <sub>H</sub> xx'0020 <sub>H</sub>	02 <sub>H</sub> 04 <sub>H</sub> 06 <sub>H</sub> 08 <sub>H</sub>	II II II II
Class B Hardware Traps: • Undefined Opcode • PMI Access Error • Protected Instruction Fault • Illegal Word Operand Access	UNDOPC PACER PRTFLT ILLOPA	BTRAP BTRAP BTRAP BTRAP	xx'0028 <sub>H</sub> xx'0028 <sub>H</sub> xx'0028 <sub>H</sub> xx'0028 <sub>H</sub>	0A <sub>H</sub> 0A <sub>H</sub> 0A <sub>H</sub> 0A <sub>H</sub>	I I I I
Reserved	–	–	[2C <sub>H</sub> - 3C <sub>H</sub> ]	[0B <sub>H</sub> - 0F <sub>H</sub> ]	–
Software Traps • TRAP Instruction	–	–	Any [xx'0000 <sub>H</sub> - xx'01FC <sub>H</sub> ] in steps of 4 <sub>H</sub>	Any [00 <sub>H</sub> - 7F <sub>H</sub> ]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.  
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.