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XC2387

16/32-Bit Single-Chip Microcontroller with
32-Bit Performance

Microcontrollers



Never stop thinking

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16/32-Bit Single-Chip Microcontroller with
32-Bit Performance

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XC2387

Revision History: V2.1, 2008-08

Previous Version(s):

V2.0, 2007-12

V0.1, 2007-06, Preliminary

Page	Subjects (major changes since last revision)
several	Maximum frequency changed to 80 MHz
31	Voltage domain for XTAL1/XTAL2 corrected to M
71	Coupling factors corrected
76, 78	Improved leakage parameters
77, 79	Pin leakage formula corrected
84	Improved ADC error values
97f	Improved definition of external clock parameters
113	JTAG clock speed corrected

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Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



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1 Summary of Features

For a quick overview and easy reference, the features of the XC2387 are summarized here.

- High-performance CPU with five-stage pipeline
 - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16×16 bit)
 - Background division ($32 / 16$ bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1024 Bytes on-chip special function register area (C166 Family compatible)
- Interrupt system with 16 priority levels for up to 87 sources
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- On-chip memory modules
 - 1 Kbyte on-chip stand-by RAM (SBRAM)
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - 16 Kbytes on-chip data SRAM (DSRAM)
 - 32 Kbytes on-chip program/data SRAM (PSRAM)
 - 576 Kbytes on-chip program memory (Flash memory)
- On-Chip Peripheral Modules
 - Two Synchronizable A/D Converters with up to 24 channels, 10-bit resolution, conversion time below 1 μ s, optional data preprocessing (data reduction, range check)
 - 16-channel general purpose capture/compare unit (CAPCOM2)
 - Four capture/compare units for flexible PWM signal generation (CCU6x)
 - Multi-functional general purpose timer unit with 5 timers

Summary of Features

- Six serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI/QSPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with 64 message objects (Full CAN/Basic CAN) on 3 CAN nodes and gateway functionality
- On-chip real time clock
- Up to 12 Mbytes external address space for code and data
 - Programmable external bus characteristics for different address ranges
 - Multiplexed or demultiplexed external address/data buses
 - Selectable address bus width
 - 16-bit or 8-bit data bus width
 - Five programmable chip-select signals
 - Hold- and hold-acknowledge bus arbitration support
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 118 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via JTAG interface
- 144-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For ordering codes for the XC2387 please contact your sales representative or local distributor.

This document describes several derivatives of the XC2387 group. **Table 1** lists these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity the term **XC2387** is used for all derivatives throughout this document.

Summary of Features

Table 1 XC2387 Derivative Synopsis

Derivative ¹⁾	Temp. Range	Program Memory ²⁾	PSRAM ³⁾	CCU6 Mod.	ADC ⁴⁾ Chan.	Interfaces ⁴⁾
SAK-XC2387-72FxxL	-40 °C to 125 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	3 CAN Nodes, 6 Serial Chan.
SAF-XC2387-72FxxL	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1, 2, 3	16 + 8	3 CAN Nodes, 6 Serial Chan.

- 1) This Data Sheet is valid for devices starting with and including design step AC.
- 2) Specific information about the on-chip Flash memory in [Table 2](#).
- 3) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM.
- 4) Specific information about the available channels in [Table 3](#).
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

The XC2387 types are offered with several Flash memory sizes. [Table 2](#) describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A ¹⁾	Flash Area B	Flash Area C
576 Kbytes	C0'0000 _H ... C0'FFFF _H	C1'0000 _H ... C8'FFFF _H	n.a.

- 1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XC2387 types are offered with different interface options. [Table 3](#) lists the available channels for each option.

Table 3 Interface Channel Association

Total Number	Available Channels
16 ADC0 channels	CH0 ... CH15
8 ADC1 channels	CH0 ... CH7
3 CAN nodes	CAN0, CAN1, CAN2
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

2 General Device Information

The XC2387 derivatives are high-performance members of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 66 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

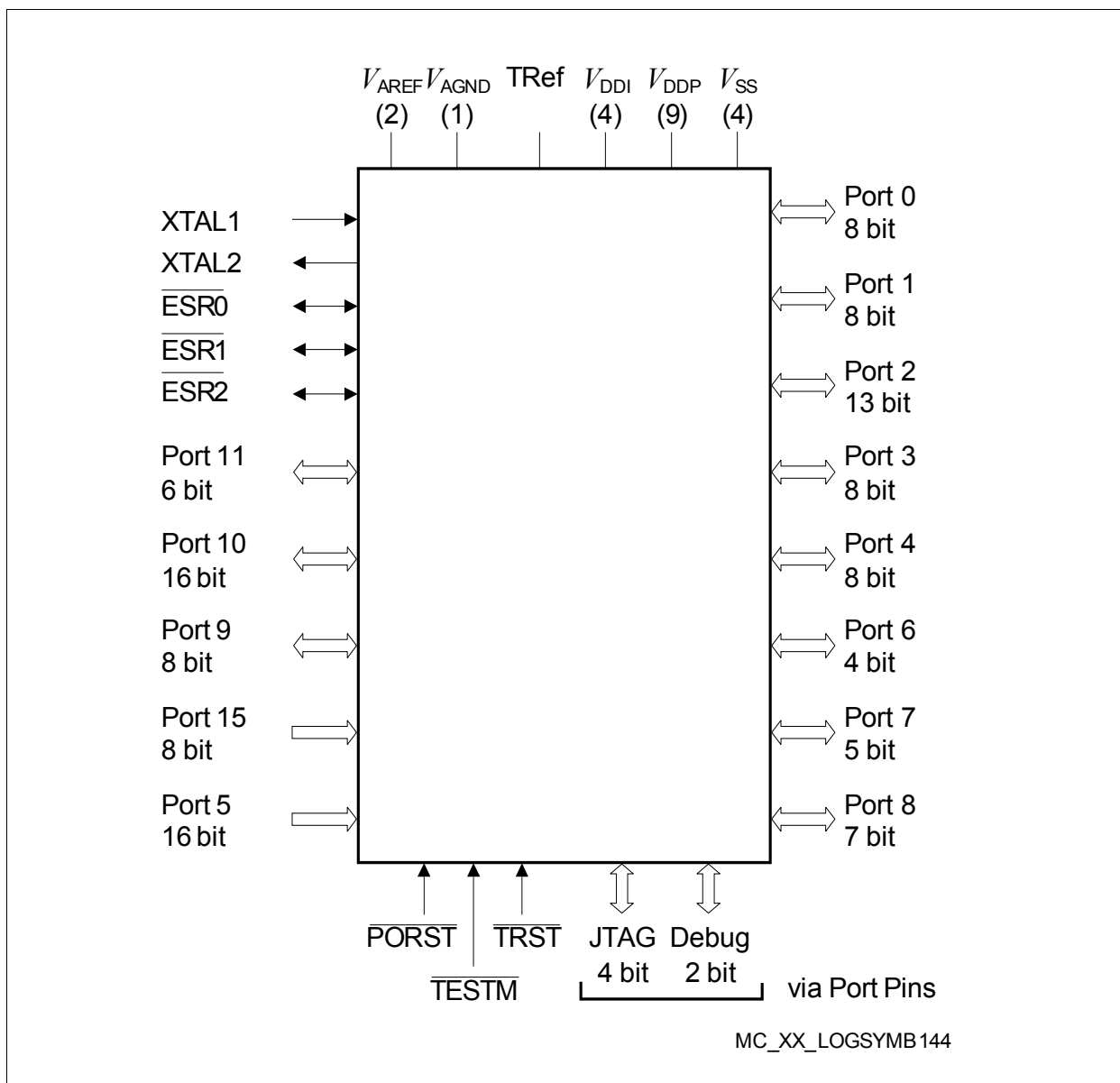


Figure 1 Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC2387 are described in detail in [Table 4](#), which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. [Figure 2](#) summarizes all pins, showing their locations on the four sides of the package.

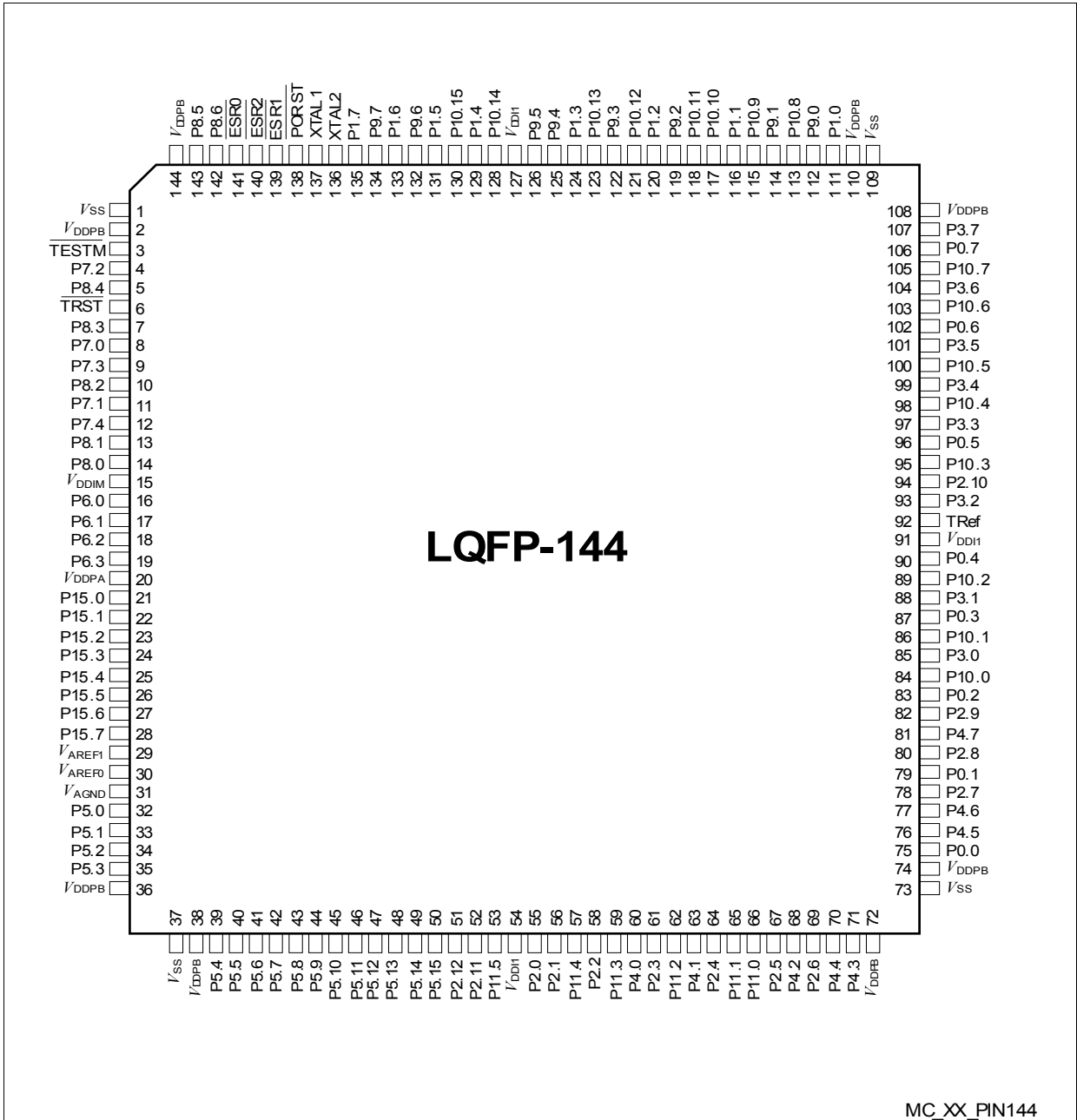


Figure 2 Pin Configuration (top view)

Notes to Pin Definitions

1. **Ctrl.:** The output signal for a port pin is selected by bitfield PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00_B, output O1 is selected by 1x01_B, etc.
Output signal OH is controlled by hardware.
2. **Type:** Indicates the pad type used (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).

Table 4 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pullup device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	CCU62_ CCPOS0A	I	St/B	CCU62 Position Input 0
	TDI_C	I	St/B	JTAG Test Data Input
5	P8.4	O0 / I	St/B	Bit 4 of Port 8, General Purpose Input/Output
	CCU60_ COUT61	O1	St/B	CCU60 Channel 1 Output
	TMS_D	I	St/B	JTAG Test Mode Selection Input
6	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of PORST activates the XC2387's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pulldown device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	Bit 3 of Port 8, General Purpose Input/Output
	CCU60_ COUT60	O1	St/B	CCU60 Channel 0 Output
	TDI_D	I	St/B	JTAG Test Data Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT1 Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT2 Timer T6 Toggle Latch Output
	TDO_A	OH	St/B	JTAG Test Data Output
	ESR2_1	I	St/B	ESR2 Trigger Input 1
9	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_ CCPOS1A	I	St/B	CCU62 Position Input 1
	TMS_C	I	St/B	JTAG Test Mode Selection Input
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
10	P8.2	O0 / I	St/B	Bit 2 of Port 8, General Purpose Input/Output
	CCU60_ CC62	O1 / I	St/B	CCU60 Channel 2 Input/Output
11	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	CCU62_ CTRAPA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input
12	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_ SCLKOUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	CCU62_ CCPOS2A	I	St/B	CCU62 Position Input 2
	TCK_C	I	St/B	JTAG Clock Input
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P8.1	O0 / I	St/B	Bit 1 of Port 8, General Purpose Input/Output
	CCU60_ CC61	O1 / I	St/B	CCU60 Channel 1 Input/Output
14	P8.0	O0 / I	St/B	Bit 0 of Port 8, General Purpose Input/Output
	CCU60_ CC60	O1 / I	St/B	CCU60 Channel 0 Input/Output
16	P6.0	O0 / I	St/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	St/A	External Analog MUX Control Output 0 (ADC0)
	BRKOUT	O3	St/A	OCDS Break Signal Output
	ADCx_ REQGTYC	I	St/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	St/A	USIC1 Channel 1 Shift Data Input
17	P6.1	O0 / I	St/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	St/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	St/A	GPT1 Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	St/A	USIC1 Channel 1 Shift Data Output
	ADCx_ REQTRYC	I	St/A	External Request Trigger Input for ADC0/1
18	P6.2	O0 / I	St/A	Bit 2 of Port 6, General Purpose Input/Output
	EMUX2	O1	St/A	External Analog MUX Control Output 2 (ADC0)
	T6OUT	O2	St/A	GPT2 Timer T6 Toggle Latch Output
	U1C1_ SCLKOUT	O3	St/A	USIC1 Channel 1 Shift Clock Output
	U1C1_DX1C	I	St/A	USIC1 Channel 1 Shift Clock Input
19	P6.3	O0 / I	St/A	Bit 3 of Port 6, General Purpose Input/Output
	T3OUT	O2	St/A	GPT1 Timer T3 Toggle Latch Output
	U1C1_ SELO0	O3	St/A	USIC1 Channel 1 Select/Control 0 Output
	U1C1_DX2D	I	St/A	USIC1 Channel 1 Shift Control Input
	ADCx_ REQTRYD	I	St/A	External Request Trigger Input for ADC0/1

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
21	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
22	P15.1	I	In/A	Bit 1 of Port 15, General Purpose Input
	ADC1_CH1	I	In/A	Analog Input Channel 1 for ADC1
23	P15.2	I	In/A	Bit 2 of Port 15, General Purpose Input
	ADC1_CH2	I	In/A	Analog Input Channel 2 for ADC1
	T5IN	I	In/A	GPT2 Timer T5 Count/Gate Input
24	P15.3	I	In/A	Bit 3 of Port 15, General Purpose Input
	ADC1_CH3	I	In/A	Analog Input Channel 3 for ADC1
	T5EUD	I	In/A	GPT2 Timer T5 External Up/Down Control Input
25	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6IN	I	In/A	GPT2 Timer T6 Count/Gate Input
26	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUD	I	In/A	GPT2 Timer T6 External Up/Down Control Input
27	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1
28	P15.7	I	In/A	Bit 7 of Port 15, General Purpose Input
	ADC1_CH7	I	In/A	Analog Input Channel 7 for ADC1
29	V_{AREF1}	-	PS/A	Reference Voltage for A/D Converter ADC1
30	V_{AREF0}	-	PS/A	Reference Voltage for A/D Converter ADC0
31	V_{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
32	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
33	P5.1	I	In/A	Bit 1 of Port 5, General Purpose Input
	ADC0_CH1	I	In/A	Analog Input Channel 1 for ADC0
34	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
35	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3IN	I	In/A	GPT1 Timer T3 Count/Gate Input
39	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	CCU63_T12HRB	I	In/A	External Run Control Input for T12 of CCU63
	T3EUD	I	In/A	GPT1 Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
40	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12HRB	I	In/A	External Run Control Input for T12 of CCU60
41	P5.6	I	In/A	Bit 6 of Port 5, General Purpose Input
	ADC0_CH6	I	In/A	Analog Input Channel 6 for ADC0
42	P5.7	I	In/A	Bit 7 of Port 5, General Purpose Input
	ADC0_CH7	I	In/A	Analog Input Channel 7 for ADC0
43	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	CCU6x_T12HRC	I	In/A	External Run Control Input for T12 of CCU6x
	CCU6x_T13HRC	I	In/A	External Run Control Input for T13 of CCU6x
44	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input
45	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	BRKIN_A	I	In/A	OCDS Break Signal Input
46	P5.11	I	In/A	Bit 11 of Port 5, General Purpose Input
	ADC0_CH11	I	In/A	Analog Input Channel 11 for ADC0

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P5.12	I	In/A	Bit 12 of Port 5, General Purpose Input
	ADC0_CH12	I	In/A	Analog Input Channel 12 for ADC0
48	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
	EX0BINB	I	In/A	External Interrupt Trigger Input
49	P5.14	I	In/A	Bit 14 of Port 5, General Purpose Input
	ADC0_CH14	I	In/A	Analog Input Channel 14 for ADC0
50	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
51	P2.12	O0 / I	St/B	Bit 12 of Port 2, General Purpose Input/Output
	U0C0_SELO4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_SELO3	O2	St/B	USIC0 Channel 1 Select/Control 3 Output
	READY	I	St/B	External Bus Interface READY Input
52	P2.11	O0 / I	St/B	Bit 11 of Port 2, General Purpose Input/Output
	U0C0_SELO2	O1	St/B	USIC0 Channel 0 Select/Control 2 Output
	U0C1_SELO2	O2	St/B	USIC0 Channel 1 Select/Control 2 Output
	$\overline{\text{BHE}}/\overline{\text{WRH}}$	OH	St/B	External Bus Interf. High-Byte Control Output Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$).
53	P11.5	O0 / I	St/B	Bit 5 of Port 11, General Purpose Input/Output
55	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	CCU63_CC60	O2 / I	St/B	CCU63 Channel 0 Input/Output
	AD13	OH / I	St/B	External Bus Interface Address/Data Line 13
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
56	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output
	TxDC0	O1	St/B	CAN Node 0 Transmit Data Output
	CCU63_ CC61	O2 / I	St/B	CCU63 Channel 1 Input/Output
	AD14	OH / I	St/B	External Bus Interface Address/Data Line 14
	ESR1_5	I	St/B	ESR1 Trigger Input 5
	EX0AINA	I	St/B	External Interrupt Trigger Input
57	P11.4	O0 / I	St/B	Bit 4 of Port 11, General Purpose Input/Output
58	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output
	TxDC1	O1	St/B	CAN Node 1 Transmit Data Output
	CCU63_ CC62	O2 / I	St/B	CCU63 Channel 2 Input/Output
	AD15	OH / I	St/B	External Bus Interface Address/Data Line 15
	ESR2_5	I	St/B	ESR2 Trigger Input 5
	EX1AINA	I	St/B	External Interrupt Trigger Input
59	P11.3	O0 / I	St/B	Bit 3 of Port 11, General Purpose Input/Output
60	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output
	CC2_24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output
61	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU63_ COUT63	O2	St/B	CCU63 Channel 3 Output
	CC2_16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	A16	OH	St/B	External Bus Interface Address Line 16
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P11.2	O0 / I	St/B	Bit 2 of Port 11, General Purpose Input/Output
	CCU63_ CCPOS2A	I	St/B	CCU63 Position Input 2
63	P4.1	O0 / I	St/B	Bit 1 of Port 4, General Purpose Input/Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_25	O3 / I	St/B	CAPCOM2 CC25IO Capture Inp./ Compare Out.
	$\overline{\text{CS}}1$	OH	St/B	External Bus Interface Chip Select 1 Output
64	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.
	A17	OH	St/B	External Bus Interface Address Line 17
	ESR1_0	I	St/B	ESR1 Trigger Input 0
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input
65	P11.1	O0 / I	St/B	Bit 1 of Port 11, General Purpose Input/Output
	CCU63_ CCPOS1A	I	St/B	CCU63 Position Input 1
66	P11.0	O0 / I	St/B	Bit 0 of Port 11, General Purpose Input/Output
	CCU63_ CCPOS0A	I	St/B	CCU63 Position Input 0
67	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_ SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	A18	OH	St/B	External Bus Interface Address Line 18
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input

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Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
68	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	$\overline{CS2}$	OH	St/B	External Bus Interface Chip Select 2 Output
	T2IN	I	St/B	GPT1 Timer T2 Count/Gate Input
69	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
70	P4.4	O0 / I	St/B	Bit 4 of Port 4, General Purpose Input/Output
	CC2_28	O3 / I	St/B	CAPCOM2 CC28IO Capture Inp./ Compare Out.
	$\overline{CS4}$	OH	St/B	External Bus Interface Chip Select 4 Output
	CLKIN2	I	St/B	RTC Count Clock Signal Input
71	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	CC2_27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	$\overline{CS3}$	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUD	I	St/B	GPT1 Timer T2 External Up/Down Control Input
75	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3 / I	St/B	CCU61 Channel 0 Input/Output
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input
76	P4.5	O0 / I	St/B	Bit 5 of Port 4, General Purpose Input/Output
	CC2_29	O3 / I	St/B	CAPCOM2 CC29IO Capture Inp./Compare Out.

General Device Information

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
77	P4.6	O0 / I	St/B	Bit 6 of Port 4, General Purpose Input/Output
	CC2_30	O3 / I	St/B	CAPCOM2 CC30IO Capture Inp./ Compare Out.
	T4IN	I	St/B	GPT1 Timer T4 Count/Gate Input
78	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
79	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3 / I	St/B	CCU61 Channel 1 Input/Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
80	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output 1)
	CC2_21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input
81	P4.7	O0 / I	St/B	Bit 7 of Port 4, General Purpose Input/Output
	CC2_31	O3 / I	St/B	CAPCOM2 CC31IO Capture Inp./ Compare Out.
	T4EUD	I	St/B	GPT1 Timer T4 External Up/Down Control Input

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Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
82	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input
	TCK_A	I	St/B	JTAG Clock Input
83	P0.2	O0 / I	St/B	Bit 2 of Port 0, General Purpose Input/Output
	U1C0_SCLKOUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC62	O3 / I	St/B	CCU61 Channel 2 Input/Output
	A2	OH	St/B	External Bus Interface Address Line 2
	U1C0_DX1B	I	St/B	USIC1 Channel 0 Shift Clock Input
84	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC60	O2 / I	St/B	CCU60 Channel 0 Input/Output
	AD0	OH / I	St/B	External Bus Interface Address/Data Line 0
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input
85	P3.0	O0 / I	St/B	Bit 0 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	BREQ	OH	St/B	External Bus Request Output
	ESR1_1	I	St/B	ESR1 Trigger Input 1
	U2C0_DX0A	I	St/B	USIC2 Channel 0 Shift Data Input
	U2C0_DX1A	I	St/B	USIC2 Channel 0 Shift Clock Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
86	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_ CC61	O2 / I	St/B	CCU60 Channel 1 Input/Output
	AD1	OH / I	St/B	External Bus Interface Address/Data Line 1
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input
87	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output
	U1C0_ SELO0	O1	St/B	USIC1 Channel 0 Select/Control 0 Output
	U1C1_ SELO1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output
	CCU61_ COUT60	O3	St/B	CCU61 Channel 0 Output
	A3	OH	St/B	External Bus Interface Address Line 3
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input
88	P3.1	O0 / I	St/B	Bit 1 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	HLDA	OH / I	St/B	External Bus Hold Acknowledge Output/Input Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	USIC2 Channel 0 Shift Data Input
89	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_ SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_ CC62	O2 / I	St/B	CCU60 Channel 2 Input/Output
	AD2	OH / I	St/B	External Bus Interface Address/Data Line 2
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COUT61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
92	TRef	IO	Sp/1	Control Pin for Core Voltage Generation 2)
93	P3.2	O0 / I	St/B	Bit 2 of Port 3, General Purpose Input/Output
	U2C0_SCLKOUT	O1	St/B	USIC2 Channel 0 Shift Clock Output
	U2C0_DX1B	I	St/B	USIC2 Channel 0 Shift Clock Input
	HOLD	I	St/B	External Bus Master Hold Request Input
94	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	A23	OH	St/B	External Bus Interface Address Line 23
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPIN	I	St/B	GPT2 Register CAPREL Capture Input
95	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COUT60	O2	St/B	CCU60 Channel 0 Output
	AD3	OH / I	St/B	External Bus Interface Address/Data Line 3
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input

Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
96	P0.5	O0 / I	St/B	Bit 5 of Port 0, General Purpose Input/Output
	U1C1_SCLKOUT	O1	St/B	USIC1 Channel 1 Shift Clock Output
	U1C0_SELO2	O2	St/B	USIC1 Channel 0 Select/Control 2 Output
	CCU61_COUT62	O3	St/B	CCU61 Channel 2 Output
	A5	OH	St/B	External Bus Interface Address Line 5
	U1C1_DX1A	I	St/B	USIC1 Channel 1 Shift Clock Input
	U1C0_DX1C	I	St/B	USIC1 Channel 0 Shift Clock Input
97	P3.3	O0 / I	St/B	Bit 3 of Port 3, General Purpose Input/Output
	U2C0_SELO0	O1	St/B	USIC2 Channel 0 Select/Control 0 Output
	U2C1_SELO1	O2	St/B	USIC2 Channel 1 Select/Control 1 Output
	U2C0_DX2A	I	St/B	USIC2 Channel 0 Shift Control Input
98	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COUT61	O2	St/B	CCU60 Channel 1 Output
	AD4	OH / I	St/B	External Bus Interface Address/Data Line 4
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
99	P3.4	O0 / I	St/B	Bit 4 of Port 3, General Purpose Input/Output
	U2C1_SELO0	O1	St/B	USIC2 Channel 1 Select/Control 0 Output
	U2C0_SELO1	O2	St/B	USIC2 Channel 0 Select/Control 1 Output
	U0C0_SELO4	O3	St/B	USIC0 Channel 0 Select/Control 4 Output
	U2C1_DX2A	I	St/B	USIC2 Channel 1 Shift Control Input

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Table 4 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
100	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLKOUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COUT62	O2	St/B	CCU60 Channel 2 Output
	AD5	OH / I	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
101	P3.5	O0 / I	St/B	Bit 5 of Port 3, General Purpose Input/Output
	U2C1_SCLKOUT	O1	St/B	USIC2 Channel 1 Shift Clock Output
	U2C0_SELO2	O2	St/B	USIC2 Channel 0 Select/Control 2 Output
	U0C0_SELO5	O3	St/B	USIC0 Channel 0 Select/Control 5 Output
	U2C1_DX1A	I	St/B	USIC2 Channel 1 Shift Clock Input
102	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COUT63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input