



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



16-Bit

Architecture

**XE167FM, XE167GM,
XE167HM, XE167KM**

16-Bit Single-Chip Real Time Signal
Controller

XE166 Family / Base Line

Data Sheet

V2.1 2011-07

Edition 2011-07

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2011 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

16-Bit

Architecture

**XE167FM, XE167GM,
XE167HM, XE167KM**

16-Bit Single-Chip Real Time Signal
Controller

XE166 Family / Base Line

Data Sheet

V2.1 2011-07

XE167xM

Revision History: V2.1, 2011-07

Previous Version(s):

V2.0, 2009-03

V1.3, 2008-11

V1.2, 2008-09

V1.1, 2008-06 Preliminary

V1.0, 2008-06 (Intermediate version)

Page	Subjects (major changes since last revisions)
52	ID registers added
99	ADC capacitances corrected (typ. vs. max.)
103	Conditions relaxed for Δf_{INT} Range for f_{WU} adapted according to PCN 2010-013-A Added startup time from power-on t_{SPO}
143	Quality #declarations added

Trademarks

C166™, TriCore™, and DAVE™ are trademarks of Infineon Technologies AG.

We Listen to Your Comments

Is there any information in this document that you feel is wrong, unclear or missing?

Your feedback will help us to continuously improve the quality of this document.

Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com



Table of Contents

1	Summary of Features	7
1.1	Basic Device Types	10
1.2	Definition of Feature Variants	11
2	General Device Information	13
2.1	Pin Configuration and Definition	14
2.2	Identification Registers	52
3	Functional Description	53
3.1	Memory Subsystem and Organization	54
3.2	External Bus Controller	57
3.3	Central Processing Unit (CPU)	58
3.4	Memory Protection Unit (MPU)	60
3.5	Memory Checker Module (MCHK)	60
3.6	Interrupt System	61
3.7	On-Chip Debug Support (OCDS)	62
3.8	Capture/Compare Unit (CAPCOM2)	63
3.9	Capture/Compare Units CCU6x	66
3.10	General Purpose Timer (GPT12E) Unit	68
3.11	Real Time Clock	72
3.12	A/D Converters	74
3.13	Universal Serial Interface Channel Modules (USIC)	75
3.14	MultiCAN Module	77
3.15	System Timer	78
3.16	Watchdog Timer	79
3.17	Clock Generation	79
3.18	Parallel Ports	80
3.19	Instruction Set Summary	81
4	Electrical Parameters	84
4.1	General Parameters	84
4.1.1	Absolut Maximum Rating Conditions	84
4.1.2	Operating Conditions	85
4.1.3	Pad Timing Definition	87
4.1.4	Parameter Interpretation	87
4.2	DC Parameters	88
4.2.1	DC Parameters	90
4.2.2	DC Parameters for Lower Voltage Area	92
4.2.3	Power Consumption	94
4.3	Analog/Digital Converter Parameters	99
4.4	System Parameters	103
4.5	Flash Memory Parameters	106

Table of Contents

4.6	AC Parameters	108
4.6.1	Testing Waveforms	108
4.6.2	Definition of Internal Timing	109
4.6.2.1	Phase Locked Loop (PLL)	110
4.6.2.2	Wakeup Clock	113
4.6.2.3	Selecting and Changing the Operating Frequency	113
4.6.3	External Clock Input Parameters	114
4.6.4	Pad Properties	116
4.6.5	External Bus Timing	119
4.6.5.1	Bus Cycle Control with the READY Input	125
4.6.5.2	External Bus Arbitration	127
4.6.6	Synchronous Serial Interface Timing	130
4.6.7	Debug Interface Timing	134
5	Package and Reliability	140
5.1	Packaging	140
5.2	Thermal Considerations	142
5.3	Quality Declarations	143

16-Bit Single-Chip Real Time Signal Controller**XE167xM (XE166 Family)****1 Summary of Features**

For a quick overview and easy reference, the features of the XE167xM are summarized here.

- High-performance CPU with five-stage pipeline and MPU
 - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
 - One-cycle 32-bit addition and subtraction with 40-bit result
 - One-cycle multiplication (16 × 16 bit)
 - Background division (32 / 16 bit) in 21 cycles
 - One-cycle multiply-and-accumulate (MAC) instructions
 - Enhanced Boolean bit manipulation facilities
 - Zero-cycle jump execution
 - Additional instructions to support HLL and operating systems
 - Register-based design with multiple variable register banks
 - Fast context switching support with two additional local register banks
 - 16 Mbytes total linear address space for code and data
 - 1024 Bytes on-chip special function register area (C166 Family compatible)
 - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels for up to 96 sources
 - Selectable external inputs for interrupt generation and wake-up
 - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
 - 8 Kbytes on-chip stand-by RAM (SBRAM)
 - 2 Kbytes on-chip dual-port RAM (DPRAM)
 - Up to 16 Kbytes on-chip data SRAM (DSRAM)
 - Up to 32 Kbytes on-chip program/data SRAM (PSRAM)
 - Up to 576 Kbytes on-chip program memory (Flash memory)
 - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules
 - Multi-functional general purpose timer unit with 5 timers
 - 16-channel general purpose capture/compare unit (CAPCOM2)
 - Up to 4 capture/compare units for flexible PWM signal generation (CCU6x)

Summary of Features

- Two Synchronizable A/D Converters with a total of up to 24 channels, 10-bit resolution, conversion time below 1 μ s, optional data preprocessing (data reduction, range check), broken wire detection
- Up to 8 serial interface channels to be used as UART, LIN, high-speed synchronous channel (SPI), IIC bus interface (10-bit addressing, 400 kbit/s), IIS interface
- On-chip MultiCAN interface (Rev. 2.0B active) with up to 128 message objects (Full CAN/Basic CAN) on up to 6 CAN nodes and gateway functionality
- On-chip system timer and on-chip real time clock
- Up to 12 Mbytes external address space for code and data
 - Programmable external bus characteristics for different address ranges
 - Multiplexed or demultiplexed external address/data buses
 - Selectable address bus width
 - 16-bit or 8-bit data bus width
 - Five programmable chip-select signals
 - Hold- and hold-acknowledge bus arbitration support
- Single power supply from 3.0 V to 5.5 V
- Programmable watchdog timer and oscillator watchdog
- Up to 119 general purpose I/O lines
- On-chip bootstrap loaders
- Supported by a full range of development tools including C compilers, macro-assembler packages, emulators, evaluation boards, HLL debuggers, simulators, logic analyzer disassemblers, programming boards
- On-chip debug support via Device Access Port (DAP) or JTAG interface
- 144-pin Green LQFP package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range:
 - SAF-...: -40°C to 85°C
 - SAK-...: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XE167xM please contact your sales representative or local distributor.

This document describes several derivatives of the XE167xM group:

Table 1 lists these derivatives and summarizes the differences.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XE167xM** is used for all derivatives throughout this document.

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XE167xM Basic Device Types

Derivative¹⁾	Flash Memory²⁾	PSRAM DSRAM³⁾	Capt./Comp. Modules	ADC⁴⁾ Chan.	Interfaces⁴⁾
XE167FM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	6 CAN Nodes, 8 Serial Chan.
XE167FM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	6 CAN Nodes, 8 Serial Chan.
XE167GM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.
XE167GM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.
XE167HM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	No CAN Nodes, 8 Serial Chan.
XE167HM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	No CAN Nodes, 8 Serial Chan.
XE167KM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	No CAN Nodes, 4 Serial Chan.
XE167KM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	No CAN Nodes, 4 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).

2) Specific information about the on-chip Flash memory in [Table 2](#).

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in [Table 4](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

1.2 Definition of Feature Variants

The XE167xM types are offered with several Flash memory sizes. [Table 2](#) describes the location of the available memory areas for each Flash memory size.

Table 2 Flash Memory Allocation

Total Flash Size	Flash Area A ¹⁾	Flash Area B	Flash Area C
576 Kbytes	C0'0000 _H ... C0'EFFF _H	C1'0000 _H ... C7'FFFF _H	CC'0000 _H ... CC'FFFF _H
384 Kbytes	C0'0000 _H ... C0'EFFF _H	C1'0000 _H ... C4'FFFF _H	CC'0000 _H ... CC'FFFF _H

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

Table 3 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0 ¹⁾	Flash 1	Flash 2	Flash 3
576 Kbytes	256	256	---	64
384 Kbytes	256	64	---	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).

The XE167xM types are offered with different interface options. [Table 4](#) lists the available channels for each option.

Table 4 Interface Channel Association

Total Number	Available Channels
16 ADC0 channels	CH0 ... CH15
8 ADC0 channels	CH0 ... CH7
8 ADC1 channels	CH0 ... CH7 (overlay: CH8 ... CH11)
6 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4, CAN5 128 message objects
2 CAN nodes	CAN0, CAN1 128 message objects
8 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1, U3C0, U3C1
4 serial channels	U0C0, U0C1, U1C0, U1C1

Summary of Features

The XE167xM types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

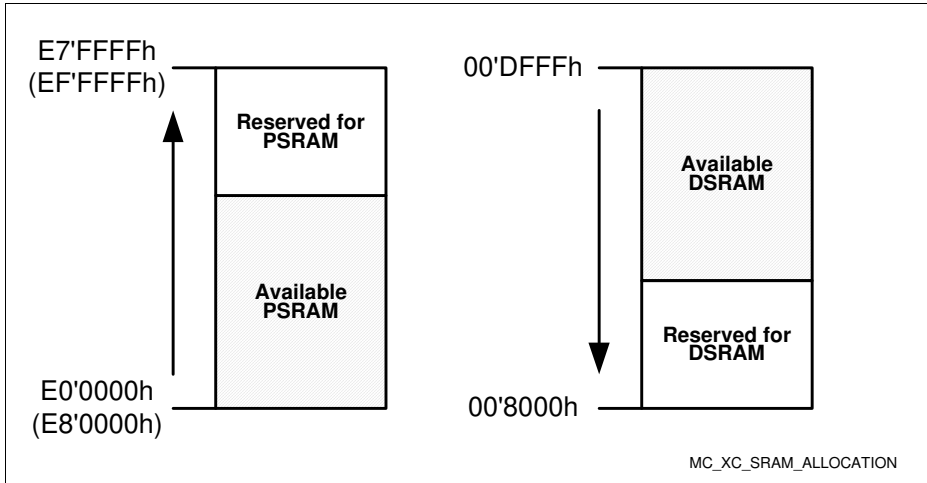


Figure 1 SRAM Allocation

2 General Device Information

The XE167xM series (16-Bit Single-Chip Real Time Signal Controller) is a part of the Infineon XE166 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 80 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

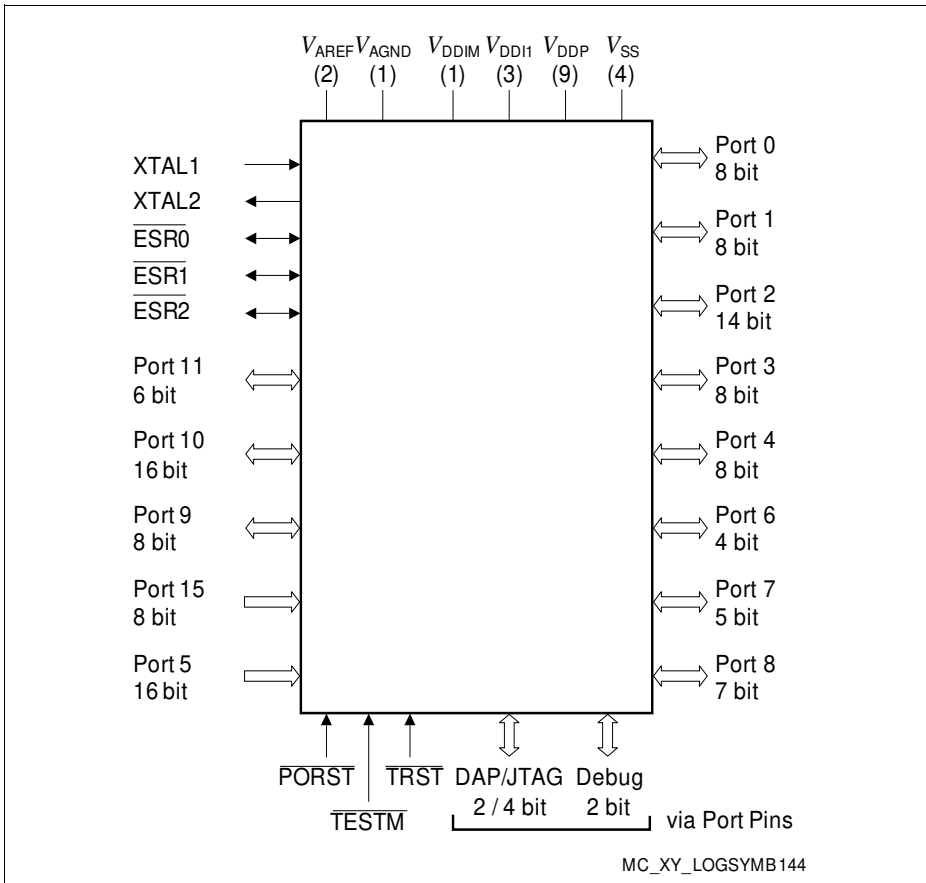


Figure 2 XE167xM Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XE167xM are described in detail in [Table 5](#), which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

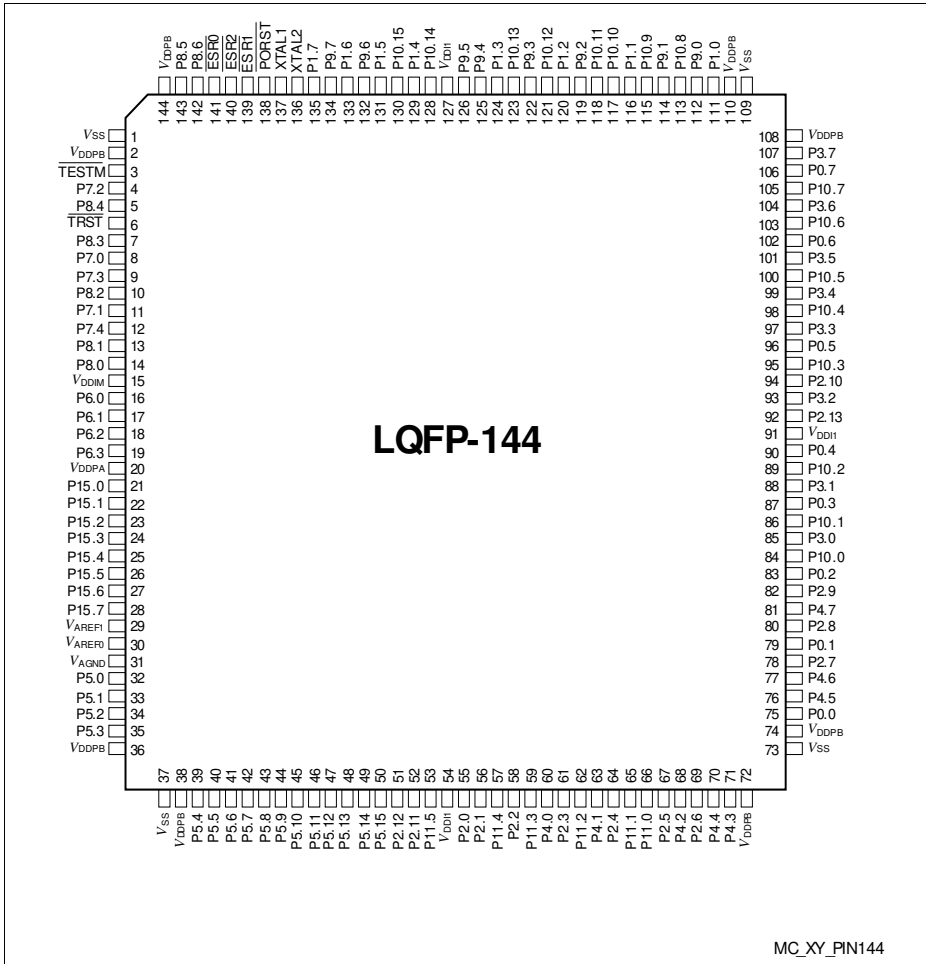


Figure 3 XE167xM Pin Configuration (top view)

Key to Pin Definitions

- **Ctrl.:** The output signal for a port pin is selected by bit field PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bit field PC to 1x00_B, output O1 is selected by 1x01_B, etc. Output signal OH is controlled by hardware.
- **Type:** Indicates the pad type and its power supply domain (A, B, M, 1).
 - St: Standard pad
 - Sp: Special pad e.g. XTALx
 - DP: Double pad - can be used as standard or high speed pad
 - In: Input only pad
 - PS: Power supply pad

Table 5 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	TESTM	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V _{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	TxDC5	O3	St/B	CAN Node 5 Transmit Data Output
	CCU62_CCP OS0A	I	St/B	CCU62 Position Input 0
	TDI_C	IH	St/B	JTAG Test Data Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P8.4	O0 / I	St/B	Bit 4 of Port 8, General Purpose Input/Output
	CCU60_COU T61	O1	St/B	CCU60 Channel 1 Output
	CCU62_CC6 1	O2	St/B	CCU62 Channel 1 Output
	TMS_D	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC6 1INB	I	St/B	CCU62 Channel 1 Input
6	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held <u>low</u> . A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE167xM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	Bit 3 of Port 8, General Purpose Input/Output
	CCU60_COU T60	O1	St/B	CCU60 Channel 0 Output
	CCU62_CC6 0	O2	St/B	CCU62 Channel 0 Output
	TDI_D	IH	St/B	JTAG Test Data Input If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	CCU62_CC6 0INB	I	St/B	CCU62 Channel 0 Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input
9	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
10	P8.2	O0 / I	St/B	Bit 2 of Port 8, General Purpose Input/Output
	CCU60_CC6 2	O1	St/B	CCU60 Channel 2 Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	U1C1_DOUT	O3	St/B	USIC1 Channel 1 Shift Data output
	CCU60_CC6 2INB	I	St/B	CCU60 Channel 2 Input
11	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	TXDC4	O2	St/B	CAN Node 4 Transmit Data Output
	CCU62_CTR APA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
12	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_SCLK OUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	CCU62_CCP OS2A	I	St/B	CCU62 Position Input 2
	TCK_C	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input	
13	P8.1	O0 / I	St/B	Bit 1 of Port 8, General Purpose Input/Output
	CCU60_CC6 1	O1	St/B	CCU60 Channel 1 Output
	CCU60_CC6 1INB	I	St/B	CCU60 Channel 1 Input
	RxDC1F	I	St/B	CAN Node 1 Receive Data Input
14	P8.0	O0 / I	St/B	Bit 0 of Port 8, General Purpose Input/Output
	CCU60_CC6 0	O1	St/B	CCU60 Channel 0 Output
	CCU60_CC6 0INB	I	St/B	CCU60 Channel 0 Input
16	P6.0	O0 / I	DA/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	DA/A	External Analog MUX Control Output 0 (ADC0)
	TxDC2	O2	DA/A	CAN Node 2 Transmit Data Output
	BRKOUT	O3	DA/A	OCDS Break Signal Output
	ADCx_REQG TyG	I	DA/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	DA/A	USIC1 Channel 1 Shift Data Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
17	P6.1	O0 / I	DA/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	DA/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	DA/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQT RyE	I	DA/A	External Request Trigger Input for ADC0/1
	RxDC2E	I	DA/A	CAN Node 2 Receive Data Input
	ESR1_6	I	DA/A	ESR1 Trigger Input 6
18	P6.2	O0 / I	DA/A	Bit 2 of Port 6, General Purpose Input/Output
	EMUX2	O1	DA/A	External Analog MUX Control Output 2 (ADC0)
	T6OUT	O2	DA/A	GPT12E Timer T6 Toggle Latch Output
	U1C1_SCLK OUT	O3	DA/A	USIC1 Channel 1 Shift Clock Output
	U1C1_DX1C	I	DA/A	USIC1 Channel 1 Shift Clock Input
19	P6.3	O0 / I	DA/A	Bit 3 of Port 6, General Purpose Input/Output
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_SELO 0	O3	DA/A	USIC1 Channel 1 Select/Control 0 Output
	U1C1_DX2D	I	DA/A	USIC1 Channel 1 Shift Control Input
	ADCx_REQT RyF	I	DA/A	External Request Trigger Input for ADC0/1
21	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
22	P15.1	I	In/A	Bit 1 of Port 15, General Purpose Input
	ADC1_CH1	I	In/A	Analog Input Channel 1 for ADC1
23	P15.2	I	In/A	Bit 2 of Port 15, General Purpose Input
	ADC1_CH2	I	In/A	Analog Input Channel 2 for ADC1
	T5INA	I	In/A	GPT12E Timer T5 Count/Gate Input
24	P15.3	I	In/A	Bit 3 of Port 15, General Purpose Input
	ADC1_CH3	I	In/A	Analog Input Channel 3 for ADC1
	T5EUDA	I	In/A	GPT12E Timer T5 External Up/Down Control Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
25	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6INA	I	In/A	GPT12E Timer T6 Count/Gate Input
26	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUDA	I	In/A	GPT12E Timer T6 External Up/Down Control Input
27	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1
28	P15.7	I	In/A	Bit 7 of Port 15, General Purpose Input
	ADC1_CH7	I	In/A	Analog Input Channel 7 for ADC1
29	V _{AREF1}	-	PS/A	Reference Voltage for A/D Converter ADC1
30	V _{AREF0}	-	PS/A	Reference Voltage for A/D Converter ADC0
31	V _{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
32	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
33	P5.1	I	In/A	Bit 1 of Port 5, General Purpose Input
	ADC0_CH1	I	In/A	Analog Input Channel 1 for ADC0
34	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input
35	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
39	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	CCU63_T12 HRB	I	In/A	External Run Control Input for T12 of CCU63
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
40	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12 HRB	I	In/A	External Run Control Input for T12 of CCU60
41	P5.6	I	In/A	Bit 6 of Port 5, General Purpose Input
	ADC0_CH6	I	In/A	Analog Input Channel 6 for ADC0
42	P5.7	I	In/A	Bit 7 of Port 5, General Purpose Input
	ADC0_CH7	I	In/A	Analog Input Channel 7 for ADC0
43	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1/2/3
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1/2/3
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
44	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	ADC1_CH9	I	In/A	Analog Input Channel 9 for ADC1
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
45	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61
46	P5.11	I	In/A	Bit 11 of Port 5, General Purpose Input
	ADC0_CH11	I	In/A	Analog Input Channel 11 for ADC0
	ADC1_CH11	I	In/A	Analog Input Channel 11 for ADC1
47	P5.12	I	In/A	Bit 12 of Port 5, General Purpose Input
	ADC0_CH12	I	In/A	Analog Input Channel 12 for ADC0
48	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
	CCU63_T13 HRF	I	In/A	External Run Control Input for T13 of CCU63
49	P5.14	I	In/A	Bit 14 of Port 5, General Purpose Input
	ADC0_CH14	I	In/A	Analog Input Channel 14 for ADC0
50	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
	RxDC2F	I	In/A	CAN Node 2 Receive Data Input
51	P2.12	O0 / I	St/B	Bit 12 of Port 2, General Purpose Input/Output
	U0C0_SELO 4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_SELO 3	O2	St/B	USIC0 Channel 1 Select/Control 3 Output
	TXDC2	O3	St/B	CAN Node 2 Transmit Data Output
	READY	IH	St/B	External Bus Interface READY Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
52	P2.11	O0 / I	St/B	Bit 11 of Port 2, General Purpose Input/Output
	U0C0_SELO 2	O1	St/B	USIC0 Channel 0 Select/Control 2 Output
	U0C1_SELO 2	O2	St/B	USIC0 Channel 1 Select/Control 2 Output
	U3C1_DOUT	O3	St/B	USIC3 Channel 1 Shift Data Output
	BHE/WRH	OH	St/B	External Bus Interf. High-Byte Control Output Can operate either as Byte High Enable (BHE) or as Write strobe for High Byte (WRH).
53	P11.5	O0 / I	St/B	Bit 5 of Port 11, General Purpose Input/Output
	CCU61_CC6 0	O1	St/B	CCU61 Channel 0 Output
	CCU61_COU T63	O2	St/B	CCU61 Channel 3 Output
	U3C1_SELO 1	O3	St/B	USIC3 Channel 1 Select/Control 1 Output
	CCU61_CC6 0INB	I	St/B	CCU61 Channel 0 Input
	U3C1_DX2B	I	St/B	USIC3 Channel 1 Shift Control Input
55	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	TxDC5	O1	St/B	CAN Node 5 Transmit Data Output
	CCU63_CC6 0	O2	St/B	CCU63 Channel 0 Output
	AD13	OH / IH	St/B	External Bus Interface Address/Data Line 13
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input
	CCU63_CC6 0INB	I	St/B	CCU63 Channel 0 Input
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
56	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output
	TxDC0	O1	St/B	CAN Node 0 Transmit Data Output
	CCU63_CC6 1	O2	St/B	CCU63 Channel 1 Output
	AD14	OH / IH	St/B	External Bus Interface Address/Data Line 14
	RxDC5C	I	St/B	CAN Node 5 Receive Data Input
	CCU63_CC6 1INB	I	St/B	CCU63 Channel 1 Input
	T5EUDB	I	St/B	GPT12E Timer T5 External Up/Down Control Input
	ESR1_5	I	St/B	ESR1 Trigger Input 5
57	P11.4	O0 / I	St/B	Bit 4 of Port 11, General Purpose Input/Output
	CCU61_CC6 2	O1	St/B	CCU61 Channel 2 Output
	U3C1_DOUT	O2	St/B	USIC3 Channel 1 Shift Data Output
	RxDC5B	I	St/B	CAN Node 5 Receive Data Input
	CCU61_CC6 2INB	I	St/B	CCU61 Channel 2 Input
	U3C1_DX0B	I	St/B	USIC3 Channel 1 Shift Data Input
58	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output
	TxDC1	O1	St/B	CAN Node 1 Transmit Data Output
	CCU63_CC6 2	O2	St/B	CCU63 Channel 2 Output
	AD15	OH / IH	St/B	External Bus Interface Address/Data Line 15
	CCU63_CC6 2INB	I	St/B	CCU63 Channel 2 Input
	ESR2_5	I	St/B	ESR2 Trigger Input 5

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
59	P11.3	O0 / I	St/B	Bit 3 of Port 11, General Purpose Input/Output
	CCU61_COU T63	O1	St/B	CCU61 Channel 3 Output
	CCU61_COU T62	O2	St/B	CCU61 Channel 2 Output
	TxDC5	O3	St/B	CAN Node 5 Transmit Data Input
	CCU61_T13 HRF	I	St/B	External Run Control Input for T13 of CCU61
60	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output
	CC2_CC24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output
61	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU63_COU T63	O2	St/B	CCU63 Channel 3 Output
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	A16	OH	St/B	External Bus Interface Address Line 16
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input
62	P11.2	O0 / I	St/B	Bit 2 of Port 11, General Purpose Input/Output
	CCU61_CC6 1	O1	St/B	CCU61 Channel 1 Output
	U3C1_DOUT	O2	St/B	USIC3 Channel 1 Shift Data Output
	CCU63_CCP OS2A	I	St/B	CCU63 Position Input 2
	CCU61_CC6 1INB	I	St/B	CCU61 Channel 1 Input