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SAF784x

One chip CD audio device with integrated MP3/WMA decoder

Rev. 02 — 9 May 2008 Product data sheet

1. General description

The SAF784x is a single-chip solution CD audio decoder with on-chip MP3 and WMA decoding, digital servo, audio DAC, sample-rate converter, preamplifier, laser driver and integrated ARM7TDMI-S microprocessor. The device contains all of the required ROM and RAM, including an internal re-programmable Flash ROM, and is targeted at low-cost compressed audio CD applications. The design is a one-chip CD audio decoder IC, with additions to allow low-cost system implementation of MP3 and WMA decoding.

2. Features

2.1 Features

- Channel decoder and digital servo
- 32-bit embedded ARM7 RISC microprocessor supporting both 32-bit and 16-bit ('Thumb') instruction sets
- Maximum ARM operating frequency of 76 MHz, equivalent to 68 MIPS
- Decoding of compressed audio stream (MP3/WMA) on ARM7 core
- All memories required for MP3/WMA decoding embedded on chip: combination of 130 kB mask-programmed internal program ROM (to reduce wait-states on high-speed code, e.g. decompression algorithms), 42 kB boot ROM, 64 kB of internal re-programmable Flash ROM (for simple re-programming of application code) 110 kB internal SRAM
- Programmable clock frequency for ARM microprocessor - allowing users to trade-off power consumption and processing power depending on requirements
- Block decoder hardware to perform C3 error correction
- Sample-rate converter circuit to convert compressed audio sample rates (in the range 8 kHz to 48 kHz) to an output rate of 44.1 kHz
- Microprocessor access to digital representations of the diode input signals from the optical pickup; the microprocessor can also generate the servo output signals RA, FO, SL, allowing the possibility of additional servo algorithms in software
- Programmable PDM outputs (effectively sine and cosine) to allow use of stepper motor for sledge mechanism
- Microprocessor access to audio streams, both from the internal CD decoder and an external stereo auxiliary input (e.g. an analog source from a tuner, converted to digital via on-chip ADCs) to allow audio processing algorithms in the ARM microprocessor, e.g. bass boost, volume control
- Four general-purpose analog inputs (A_IN1 to A_IN4) allowing the ARM microprocessor access to other external analog signals, e.g. low-cost keypad, temperature sensor, via on-chip ADCs

- Two additional analog audio inputs (AUX_L, AUX_R) to allow the ARM microprocessor access to external audio signals (e.g. tuner); allows audio algorithms (e.g. bass boost) to be performed on external audio signals
- Real-time clock operated from separate 32 kHz crystal; allows low-power Standby mode with real-time clock still operational
- Watchdog timer
- I^2S-bus, S/PDIF, subcode (V4) and subcode sync outputs
- 32 GPIOs
- Two standard UART channels
- Two external interrupt pins
- I^2C-bus interface configurable for master or slave modes, supporting 100 kbit/s and 400 kbit/s standards
- Slave I^2S-bus mode, in which the channel decoder can synchronize the CD playback speed to an I^2S-bus clock input
- Integrated digital HF/Mirror detector with measurement of minimum and maximum peak values, amplitude and offset
- Integrated CD-text decoder
- Up to 6× decode speed, CLV or CAV modes
- LQFP144 package with 0.5 mm pin pitch
- Separate left and right channel digital silence detection available on KILL pins
- Digital silence detection available on loopback data from external source as well as internal data
- ‘Filterless’ pseudo bit stream audio DAC with minimal external components
- Stereo line outputs for audio DAC
- Loopback mode allowing the use of integrated DAC with external I^2S-bus/EIAJ sources
- Compatible with voltage mode mechanisms
- On-chip buffering and filtering of the diode signals from the mechanism in order to optimize the signals for the decoder and servo parts
- LF (servo) signals converted to digital representations by Sigma-Delta ADCs shared between pairs of channels to minimize DC offset between channels
- HF part summed from signals D1 to D4 and converted to digital signals by HF 6-bit ADC
- Selectable DC offset cancellation of quiescent mechanism voltages and dark currents, digitally controlled; additional fine DC-offset cancellation in digital domain
- Eye pattern monitor system to observe selectable points within the analog pre-amp
- Current and average jitter values available via registers
- On-chip laser power control, up to maximum currents of 120 mA
- Laser on-off control, including ‘soft’-start control - zero-to-nominal output power in 1 ms
- Monitor control and feedback circuit to maintain nominal output power throughout laser life
- Configured for Nsub (N-substrate) monitor diode
- JTAG interface for device access and ARM code development (compatible with ARM multi-ICE)
- All digital input pins 5 V tolerant
- Low-latency static memory interface to access a maximum of two 2 MB memory

- This product has been qualified in accordance with AEC-Q100

2.2 Formats

Reads the following CD-decode formats

- CD-R
- CD-RW
- CD-DA (*CD Red Book; IEC 60908*)
- CD-ROM (Mode 1 and Mode 2)
- CD-MP3
- CD-WMA
- Video CD
- SACD (CD layer only)
- Support 80 minute to 100 minute CD playback
- Multi-session discs

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SAF7846HL	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
SAF7847HL			

4. Block diagram

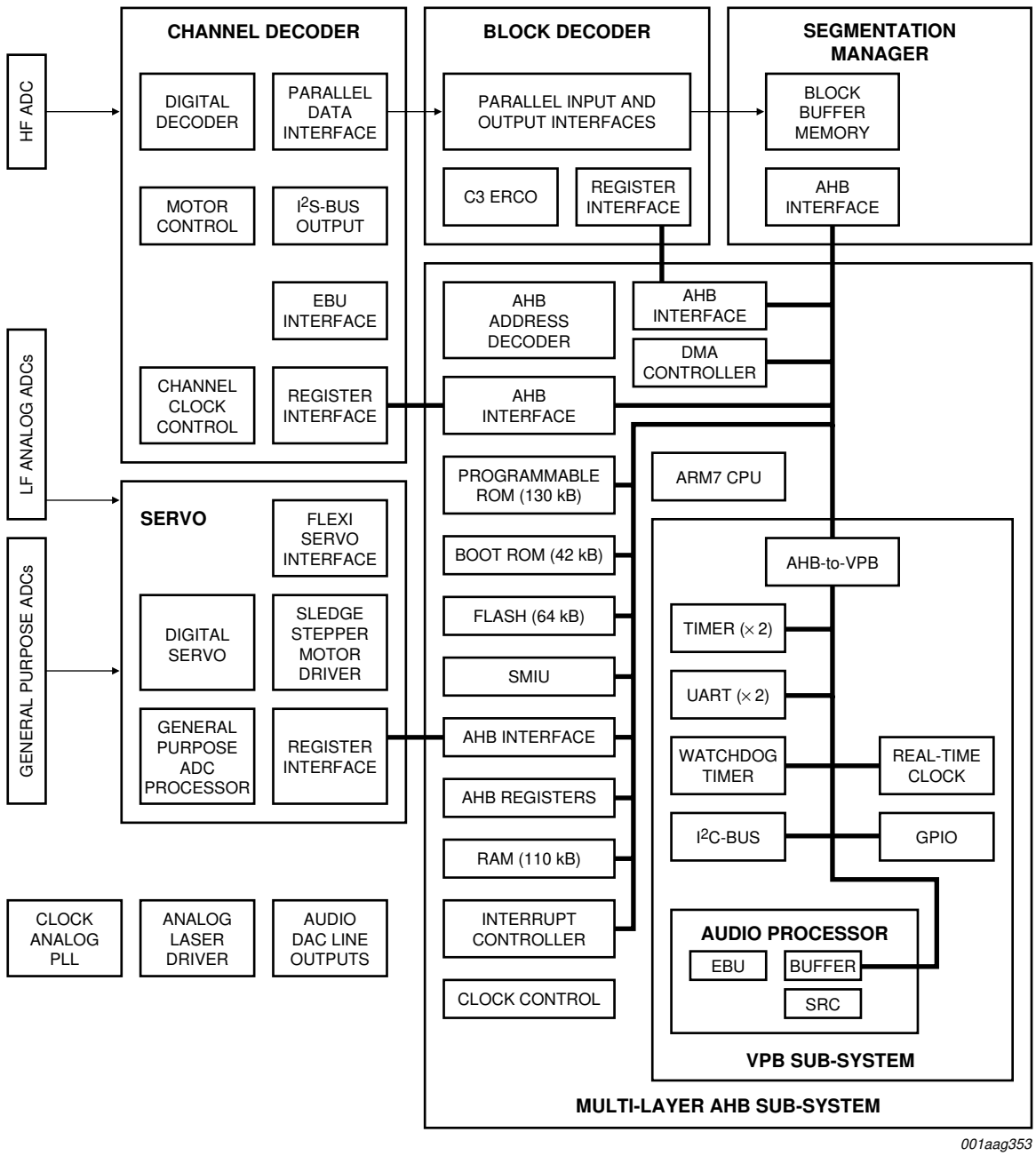


Fig 1. SAF784x top level block diagram

5. Pinning information

5.1 Pinning

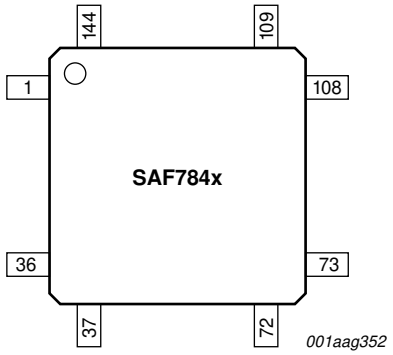


Fig 2. SAF784x pinning diagram

5.2 Pin description

Table 2. Pin description

All digital inputs and bidirectional pins are 5 V tolerant.

Symbol	Pin	Type[1]	Description
SL_SIN	1	O	sledge actuator/stepper motor PDM output (sine)
COS/GPIO31	2	B	stepper motor PDM output (cosine)/general purpose I/O 31
LPOWER	3	P	laser power supply
LASER	4	P	laser diode drive
MONITOR	5	AI	laser monitor diode input
VSSA1	6	P	analog ground 1
HF_MON	7	AIO	HF monitor output signal
VDDA1	8	P	analog supply voltage 1
D1	9	AI	central diode signal voltage input
D2	10	AI	central diode signal voltage input
D3	11	AI	central diode signal voltage input
D4	12	AI	central diode signal voltage input
R1	13	AI	satellite diode signal voltage input
R2	14	AI	satellite diode signal voltage input
AUX_L	15	AI	auxiliary audio left signal input
AUX_R	16	AI	auxiliary audio right signal input
VDDA2	17	P	analog supply voltage 2
OPU_REF_OUT	18	AO	OPU reference voltage
VSSA2	19	P	analog ground 2
OSCOUT	20	AO	crystal or resonator output
OSCIN	21	AI	crystal or resonator input
VDDA3	22	P	analog supply voltage 3

Table 2. Pin description *...continued*

All digital inputs and bidirectional pins are 5 V tolerant.

Symbol	Pin	Type[1]	Description
DAC_LP	23	AO	audio DAC left channel differential output (positive)
DAC_LN	24	AO	audio DAC left channel differential output (negative)
DAC_VREF	25	AIO	audio DAC decoupling point (10 µF/100 nF to ground)
DAC_RN	26	AO	audio DAC right channel differential output (negative)
DAC_RP	27	AO	audio DAC right channel differential output (positive)
DAC_FGND	28	P	audio DAC floating ground
VSSA3	29	P	analog ground 3
OSC_32K_IN	30	AO	32 kHz crystal input
OSC_32K_OUT	31	AO	32 kHz crystal output
VDDD1	32	P	digital core supply voltage 1
A_IN1/GPIO0	33	AIB	analog input 1/general purpose I/O 0
A_IN2/GPIO1	34	AIB	analog input 2/general purpose I/O 1
A_IN3/GPIO2	35	AIB	analog input 3/general purpose I/O 2
A_IN4/GPIO3	36	AIB	analog input 4/general purpose I/O 3
VSSD1	37	P	digital core ground 1
TX/GPIO4	38	B	UART transmit/general purpose I/O 4
RX/GPIO5	39	B	UART receive/general purpose I/O 5
TX2/GPIO6	40	B	UART2 transmit/general purpose I/O 6
DM_ADDR_0	41	O	external memory address bit 0
RX2/GPIO7	42	B	UART2 receive/general purpose I/O 7
DM_ADDR_1	43	O	external memory address bit 1
SDA	44	B	micro interface data I/O line (open-drain output)
DM_ADDR_2	45	O	external memory address bit 2
SCL	46	B	microprocessor interface clock line
DM_ADDR_3	47	O	external memory address bit 3
LKILL	48	O	kill output for left channel (configurable as open-drain)
DM_ADDR_4	49	O	external memory address bit 4
RKILL	50	O	kill output for right channel (configurable as open-drain)
VSSP1	51	P	digital ground 1 to periphery (pads)
DOBM	52	O	bi-phase mark output (no external buffer required)
VDDP1	53	P	digital supply voltage 1 to periphery (pads)
DM_ADDR_5	54	O	external memory address bit 5
INT2/GPIO8	55	B	external interrupt 2/general purpose I/O 8
DM_ADDR_6	56	O	external memory address bit 6
GPIO9	57	B	general purpose I/O 9
DM_ADDR_7	58	O	external memory address bit 7
GPIO10	59	B	general purpose I/O 10
DM_ADDR_8	60	O	external memory address bit 8
GPIO11	61	B	general purpose I/O 11
DM_ADDR_9	62	O	external memory address bit 9

Table 2. Pin description *...continued*

All digital inputs and bidirectional pins are 5 V tolerant.

Symbol	Pin	Type[1]	Description
GPIO12	63	B	general purpose I/O 12
DM_ADDR_10	64	O	external memory address bit 10
GPIO13	65	B	general purpose I/O 13
DM_ADDR_11	66	O	external memory address bit 11
GPIO14	67	B	general purpose I/O 14
DM_ADDR_12	68	O	external memory address bit 12
GPIO15	69	B	general purpose I/O 15
DM_ADDR_13	70	O	external memory address bit 13
SDI/GPIO16	71	B	serial data input (loopback)/general purpose I/O 16
DM_ADDR_14	72	O	external memory address bit 14
WLCI/GPIO17	73	B	serial word clock input (loopback)/general purpose I/O 17
DM_ADDR_15	74	O	external memory address bit 15
SCLI/GPIO18	75	B	serial bit clock input (loopback)/general purpose I/O 18
VSSD2	76	P	digital core ground 2
VDDD2	77	P	digital core supply voltage 2
DM_ADDR_16	78	O	external memory address bit 16
T1/GPIO19	79	B	tacho input 1 (for spindle motor sensor)/general purpose I/O 19
DM_ADDR_17	80	O	external memory address bit 17
T2/GPIO20	81	B	tacho input 2 (for spindle motor sensor)/general purpose I/O 20
DM_ADDR_18	82	O	external memory address bit 18
T3/GPIO21	83	B	tacho input 3 (for spindle motor sensor)/general purpose I/O 21
DM_ADDR_19	84	O	external memory address bit 19
PWM1/CAP1/GPIO22	85	B	timer PWM output 1/capture input 1/general purpose I/O 22
DM_ADDR_20	86	O	external memory address bit 20
PWM2/CAP2/GPIO23	87	B	timer PWM output 2/capture input 2/general purpose I/O 23
DM_BLS_0	88	O	external RAM lower-byte lane select (lower 8-bits)
PWM3/CAP3/GPIO24	89	B	timer PWM output 3/capture input 3/general purpose I/O 24
DM_BLS_1	90	O	external RAM upper byte lane select (upper 8-bits)
PWM4/CAP4/GPIO25	91	B	timer PWM output 4/capture input 4/general purpose I/O 25
DM_WE	92	O	external memory right control
MEAS/GPIO26	93	B	channel decoder telemetry output/general purpose I/O 26
DM_OE	94	O	external memory output enable
CFLG/GPIO27	95	B	channel decoder correction statistics/general purpose I/O 27
DM_CE_0	96	O	external memory chip-select Bank 0
CL1/GPIO28	97	B	clock output for sampling channel decoder telemetry outputs/general purpose I/O 28
GPIO29	98	B	general purpose I/O 29
VSSP2	99	P	digital ground 2 to periphery (pads)
$\overline{\text{RESET}}$	100	IUH	power-on reset (active LOW)
VDDP2	101	P	digital supply voltage 2 to periphery (pads)

Table 2. Pin description *...continued*

All digital inputs and bidirectional pins are 5 V tolerant.

Symbol	Pin	Type[1]	Description
DM_CE_1	102	O	external memory chip-select Bank 1
INT1	103	IUH	external interrupt 1
DM_DATA_0	104	B	external memory data input/output bit 0
VSSD3	105	P	digital core ground 3
VDDD3	106	P	digital core supply voltage 3
EF	107	O	C2 error flag
DM_DATA_1	108	B	external memory data input/output bit 1
DATA	109	O	serial data output
DM_DATA_2	110	B	external memory data input/output bit 2
WCLK	111	O	word clock output
DM_DATA_3	112	B	external memory data input/output bit 3
SCLK	113	O	serial clock output
DM_DATA_4	114	B	external memory data input/output bit 4
SYNC	115	O	EFM frame synchronization
DM_DATA_5	116	B	external memory data input/output bit 5
V4/CL16	117	B	versatile pin 4/clock output 16.9344 MHz
DM_DATA_6	118	B	external memory data input/output bit 6
TDI	119	IU	JTAG1/2 test data input
DM_DATA_7	120	B	external memory data input/output bit 7
TMS	121	IU	JTAG1/2 test mode select
DM_DATA_8	122	B	external memory data input/output bit 8
TCK	123	IDH	JTAG1/2 test clock
DM_DATA_9	124	B	external memory data input/output bit 9
$\overline{\text{TRST}}$	125	IU	JTAG1/2 asynchronous reset (active LOW)
DM_DATA_10	126	B	external memory data input/output bit 10
TDO	127	O	JTAG1/2 test data output
DM_DATA_11	128	B	external memory data input/output bit 11
ARM_JTAG_SEL	129	I	select ARM JTAG (active HIGH) or general JTAG (active LOW)
DM_DATA_12	130	B	external memory data input/output bit 12
RTCK/GPIO30	131	B	JTAG clock output/general purpose I/O 30
DM_DATA_13	132	B	external memory data input/output bit 13
DEV_ROM	133	ID	development ROM select (LOW = internal ROM)
DM_DATA_14	134	B	external memory data input/output bit 14
VSSD4	135	P	digital core ground 4
VDDD4	136	P	digital core supply 4
DM_DATA_15	137	B	external memory data input/output bit 15
MOTO1	138	O	motor output 1
MOTO2	139	O	motor output 2
VSSP3	140	P	digital ground 3 to periphery (pads)
VDDP3	141	P	digital supply voltage 3 to periphery (pads)

Table 2. Pin description *...continued*

All digital inputs and bidirectional pins are 5 V tolerant.

Symbol	Pin	Type[1]	Description
RA	142	O	radial actuator
FO	143	O	focus actuator
n.c.	144	-	not connected pad

[1] See Table 3 for pin type definition.

Table 3. Pin type definition

Type	Definition
AI	analog input
AO	analog output
AIO	analog input/output
AIB	analog input or bidirectional
ID	digital input with pull-down
IDH	digital input with pull-down and hysteresis
IU	digital input with pull-up
IUH	digital input with pull-up and hysteresis
O	digital output, slew-rate limited
B	digital bidirectional, slew-rate limited
P	power connection

6. Functional description

6.1 Analog data acquisition

The input signals from the OPU photodiodes contain information used in the servo loops and the high frequency data from which the audio samples are reconstructed. The SAF784x contains all the necessary circuitry to process the photodiode signals directly and hence removes the need for a separate external diode signal preamplifier.

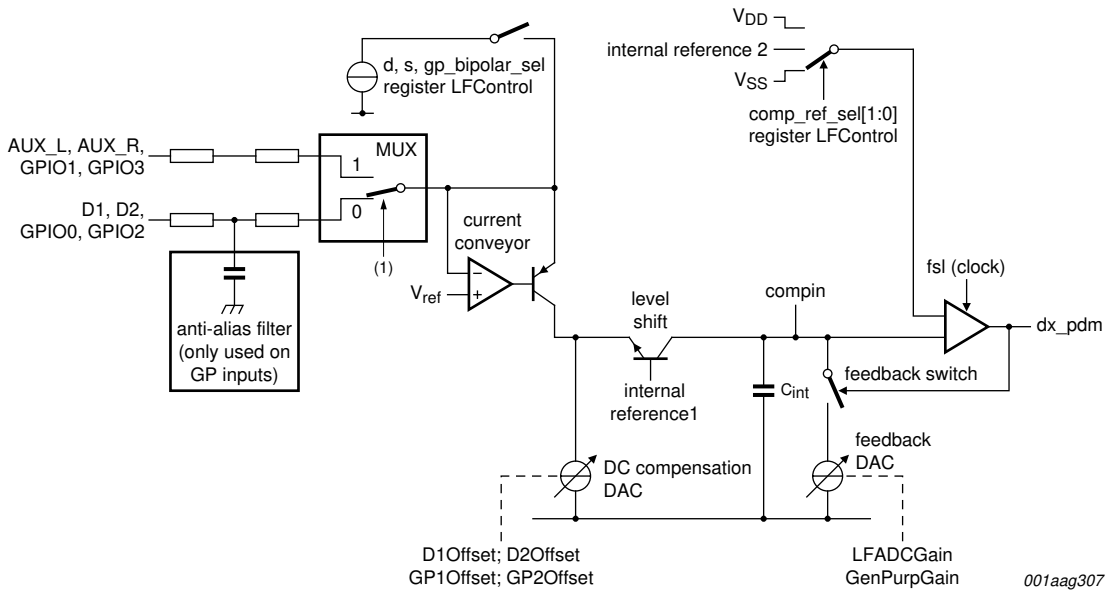
6.1.1 LF acquisition

The LF signal path acquires the photodiode voltage signals and converts them into 4 MHz pulse-density modulated digital data streams. These streams are processed within the digital servo to control the focus, radial and sledge loops.

The servo processing makes use of the difference calculations D1 − D2, D3 − D4 and R1 − R2. Ideally these differences should be zero when the quantities D1 to R2 are equal due to the laser illumination. However in a practical system, errors reduce the accuracy of the signal processing. Two main forms of errors exist - DC offsets and relative gain mismatch between the difference channels.

The DC offsets are minimized in the SAF784x by DC-offset compensation circuitry which allows the DC present in the Pulse Density Modulation (PDM) streams to be measured when the laser is switched off, and then subtracted from the signals in the digital domain when the laser is on.

Relative gain mismatch is minimized by using carefully scaled circuitry in the time-continuous parts of the signal path, and by time-sharing circuitry in the time-discrete parts. A simplified block diagram of the LF acquisition path is shown in Figure 3.



(1) if_auxin_sel = 0: D1 and D2 selected; if_auxin_sel = 1: AUX_L, AUX_R selected.
if_gpio_sel = 0: GPIO0 and GPIO2 selected; if_gpio_sel = 1: GPIO1 and GPIO3 selected.

Fig 3. LF acquisition block diagram

The output of the OPU is converted to a current across the input resistor. The current conveyor provides a low input impedance and a high output impedance and sets a virtual earth at the end of the voltage-to-current converter to the same voltage as V_{ref} (1.6 V).

The level shifter acts as a summing node for the DC cancellation and produces a current that is referenced to an internal bias voltage which is independent of V_{ref}.

The output current charges an integration capacitor C_{int}. When the voltage reaches V_{DDA} / 2, the comparator switches and sends a feedback current that has opposite polarity to the input current which tries to discharge the capacitor.

The register LFADCGain defines the amount of feedback current and so sets the ADC gain. A PDM waveform appears at the output of the ADC, and is passed through a low-pass filter (in the digital domain). The average value at the output of the filter is in proportion to the voltage between V_i and V_{ref}.

Input signals from the OPU, GPIO inputs and the AUX inputs are routed to eight ADCs comprising six LF ADCs and two general purpose ADCs. ADCs LF1, LF2, GP1 and GP2 are shared by some of these inputs which are routed via an internal multiplexer. ADC LF1 is shared by input pairs D1, D2, and AUX_L, AUX_R via the multiplexer. ADCs LF3 to LF6 are dedicated to inputs D3, D4, R1 and R2 respectively. ADC GP2 is shared by input pairs GPIO0, GPIO2, and GPIO1, GPIO3 via the multiplexer. The internal multiplexer is controlled by register AuxandGPADCControl.

6.1.2 HF acquisition

The HF data (EFM) signal is obtained by summing the signals from the three or four central diodes of the OPU and filtering and converting the signals to a digital representation via a 6-bit HF ADC. Figure 4 shows a simplified block diagram of the HF path.

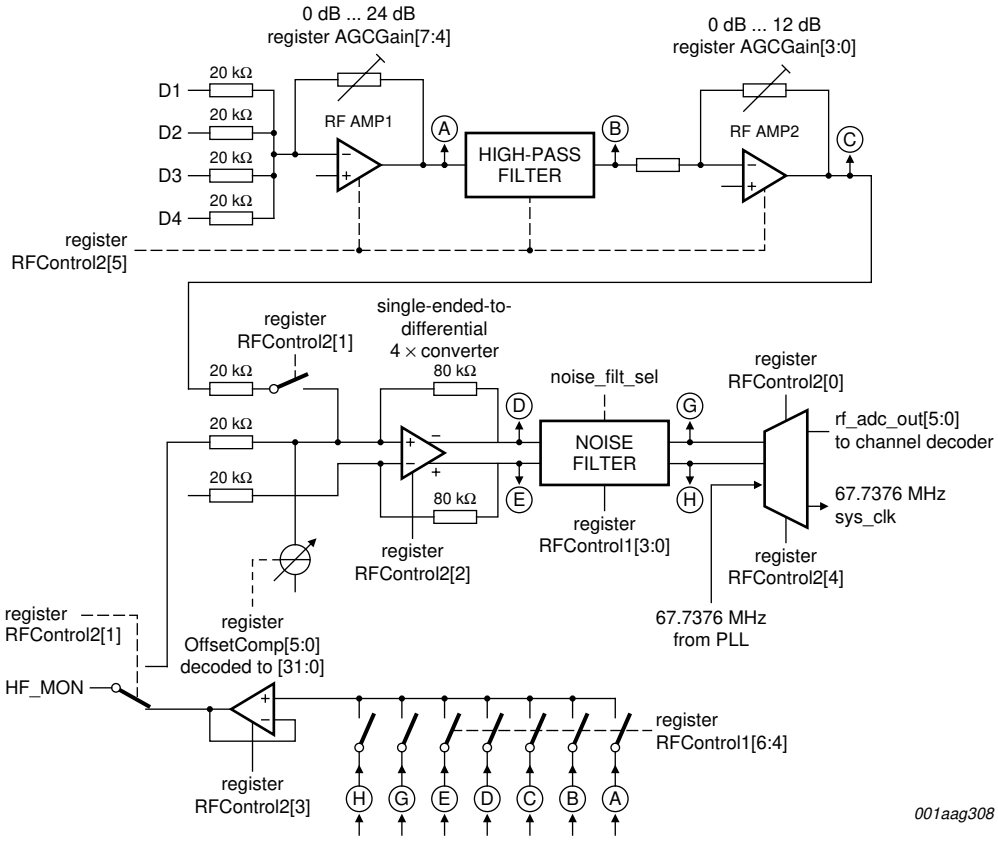


Fig 4. HF acquisition block diagram

The four diode signals D1, D2, D3 and D4 are summed in the first RF amplifier. The gain of the first amplifier is controlled by register AGCGain[7:4].

A second gain stage has been added to lessen the gain bandwidth requirements of a single gain stage operational amplifier and also to act as dynamic Automatic Gain Control (AGC). The gain of this amplifier is set by register AGCGain[3:0] and can be changed on-the-fly from the ARM microprocessor. The gain range accommodates 12 dB of gain needed to boost the signal when the laser tracks across a fingerprint defect on the disc.

CD-R, CD-RW, and finger prints, not only reduce the AC signal amplitude compared to a perfectly pressed disc but also reduces the DC pedestal voltage. The high-pass filter will remove all DC present at the input, but offsets will be added by the second and third gain stages. A 5-bit plus-sign DAC controlled by register OffsetComp[5:0] adds a current to compensate for this offset. The current reduces in linear dB steps and follows the AC gain.

To help users set up the correct gain and DC offset for each particular mechanism, an eye pattern monitor facility is included. This consists of a high frequency buffer amplifier whose input can be selected to monitor various important nodes within the analog RF path. The monitor point is controlled by register RFControl1[6:4] field RFMONSEL. The output of the buffer drives HF_MON pin (pin 7). This register also controls the roll-off frequency of the noise filter which is in front of the 6-bit ADC in the RF path.

Various blocks within the analog RF path can be powered down if required, including the complete path. These power-down bits are controlled by register RFControl2[5:0].

In addition, the 6-bit RF ADC can be stand-alone tested in application mode, or a separate external RF path IC can be connected to SAA7834 by selecting bit 1 of register RFBypassSel. The input for the RF signal is then via pin HF_MON. In this mode the central diode summing circuit, RF AMP1, high-pass filter and RF AMP2 are all bypassed.

6.2 Analog clock generation

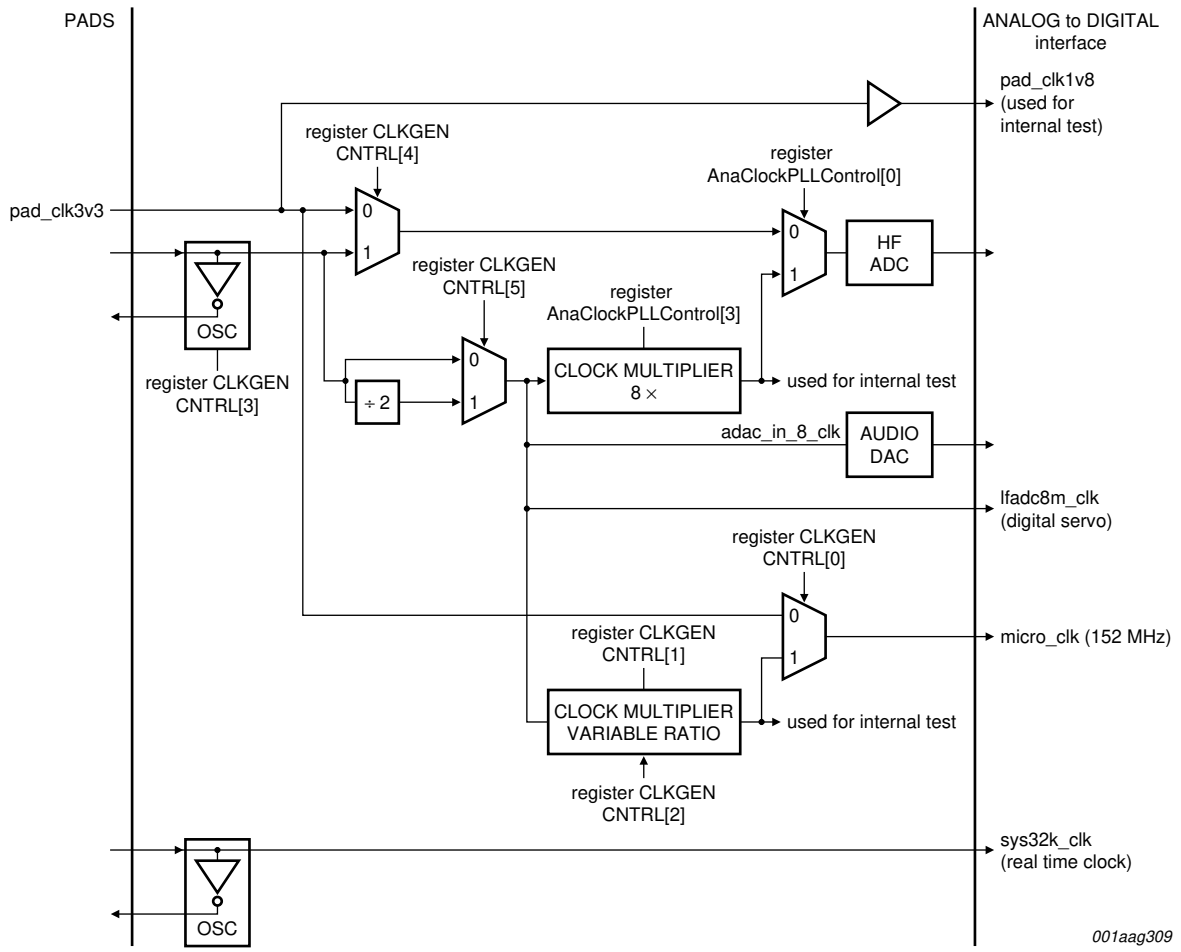


Fig 5. Analog clock generation

The SAF784x consists of two analog phase-locked loops. The 67 MHz PLL is dedicated to the channel decoder. The 152 MHz PLL is dedicated to the remaining functionality. The clock strategy for the SAF784x is intended to address areas that are prone to noise effects

that can decrease the quality of audio. The clocks related to audio DAC and LF ADC are generated directly from the analog signal, instead of being derived from high frequency PLLs. The clocking strategy for the digital core is shown in Figure 9.

6.3 General purpose analog inputs

The four general purpose ADC inputs, GPIO0 (pin 33), GPIO1 (pin 34), GPIO2 (pin 35), and GPIO3 (pin 36), can be used for giving the ARM microprocessor access to external analog sources, such as monitoring temperature and to provide simple resistor-ladder keypad functionality. These inputs use an additional pair of sigma-delta ADCs identical to those used for the LF diode inputs.

The general purpose analog inputs have separate interrupt request lines and use address space in the servo registers for storing the converted digital values. The output of the general purpose ADCs are low-pass filtered and can have fine-offset compensation added before being passed to a decimation filter. The digital values output from the decimation filter are then captured in the servo registers with a resolution of 10 bits per channel.

There are only two ADCs for general purpose application and so each ADC is multiplexed between two inputs: ADC1 between GPIO0 and GPIO2, and ADC2 between GPIO1 and GPIO3. GPIO2 and GPIO3 inputs are selected by signal AuxControlandGPADC.

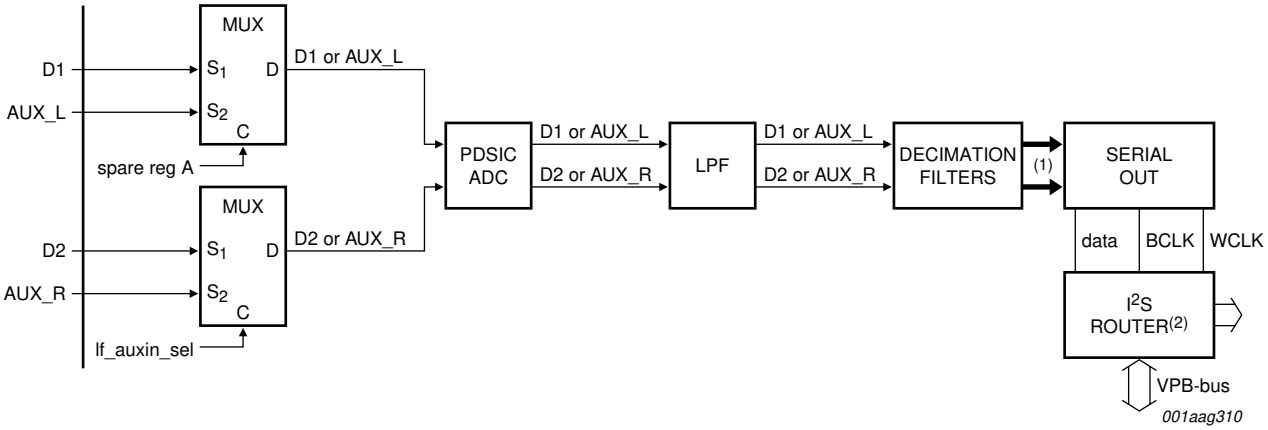
6.4 Auxiliary analog inputs

Analog inputs, AUX_L and AUX_R, are available, and have sufficient resolution, for the input of external audio sources, such as allowing ARM access to an external audio source for sound processing algorithms. This allows audio processing of external audio sources via the AUX pins, whilst simultaneously using the general purpose inputs for keyboard and temperature inputs.

Since these two inputs share one pair of the LF sigma-delta ADCs used in the LF path (for inputs D1 and D2) a multiplexer is used to control the data source into the ADCs. Therefore, D1 and D2 cannot be used at the same time as AUX_L and AUX_R. This path is designed for a tuner input where the THD specification is ~0.3 % and the S/N is < 60 dB. These performance values are lower than when the normal CD audio path is used i.e. S/N > 80 dB and THD < 0.01 %.

The audio data is converted to a pulse-density modulated digital stream for both input channels. This data is then low-pass filtered and decimated to produce 10-bit representations of the analog inputs.

The auxiliary inputs differ from the general purpose analog inputs because the parallel data is converted to an I^2S format stream and then sent to the I^2S handler block to make the data available to the ARM microprocessor. The I^2S handler contains a 12-deep data FIFO which allows the ARM microprocessor to service the audio data with a lower priority than it would need if it were directly registered; see Figure 6.



(1) 10-bit samples of AUX_L and AUX_R expanded to 16 bits by adding 6 LSBs.

(2) I^2S router block used to route I^2S to audio DAC or pins.

Fig 6. Auxiliary analog inputs block diagram

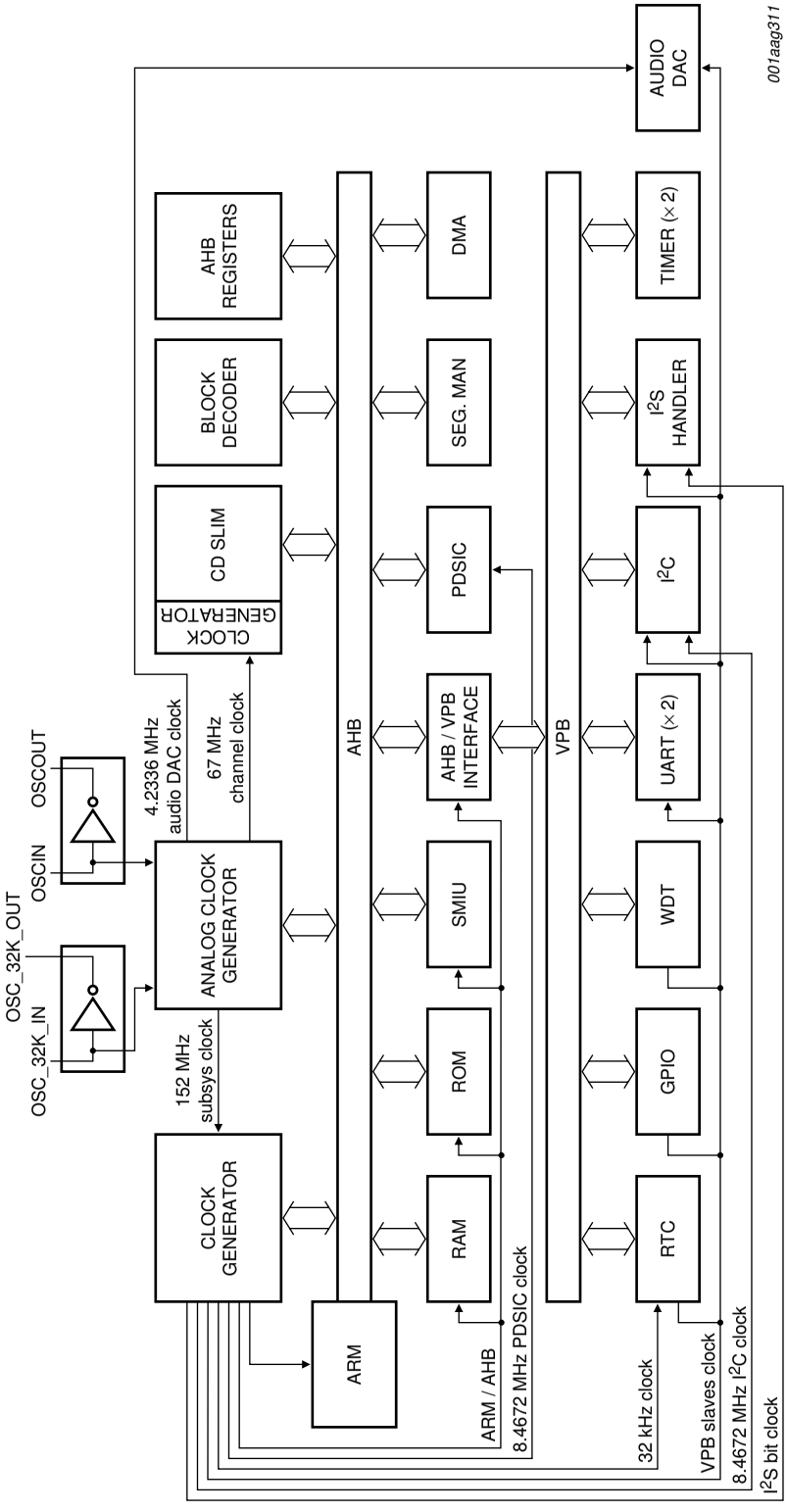


Fig 7. Clocking top-level block diagram

6.5 Channel decoder

6.5.1 Features

The channel decoder in the SAF784x is derived from the design used in the SAA7817HL DVD decoder IC. The design has been optimized for CD decode functionality (EFM and demodulation is removed) and has the following features:

- One-channel interface to the on-chip 6-bit 67 MHz ADC
- Signal conditioning logic with high-pass filter, DC-offset cancellation (AOC) and AGC logic
- HF defect detection circuitry with automatic hold of AGC, AOC, HPF, PLL and slicer on defect detection
- Digital equalizer, noise filter, PLL and slicer
- Run Length 2 (RL2) push back mechanism
- EFM demodulator with sync interpolation
- CD text and subcode Q-channel extraction blocks with software interface via registers
- Decoding, de-interleaving and Reed-Solomon error correction according to CD CIRC standards
- On-chip de-interleaving SRAM memory
- Audio processing back end with interpolate/hold, mute, kill and silence detect logic, de-emphasis and 4× upsample filter
- Two data output interfaces: I^2S and EBU
- One serial subcode output interface (V4)
- Motor control for CLV (locked-on EFM) or CAV (locked-on tacho) or open loop or software-controlled regulation with one or two motor pins
- On-board tacho measurement with one or three Hall sensor inputs (T1 to T3), that provides frequency input for motor loop; the sensor inputs are shared with GPIO pins
- 8-bit register map, with AHB slave interface
- An interrupt output with associated interrupt, status and interrupt enable registers for full interrupt-driven operation
- Debug information available via Meas1 (CL1, pin 97) and pin CFLG (pin 95) and parallel debug bus

6.5.2 Block diagram

The incoming diode signals are first added and processed in the analog front end to create a normal RF (HF) signal and then converted to digital by the ADC. This signal is then resampled from the ADC clock to the system clock domain via the integrate-and-dump block. Offset and gain on the RF signal is removed via the AGC/AOC loop (via the analog front end). Any remaining offset which is not removed by the analog front end can be removed via the digital HPF. The RF signal is then sliced by the bit detector, clock recovery is done by a full digital PLL with noise filter, equalizer and sample-rate convertor. A defect detector allows AGC, AOC, HPF, slicer and PLL to be held during black or white dots. At this point in the data path, RF samples are converted into a bit stream. The RL2 push back avoids RL3s in the RF being accidently translated into RL1 or RL2 in the bit stream. The channel bit stream is demodulated in to bytes by the EFM demodulator. Q-channel subcode and CD-text information is extracted via the Q-subcode

and CD-text decoder, available for readout through the sub-CPU interface. The main data stream is error-corrected by the ERCO, while the memory processor takes care of the CIRC de-interleaving and buffering of data in a FIFO. At the back end of the channel decoder, corrupted audio samples can be interpolated and held, while a burst of errors can trigger the mute block. Detection of digital silence can be used to kill the internal or external audio DAC. Pre-emphasis on the audio disc can be removed via the de-emphasis filter, and the data can be 4× upsampled before it is sent to the audio DAC. CD data is output via the I^2S and/or the EBU outputs. Motor control can be frequency-regulated to the incoming RF bit rate, with additional phase regulation by FIFO filling, or it can be fully controlled via software. This method guarantees CLV support. A tacho measurement block is also available. The motor can also be regulated by the tacho frequency which allows possible CAV support.

Debug information is available via registers, via the dedicated serial lines Meas1 and Cflg.

The ARM AHB address of registers that control specific logic are shown next to each functional block in Figure 8.

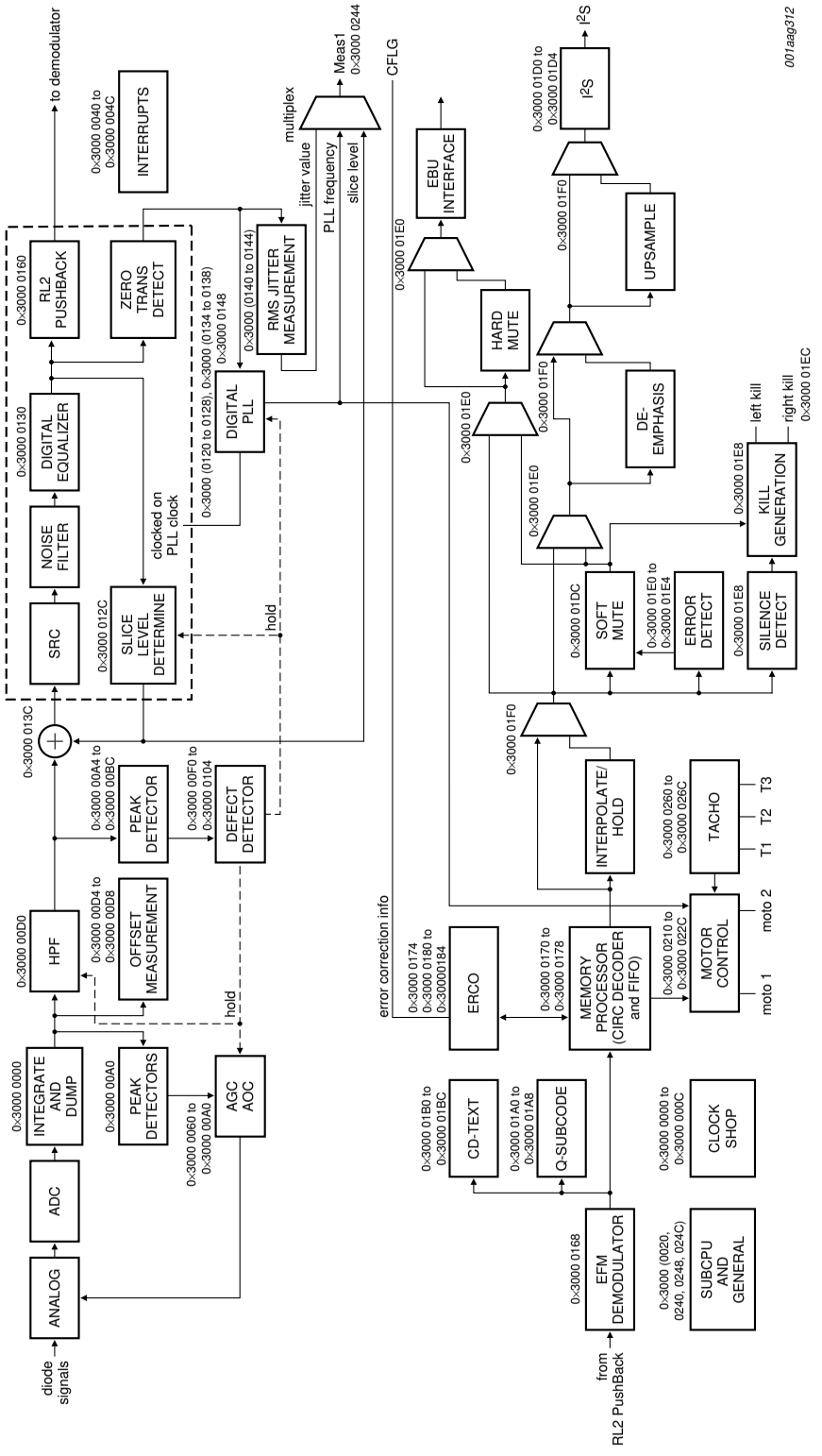
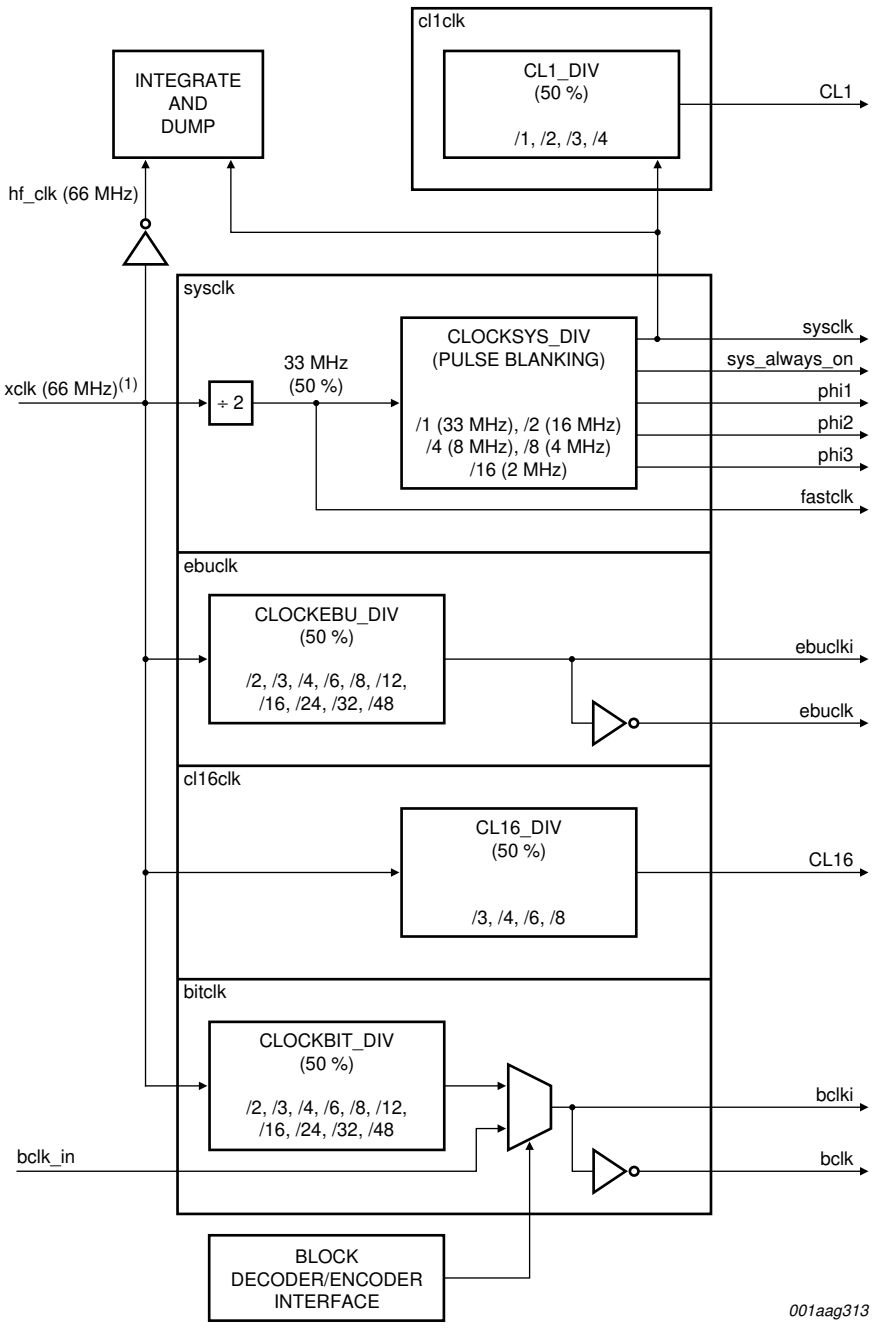


Fig 8. Channel decoder top-level block diagram

6.5.3 Clock control



(1) 66 MHz is an approximate value.

Fig 9. Clock control block diagram

The clock control block defines the clock frequencies for four clock domains.

- xclk: most internal clocks are derived from the crystal clock. This clock is the output of the clock multiplier in the analog part and has a fixed frequency of 67.7376 MHz = 8.4672 MHz (f_{xtal}) × 8. If a 16 MHz crystal is used, the crystal clock is divided by 2 inside the analog block. Crystal selection is done via AnalPLLControl bit SEL16.
- sysclk domain: the system clock, or its derivatives, runs the main part of the internal channel decoder. The sysclk is derived from xclk divided by 2 (50 % duty cycle) and can be further divided down via register SysclockConfig bit SYSDIV. This register also allows the majority of clocks to be powered down (for Sleep mode). The choice of the sysclk frequency $f_{clk(sys)}$ in an application is determined by the expected input bit rate f_{bit} of the RF bit stream. The relationship between this incoming bit stream frequency and the system clock frequency $f_{clk(sys)}$ is expressed by the ratio $f_{bit} / f_{clk(sys)}$. There are two limiting factors:
  - The HF-PLL operating range is between $0.25 \times (f_{bit} / f_{clk(sys)})$ and $2 \times (f_{bit} / f_{clk(sys)})$
  - The decoder and error corrector throughput rate is limited to $1.7 \times (f_{bit} / f_{clk(sys)})$

  This brings the constraint to $0.25 < f_{bit} / f_{clk(sys)} < 1.7$.
- bitclk domain: runs the I²S back-end logic. The bit clock (bitclk) is also output as part of the I²S interface. In audio slave mode this clock must be programmed to be exactly 44100 Hz × 2 × 16/24/32 (depending on I²S mode), to get a 1× data rate to the audio DAC. In master mode with gated bitclk, the bitclk must be programmed to be at a higher rate than the outgoing bit rate required for the disc speed, to avoid FIFO overflow in the decoder. For example, at N = 1, the incoming RF bit rate = 4.3218 MHz, which corresponds to an output bit rate of 1.4112 MHz. This means that the bitclk frequency is above 1.4112 MHz and is high enough when I²S-16 is chosen, while I²S-32 requires the bitclk to be at least 2.8224 MHz. The bitclk division is selected via register BitClockConfig. Also, bitclk gating can be enabled via the same register.
- ebuclk domain: runs the EBU back end. The EBU (or S/PDIF) interface is only enabled during audio slave mode. The ebuclk needs to be exactly 44100 Hz × 64 = 2.8224 MHz for 1× operation. The ebuclk division is selected via register EBUClockConfig.

  The following clocks are also controlled by the clock control block:
  - The hf_clk is fixed at 67.7376 MHz, and is used to clock-in the samples from the ADC, which is clocked by the xclk with the same clock frequency
  - The bclk_in is the incoming I²S bit clock, which is used when I²S is programmed to receive bclk rather than transmitting it (programmed via register I2SConfig)
  - The cl1clk can be used to monitor the Cflg and Meas1 debug lines. The frequency can be programmed via register CLClockConfig
  - The cl16clk can be used to clock an external audio DAC or audio filter IC. The frequency can be programmed via register CLClockConfig

6.5.4 Decoder-ARM microprocessor interface

The decoder core is internally connected to the ARM core via the AHB interface for register access to the decoder internal configuration registers.

6.5.4.1 Programming interface

Decoder registers are programmed through the AHB interface. The programming interface is not fully described in this document.

For the application, it should be noted that the interface supports 32-bit registers, while the decoder only contains 8-bit registers. Therefore, the decoder registers are treated as 32-bit registers of which the 24 MSBs are not used.

The register address map occupied by the decoder goes from relative address 0x3000 0000 to address 0x3000 0374, and can be split into two parts:

0x3000 0000 - 0x3000 024C: the decoder's own registers - used to configure the channel decoder, and the functionality they control is described in detail in this section.

0x3000 02A0 - 0x3000 0374: the decoder immigrant registers - used to control parts of the SAF784x that do not have their own AHB interface (they are not used to control the decoder channel decoder).

6.5.4.2 Interrupt strategy

The channel decoder contains two interrupt status registers: InterruptStatus1 contains all interrupts that operate as set/reset latches (set by hardware, reset by reading from the register). InterruptStatus2 contains all interrupts that operate as feed-throughs (set by hardware, reset by hardware or by accessing other registers).

Each interrupt bit can be enabled or disabled separately by writing to its corresponding enable bit in the InterruptEnable1 and InterruptEnable2 registers. If one or several interrupt bits are set and at least one is enabled, the interrupt line of the decoder to the microcontroller will go active (LOW). If an interrupt bit is disabled (enable bit turned off), it is prevented from activating the interrupt line to the microcontroller. However, this mode allows the interrupt to be processed if the status register is polled instead of interrupt handling by the microcontroller.

6.5.5 EFM bit detection and demodulation

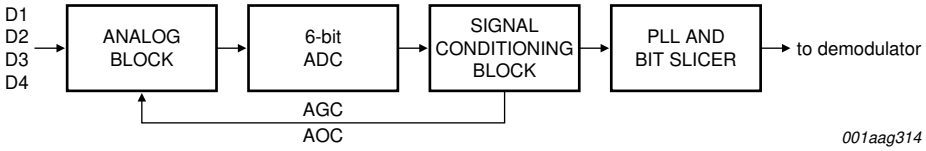


Fig 10. Bit recovery block diagram

A block diagram of the bit recovery is shown in Figure 10.

The HF signal comprises the four diode inputs inside the analog block. It is pre-processed (LPF, HPF, offset removal and gain adjustment) and then sampled by a 6-bit ADC.

On the sampled HF, bit recovery is done by means of a full digital PLL and slicer.

Before the sampled signal enters the PLL section, it is pre-processed by a signal conditioning block. This consists of an integrate-and-dump block, a high-pass filter and logic available for gain control and offset control on the RF signal in the analog section.

For good playability on defects, a defect detector puts the PLL, the slicer, the AGC, the offset cancellation and the high-pass filter into hold during defects.

The detected bits are then sent to the demodulator for sync extraction and EFM demodulation. For playing on damaged or out-of-specification discs, flywheels are in place to make the sync extraction more robust.

6.5.5.1 Signal conditioning

This device has a number of blocks which process the incoming 6-bit HF signal.

- Integrate-and-dump block to adapt the frequency of the ADC to the system clock
- Peak detection logic for amplitude measurement
- Peak detection logic for DC-offset measurement
- Digital high-pass filter with configurable cut-off frequency
- DC and gain control logic for on-board variable gain and offset control (in the analog section)
- A defect detector

All blocks can be configured under microprocessor control.

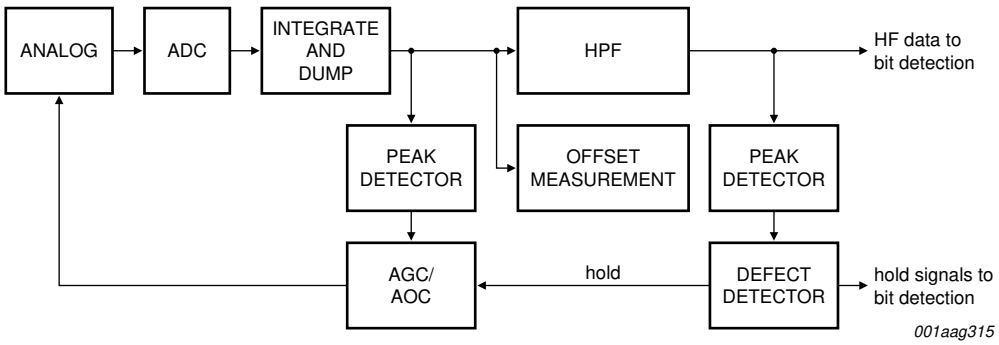


Fig 11. Signal conditioning block diagram

Integrate-and-dump block: the ADC delivers one sample every xclk period (= one sample every hf_clk period). The sample rate needs to be adapted from this xclk rate to the lower sysclk rate. For more information on sysclk speed, see Section 6.5.3 on page 19. The integrate-and-dump block converts the incoming samples at the hf_clk frequency into a stream of one sample per sysclk period. It converts an average of a number of samples to achieve this. If the division factor for the system clock is /2, /4, /8, /16, /32, an average of 2, 4, 8, 16 or 32 incoming samples respectively, is taken and passed further. This results in a gain in the number of effective bits of the A-D conversion.

High-pass filter: A 1st-order IIR high-pass filter with a variable 3 dB point is implemented to filter out the remaining DC jump-on defects. Most of these defects will have been filtered by the analog HPF. The cut-off frequency of the digital high-pass filter can be changed on-the-fly, by writing to register HighPassFiltCont.

It is possible to reset the state of the high-pass filter via bit 6 of register HighPassFiltCont. The input and the output of the high-pass filter are 8-bits wide.

The high-pass filter is implemented in a ‘1 minus low pass’ structure. It is possible to hold the low-pass filter on defects. For more information, see Section “Defect detector” on page 26.

The high-pass filter works on the system clock. Its bandwidth is also proportional to the sysclk.

A formula for approximating the cut-off frequency (f_c), of the high-pass filter is:

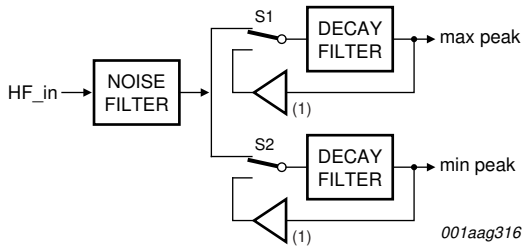
$$f_{c,HPF} = \frac{HPSet[5:0]}{2\pi \times 2^{11}} \times f_{clk(sys)} \quad (1)$$

Peak Detectors: The signal conditioning block has two types of peak detector:

- peak detector with decay filter: works on an immediate attack/slow-decay basis, and is used for measuring peaks, amplitude and offset, read by software which sends peak information to the defect detector.
- peak detector based on window: works on the principle of detecting maximum and minimum peaks within a window, and is used for the AGC and AOC control logic.

Both peak detectors monitor the RF after it has passed an optional noise filter. This noise filter is a LPF with a programmable high cut-off frequency. This bandwidth is programmed via register PDBandwidth bit NOISEFILTERBW for the noise filter before the peak detectors of AGC/AOC and measurement read back. The defect detector peak detector has its own noise filter which is programmed via register DefectDetPeakBW bit NOISEFILTERBW.

Peak detector with decay filter: The functional schematic of this peak detector is shown in Figure 12.



(1) Determines the time-constant coefficient.

Fig 12. Peak detection block with decay filter

The maximum and minimum peaks of the incoming signal are measured at the inputs of switches S1 and S2 respectively. The maximum and minimum peak signal paths both have a decay filter with a long time-constant and matching bandwidth. The maximum peak decay filter responds to the smallest value possible. The decay filter for the minimum peak responds to the largest value possible.

The decay bandwidth of the measurement readback decay filter is controlled by register PDBandwidth bit DECAYBW, the bandwidth of the defect detector is controlled via register DefectDetPeakBW bit DECAYBW.

The following settings of the decay filters are possible: $C = 1 - 2^{-m}$, for m = 6 to 21, where

C = time-constant coefficient, m = DecayBW[3:0] + 6.

The bandwidths and corresponding time-constant (t) of the decay filter are shown in Table 4, when the system clock frequency $f_{clk(sys)}$ is 10 MHz.

Table 4. Decay filter time-constants at $f_{clk(sys)}$ = 10 MHz

m	t	m	t	m	t	m	t
6	6.35 µs	10	102.4 µs	14	1.64 ms	18	26.21 ms
7	12.75 µs	11	204.7 µs	15	3.28 ms	19	52.43 ms
8	25.55 µs	12	409.6 µs	16	6.55 ms	20	104.8 ms
9	51.15 µs	13	819.2 µs	17	13.11 ms	21	209.7 ms

Peak detector based on window: The functional schematic of this peak detection is shown in Figure 13.

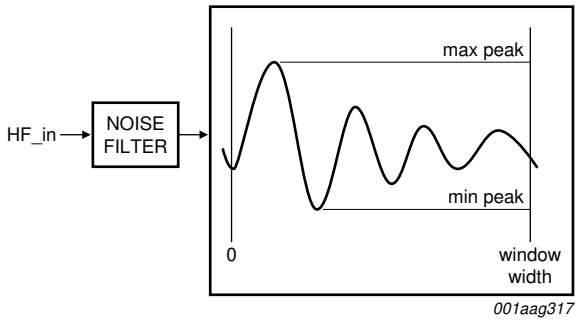


Fig 13. Peak detection block with window

The minimum and maximum peaks of the incoming signal are measured during a programmable window period. The highest and lowest sample within this window are used to update maximum and minimum peaks.

The window width of the measurement is controlled via register AGCAOCControl bit PDMEASWINDOW.

AGC and AOC control block: The AGC control block controls the RF amplitude at the input of the ADC by controlling the gain of an on-chip analog gain amplifier. The AOC control block controls the RF offset at the input of the ADC by adding or subtracting the offset just before the ADC. Both AGC and AOC loops are built up in the same manner and are shown in Figure 14 in their relative position within the signal conditioning block.

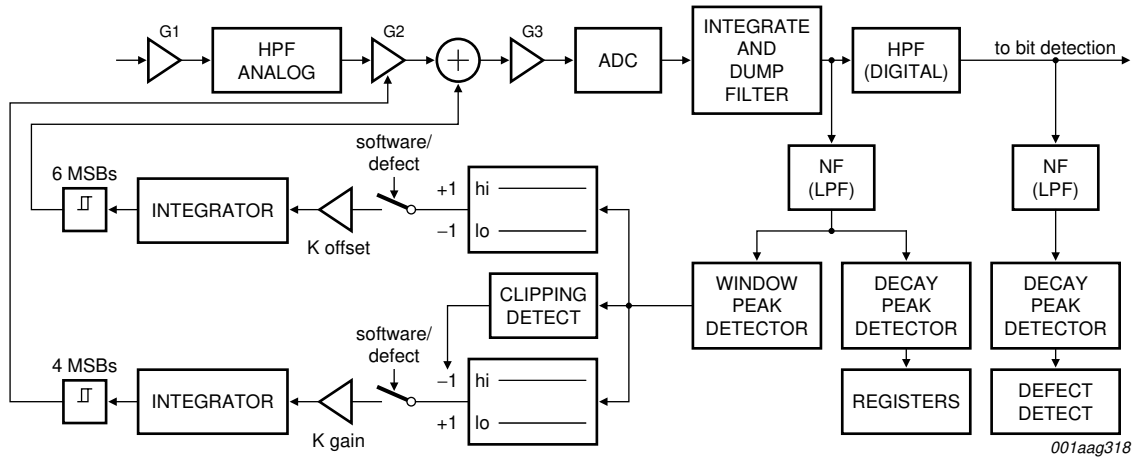


Fig 14. AGC and AOC loops

The maximum and minimum peaks on the envelope of the RF signal after the ADC are first measured via a noise filter and the window peak detector (see Section "Peak Detectors" on page 23. The amplitude is then calculated as maxpeak – minpeak, and the offset as (maxpeak + minpeak) / 2.

For tuning the loops, it is possible to read back the HFMaxPeak, HFMinPeak, HFAmplitude and HFOffset, as measured from their registers by the decay peak detector.

AGC control: The RF amplitude at the ADC input can be changed with two gain amplifiers in the analog part: G1 (fixed) and G2 (dynamic). G1 has a gain range from 0 dB to 24 dB in 16 steps of 1.6 dB, while G2 has a range from 0 dB to 12 dB in 16 steps of 0.8 dB. Both gains can be programmed via register AGCGain. G1 will stay fixed, while G2 can be regulated by hardware when the AGC is turned on.

The AGC will regulate the gain such that the measured amplitude stays between a programmed upper threshold (AGCThrHi) and lower threshold (AGCThrLo). If the amplitude is smaller, gain will increase; if the amplitude is too large, gain will decrease. When clipping is detected on either one or both sides, the gain will decrease. These gain changes are not sent to the analog gain amplifier directly but are integrated over time. Only if, on average, a gain increase or decrease is requested, will this result in a real gain increase or decrease of the amplifier. This can also be read back via register AGCGain. The AGC, together with the noise filter on the peak detector, prevents RF noise causing over-sensitive gain regulation. To further reduce sensitive behavior, a hysteresis window with a width of one gain step is added between the integrator and amplifier G2. The bandwidth of the gain loop determines how fast it reacts to fingerprints and scratches; it is programmed via register AGCIntegBW. It is also possible to limit the range of G2 by programming a maximum and minimum boundary by register AGCGainBound.

AOC control: Most of the RF offset at the ADC input will be removed by the analog HPF (1st-order HPF with 3 dB point around 3.6 kHz). The remaining offset (mainly introduced by the analog front end), can be removed by adding or subtracting a fixed offset in the analog part. This offset subtraction/addition has a range of 32 steps in each direction, with approximately 1.4 LSBs per step (referenced to the RF ADC). This leads to a full