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SIEMENS

Data Communications ICs

High-Level Serial Communication Controller Extended (HSCX)
SAB 82525; SAB 82526
SAF 82525; SAF 82526

User’s Manual 10.94

SAB 82525; SAF 82525; SAB 82526; SAF 82526 Revision History: 10.94	
Previous Releases: 01.92	
Page	Subjects (changes since last revision)
	Update

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about "**Processing Guidelines**" and "**Quality Assurance**" for ICs, see our "**Product Overview**".

Edition 10.94

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The SAB 82525 is a High-Level Serial Communication Controller compatible to the SAB 82520 HSCC with extended features and functionality (HSCX).

The SAB 82526 is pin and software compatible to the SAB 82525, realizing one HDLC channel (channel B).

The HSCX has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

Due to its 8-bit demultiplexed adaptive bus interface it fits perfectly into every Siemens/Intel or Motorola 8- or 16-bit microcontroller or microprocessor system. The data through-put from/to system memory is optimized transferring blocks of data (usually 32 bytes) by means of DMA or interrupt request. Together with the storing capacity of up to 64 bytes in on-chip FIFO's, the serial interfaces are effectively decoupled from the system bus which drastically reduces the dynamic load and reaction time of the CPU.

The HSCX directly supports the X.25 LAPB, the ISDN LAPD, and SDLC (normal response mode) protocols and is capable of handling a large set of layer-2 protocol functions independently from the host processor.

Furthermore, the HSCX opens a wide area for applications which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications) by its programmable telecom-specific features.

The HSCX is fabricated using Siemens advanced ACMOS 3 technology and available in a P-LCC-44 pin package.

The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as

– Flag insertion and detection,
– Bit stuffing,
– CRC generation and checking,
– Address field recognition.

Associated with each serial channel is a set of independent command and status registers (SP-REG) and 64-byte deep FIFO's for transmit and receive direction.

DMA capability has been added to the HSCX by means of a 4-channel DMA interface (SAB 82525) with one DMA request line for each transmitter and receiver of both channels.

General

- Advanced CMOS technology
- Low power consumption: active 25 mW at 4 MHz
  standby 4 mW

SIEMENS

SAB 82525
SAB 82526
SAF 82525
SAF 82526

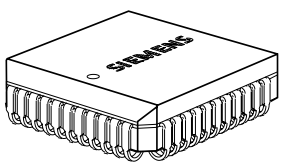
High-Level Serial Communications Controller Extended (HSCX)

Preliminary Data **CMOS IC**

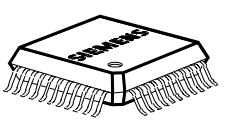
1 Features

Serial Interface

- Two independent full-duplex HDLC channels (SAB 82526: one channel)
  - On chip clock generation or external clock source
  - On chip DPLL for clock recovery for each channel
  - Two independent baudrate generators (SAB 82526: one baudrate generator)
  - Independent time-slot assignment for each channel with programmable time-slot length (1-256 bit)
- Different modes of data encoding
- Modem control lines (RTS, CTS, CD)
- Support of bus configuration by collision resolution
- Programmable bit inversion
- Transparent receive/transmit of data bytes without HDLC framing
- Continuous transmission of 1 to 32 bytes possible
- Data rate up to 4 Mbit/s



P-LCC-44-1



P-MQFP-44-2

Type	Ordering Code	Package
SAB 82525 N	Q67100-H6486	P-LCC-44-1 (SMD)
SAB 82526 N	Q67100-H6512	P-LCC-44-1 (SMD)
SAF 82525 N	Q67100-H6504	P-LCC-44-1 (SMD)
SAF 82526 N	Q67100-H6511	P-LCC-44-1 (SMD)
SAB 82525 H	Q67101-H6482	P-MQFP-44-2 (SMD)

Features (cont'd)

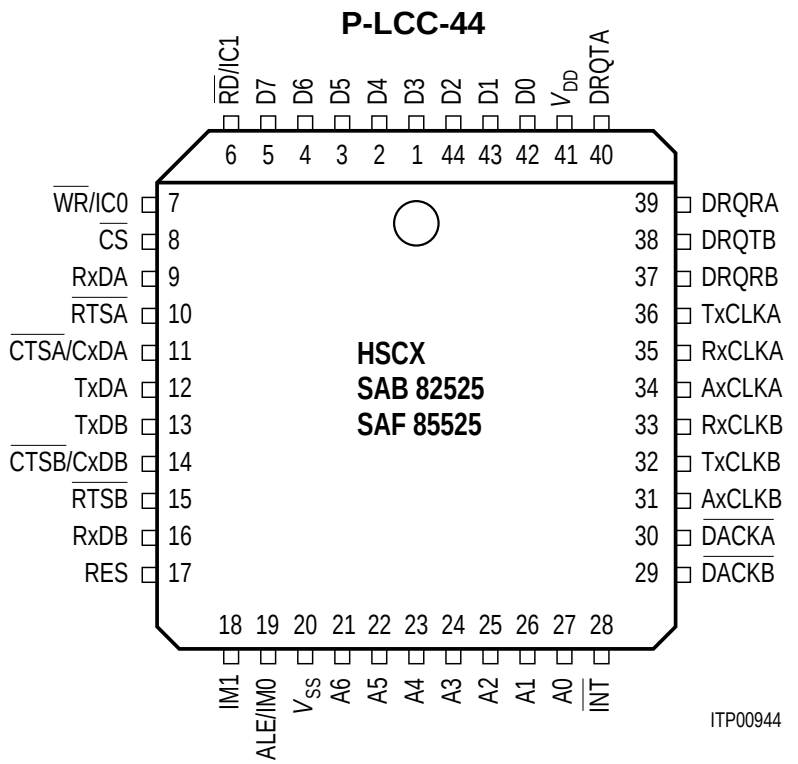
Protocol Support

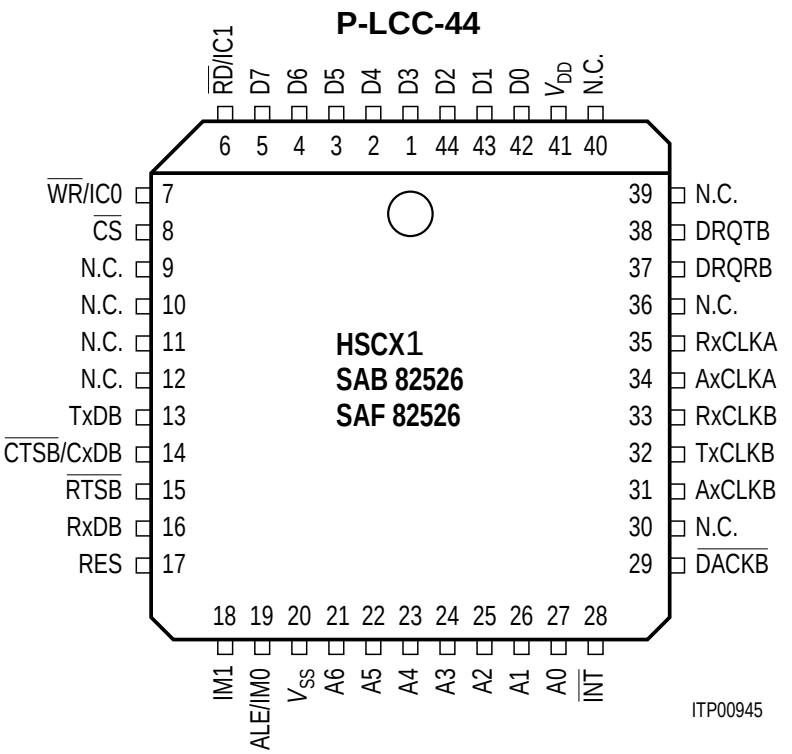
- Various types of protocol support depending on operating mode
  - Auto-mode
  - Non-auto mode
  - Transparent mode
- Handling of bit oriented functions in all modes
- Support of LAPB/LAPD/SDLC/HDLC protocol in auto-mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

µP Interface

- 64 byte FIFO's per channel and direction
- Storage capacity of up to 17 short frames in receive direction
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- 8-bit demultiplexed or multiplexed bus interface
- Intel or Motorola type µP interface

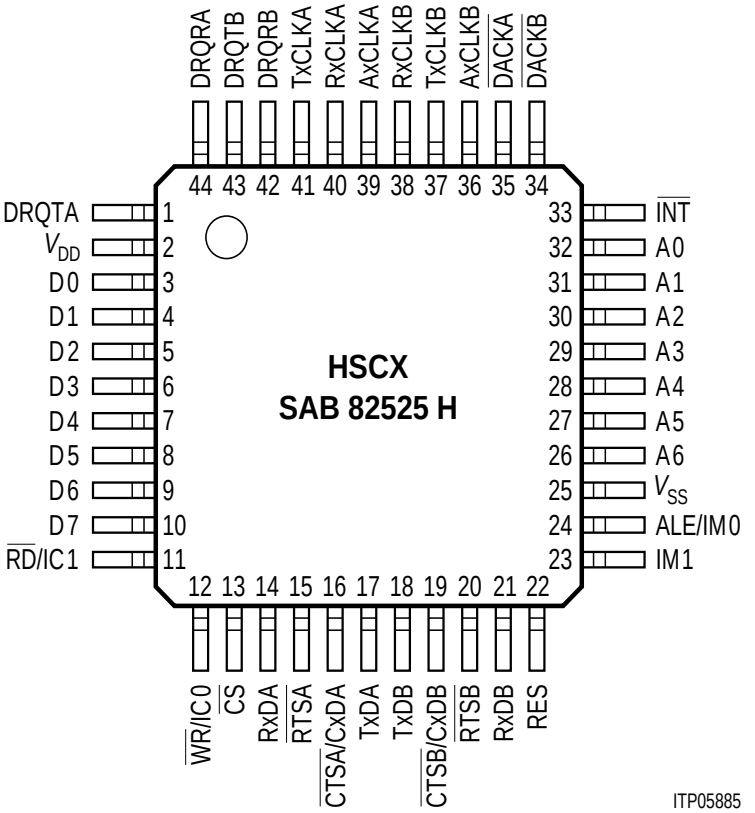
Pin Configurations
(top view)





Pin Configurations
(top view)

P-MQFP-44-2



1.1 Pin Definitions and Functions

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
42 43 44 1 2 3 4 5	3 4 5 6 7 8 9 10	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Data Bus** The data bus lines are bidirectional threestate lines which interface with the system's data bus. These lines carry data and command/status to and from the HSCX.
6	11	$\overline{RD}$/IC1	I	**Read**, Intel bus mode, IM1 connected to low This signal indicates a read operation. When the HSCX is selected via $\overline{CS}$ the read signal enables the bus drivers to put data from an internal register addressed via A0-A6 on the data bus. When the HSCX is selected for DMA transfers via DACK, the RD signal enables the bus driver to put data from the respective receive FIFO on the data bus. Inputs to A0-A6 are ignored. **Input Control 1**, Motorola bus mode IM1 connected to high. If Motorola bus mode has been selected this pin serves either as E = Enable, active high (IM0 tied to low) or DS = Data Strobe, active low (IM0 tied to high) input (depending on the selection via IM0) to control read/ write operations.
7	12	$\overline{WR}$/IC0	I	**Write**, Intel bus mode This signal indicates a write operation. When $\overline{CS}$ is active the HSCX loads an internal register with data provided via the data bus. When DACK is active for DMA transfers the HSCX loads data from the data bus on the top of the respective transmit FIFO. **Input Control** Motorola bus mode In Motorola bus mode, this pin serves as the R/$\overline{W}$ input to distinguish between read or write operations.
8	13	$\overline{CS}$	I	**Chip Select** A low signal selects the HSCX for a read/write operation.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
9 16	14 21	RXDA RXDB	I	**Receive Data** (channel A/channel B) Serial data is received on these pins at standard TTL or CMOS levels.
10 15	15 20	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O	**Request to Send** (channel A/channel B) When the RTS bit in the mode register is set, the RTS signal goes low. When the RTS is reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In a bus configuration, this pin can be programmed via CCR2 to: – go low during the actual transmission of a frame shifted by one clock period, excluding collision bits – go low during the reception of a data frame – stay always high (RTS disabled).
11 14	16 19	$\overline{\text{CTSA}}$/ CXDA $\overline{\text{CTSB}}$/ CXDB	I	**Clear to Send** (channel A/channel B) A low on the CTS inputs enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTS pin (programmable feature). If no "Clear To Send" function is required, the CTS inputs can be connected directly to V_{SS}. **Collision Data** (channel A/channel B) In a bus configuration, the external serial bus must be connected to the respective C × D pin for collision detection.
12 13	17 18	TXDA TXDB	O	**Transmit Data** (channel A/channel B) Transmit data is shifted out via these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.
17	22	RES	I	**RESET** A high signal on this input forces the HSCX into the reset state. The HSCX is in power-up mode during reset and in power-down mode after reset. The minimum pulse width is 1.8 µs.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
18	23	IM1	I	**Input Mode 1** Connecting this pin to either V_{SS} or V_{DD} the bus interface can be adapted to either Siemens/Intel or Motorola environment. IM1 = LOW: Intel bus mode IM1 = HIGH: Motorola bus mode
19	24	ALE/ IM0	I	**Address Latch Enable** (Intel bus mode) A high on this line indicates an address on the external address/data bus, which will select one of the HSCX's internal registers. The address is latched by the HSCX with the falling edge of ALE. This allows the HSCX to be directly connected to a CPU with multiplexed address/data bus compatible to SAB 82520 HSCC. The address input pins A0-A6 must be externally connected to the data bus pins (D0-D6 for 8-bit CPU's, D1-D7 for 16-bit CPU's, i.e. multiply all internal register addresses by 2). This pin should be connected to high for a de-multiplexed bus. **Input Mode 0**, Motorola bus mode In Motorola Bus Mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).
20	25	V_{SS}	I	**Ground**
27 26 25 24 23 22 21	32 31 30 29 28 27 26	A0 A1 A2 A3 A4 A5 A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write. They are usually connected at A0-A6 in 8-bit systems or at A1-A7 in 16-bit systems.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
28	33	$\overline{\text{INT}}$	oD	**Interrupt Request** The signal is activated, when the HSCX requests an interrupt. The CPU may determine the particular source and cause of the interrupt by reading the HSCX's interrupt status registers. (ISTA, EXIR). $\overline{\text{INT}}$ is an open drain output, thus the interrupt requests outputs of several HSCX's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull-up resistor.
30 29	35 34	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/channel B) When low, this input signal from the DMA controller notifies, the HSCX, that the requested DMA cycle controlled via DRQxx (pins 37–40) is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with $\overline{\text{RD}}$, if DMA has been requested from the receiver, or with $\overline{\text{WR}}$, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If $\overline{\text{DACKn}}$ is active, the input on pins A0–A6 is ignored and the FIFOs are implicitly selected. If the $\overline{\text{DACKn}}$ signals are not used, these pins must be connected to V_{DD}.
34 31	39 36	AxCLK A AxCLK B	I	**Alternative Clock** (channel A/channel B) These pins realize several input functions. Depending on the selected clock mode, they may supply either a – CD (= Carrier Detect) modem control or general purpose input. This pin can be programmed to functions as receiver enable if the "auto start" feature is selected (CAS bit in XBCH set). The state at this pin can be read from VSTR register, – or a receive strobe signal (clock mode 1) – or a frame synchronization signal in time-slot oriented operation mode (clock mode 5) – or, together with RxCLK, a crystal connection for the internal oscillator (clock mode 4, 6, 7, AxCLK A only).

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
36 32	41 37	TxCLK A TxCLK B	I/O	**Transmit Clock** (channel A/channel B) The functions of these pins depend on the programmed clock mode, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either – the transmit clock for the respective channel (clock mode 0, 2, 6), – or a transmit strobe signal (clock mode 1). Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the – transmit clock of the respective channel which is generated either ● from the baudrate generator (clock mode 2, 6; TSS bit in CCR2 set), ● or from the DPLL circuit (clock mode 3, 7), ● or from the crystal oscillator (clock mode 4) – or a tristate control signal indicating the programmed transmit time-slot (clock mode 5).
35 33	40 38	RxCLK A RxCLK B	I	**Receive Clock** (channel A/channel B) The functions of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either – the receive clock (clock mode 0) – or the receive and transmit clock (clock mode 1, 5) – or the clock for the baudrate generator (clock mode 2, 3), – or a crystal connection for the internal oscillator (clock mode 4,6,7, RxCLK A/B together with AxCLK A)
39 37	44 42	DRQRA DRQRB	O	**DMA Request Receiver** (channel A/channel B) The receiver of the HSCX requests a DMA data transfer by activating this line. The DRQRn remains high as long as the receive FIFO requires data transfers, thus always blocks of data (32, 16, 8 or 4 bytes) are transferred. DRQRn is deactivated immediately following the falling edge of the last read cycle.

Pin Definitions and Functions (cont'd)

Pin No. P-LCC	Pin No. P-MQFP	Symbol	Input (I) Output (O)	Function
40 38	1 43	DRQTA DRQTB	O	**DMA Request Transmitter** (channel A/channel B) The transmitter of the HSCX requests a DMA data transfer by activating this line. The DRQTn remains high as long as the transmit FIFO requires data transfers. The amount of data bytes to be transferred from system memory to the HSCX (= byte count) must be written first to the XBCH, XBCL registers. Always blocks of data (n x 32 bytes + REST, n = 0, 1,…) are transferred till the byte count is reached. DRQTn is deactivated immediately following the falling edge of the last $\overline{WR}$ cycle.
41	2	V_{DD}	I	Power supply + 5 V.

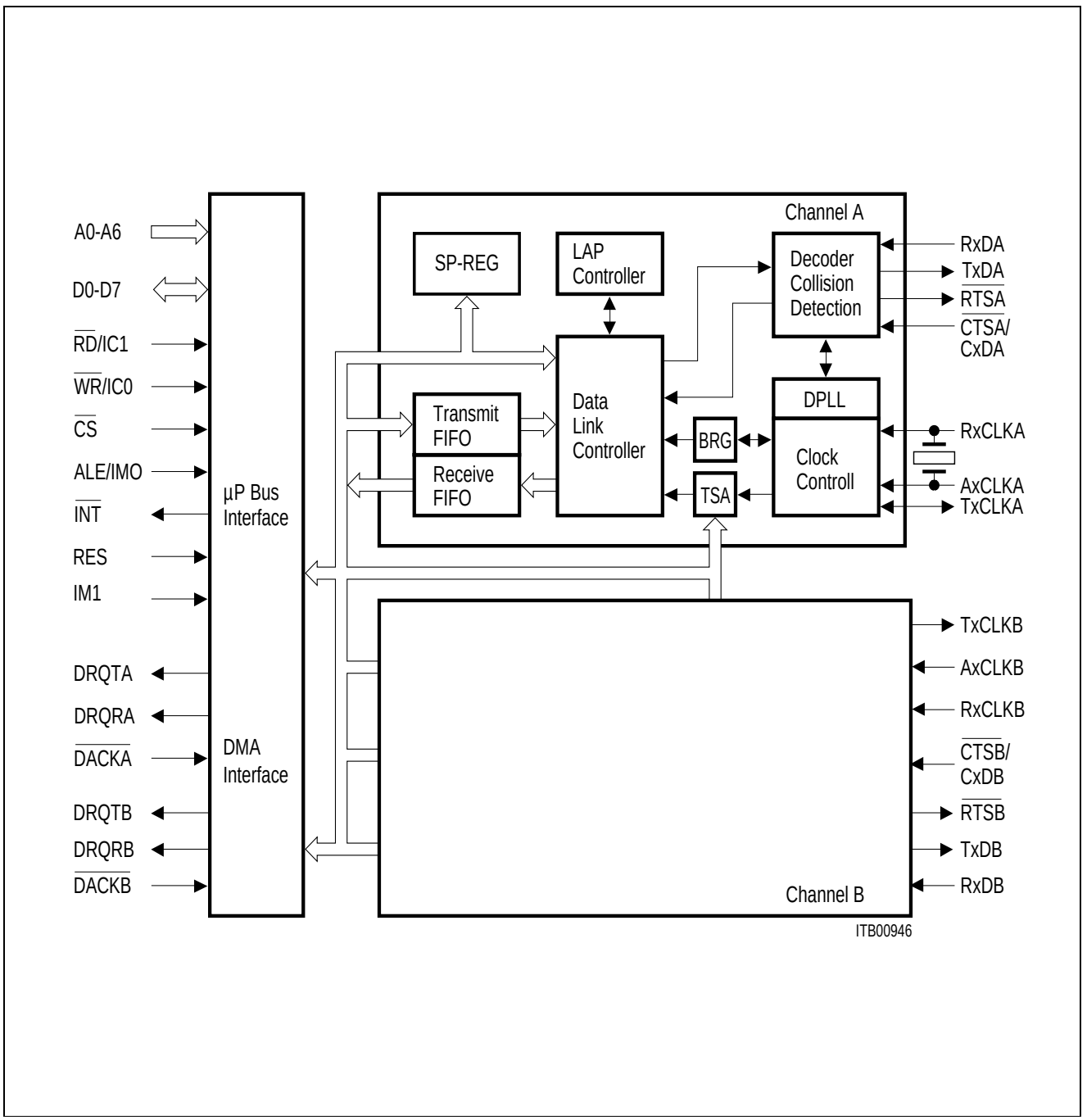


Figure 1
Block Diagram SAB 82525/SAB 82526

The HSCX SAB 82526 comprises one (channel B), the SAB 82525 two completely independent full-duplex HDLC channels (channel A and channel B), supporting various layer-1 functions by means of internal oscillator, Baud Rate Generator (BRG), Digital Phase Locked Loop (DPLL), and Time-Slot Assignment (TSA) circuits.

Furthermore, layer-2 functions are performed by an on-chip LAP (Link Access Procedure, e.g. LAPB or LAPD) controller.

1.2 System Integration

General Aspects

Figure 2 gives a general overview of the system integration of HSCX.

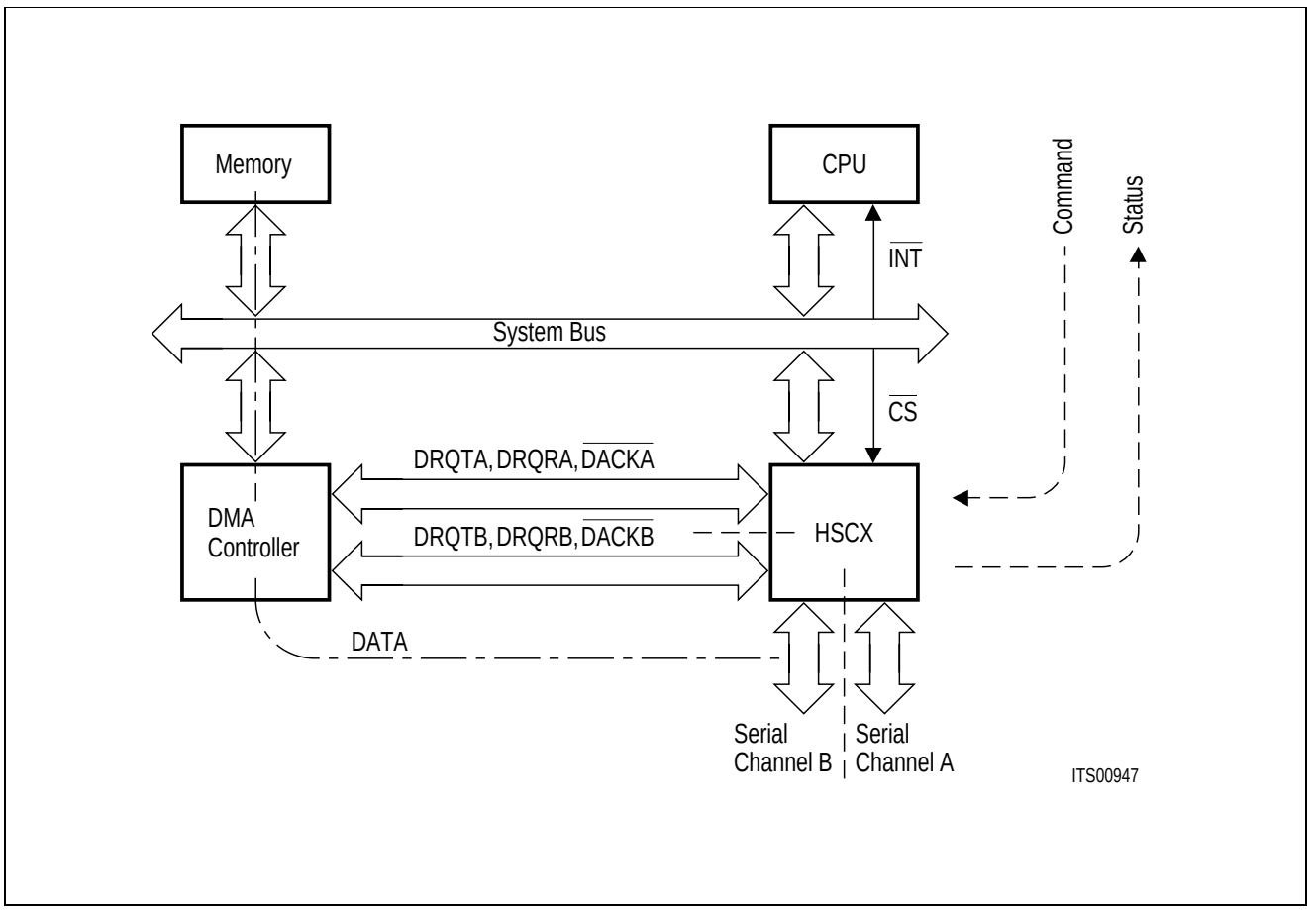


Figure 2
General System Integration of HSCX

The HSCX bus interface consists of an 8-bit bidirectional data bus (D0–D7), seven address line inputs (A0–A6), three control inputs ($\overline{RD}$/DS, $\overline{WR}$/R/$\overline{W}$, $\overline{CS}$), one interrupt request output ($\overline{INT}$) and a 4-channel DMA interface (DRQTA, DRQRA, $\overline{DACKA}$, DRQTB, DRQRB, $\overline{DACKB}$). Mode input pins (strapping options) allow the bus interface to be configured for either Siemens/ Intel or Motorola environment.

Generally, there are two types of transfers occurring via the system bus:

– command/status transfers, which are always controlled by the CPU. The CPU sets the operation mode (initialization), controls function sequences and gets status information by writing or reading the HSCX's registers (via $\overline{CS}$, $\overline{WR}$ or $\overline{RD}$, and register address via A0-A6).
– data transfers, which are effectively performed by DMA without CPU interaction using the HSCX's DMA interface (DMA mode). Optionally, interrupt controlled data transfer can be done by the CPU (interrupt mode).

Specific Applications

HSCX with SAB 8051 Microcontroller

For cost-sensitive applications, the HSCX can be interfaced with a small SAB 8051 microcontroller system (without DMA support) very easily as shown in **figure 3**.

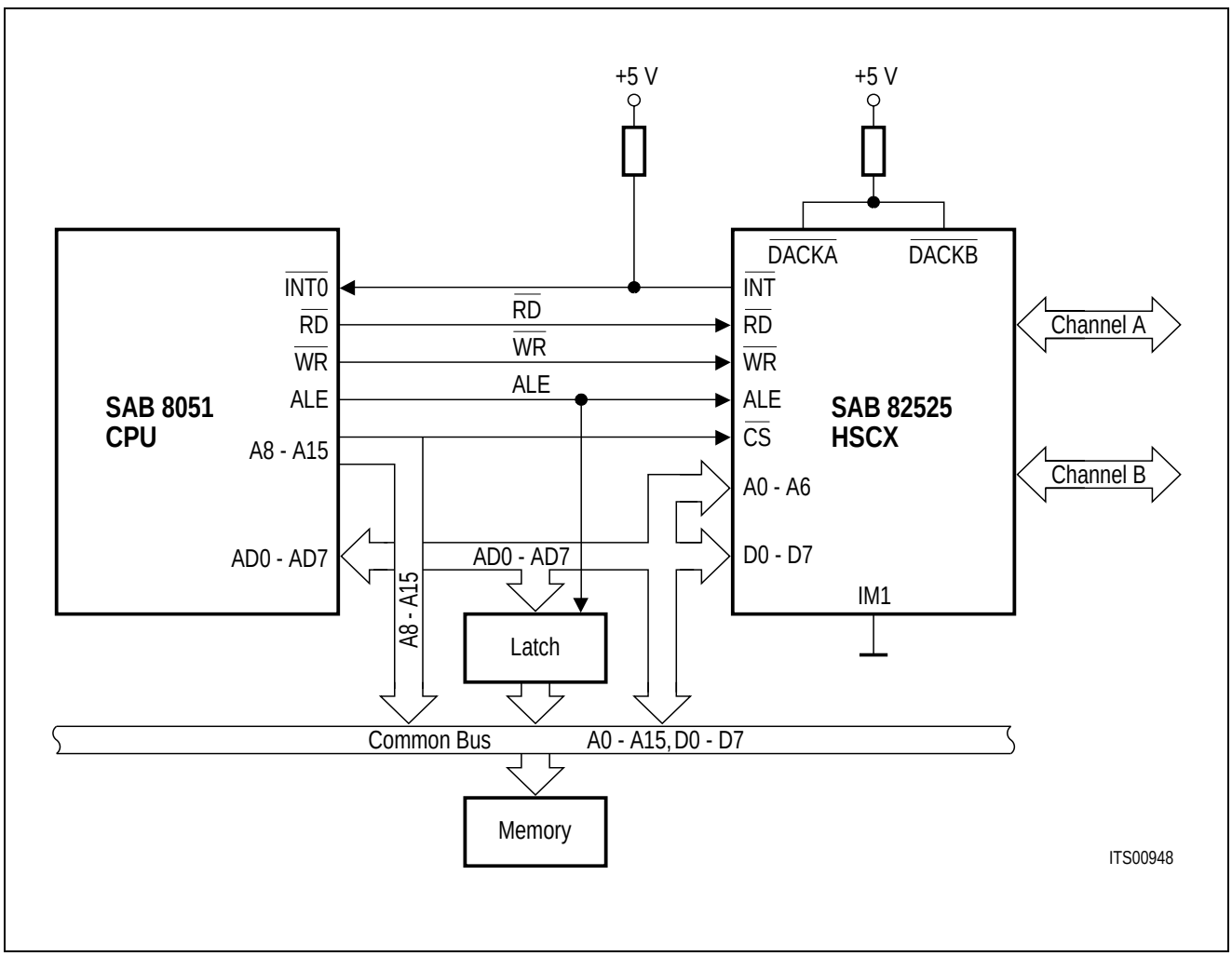


Figure 3
HSCX with 8051 CPU

Although the HSCX provides a demultiplexed bus interface, it can optionally be connected directly to the local multiplexed bus of SAB 8051 because of the internal address latch function (via ALE, compatibility to SAB 82520 HSCC).

The address lines A0 … A6 must be wired externally to the data lines D0 … D6 (direct connection) in this case.

Intel bus mode is selected connecting IM1 pin to low (V_{SS}). Since data transfer is controlled by interrupt, the DMA acknowledge inputs ($\overline{DACKA}$, $\overline{DACKB}$) are connected to V_{DD} (+ 5 V).

HSCX with SAB 80188 Microprocessor

A system with minimized additional hardware expense can be with a SAB 80188 microprocessor as shown in **figure 4.**

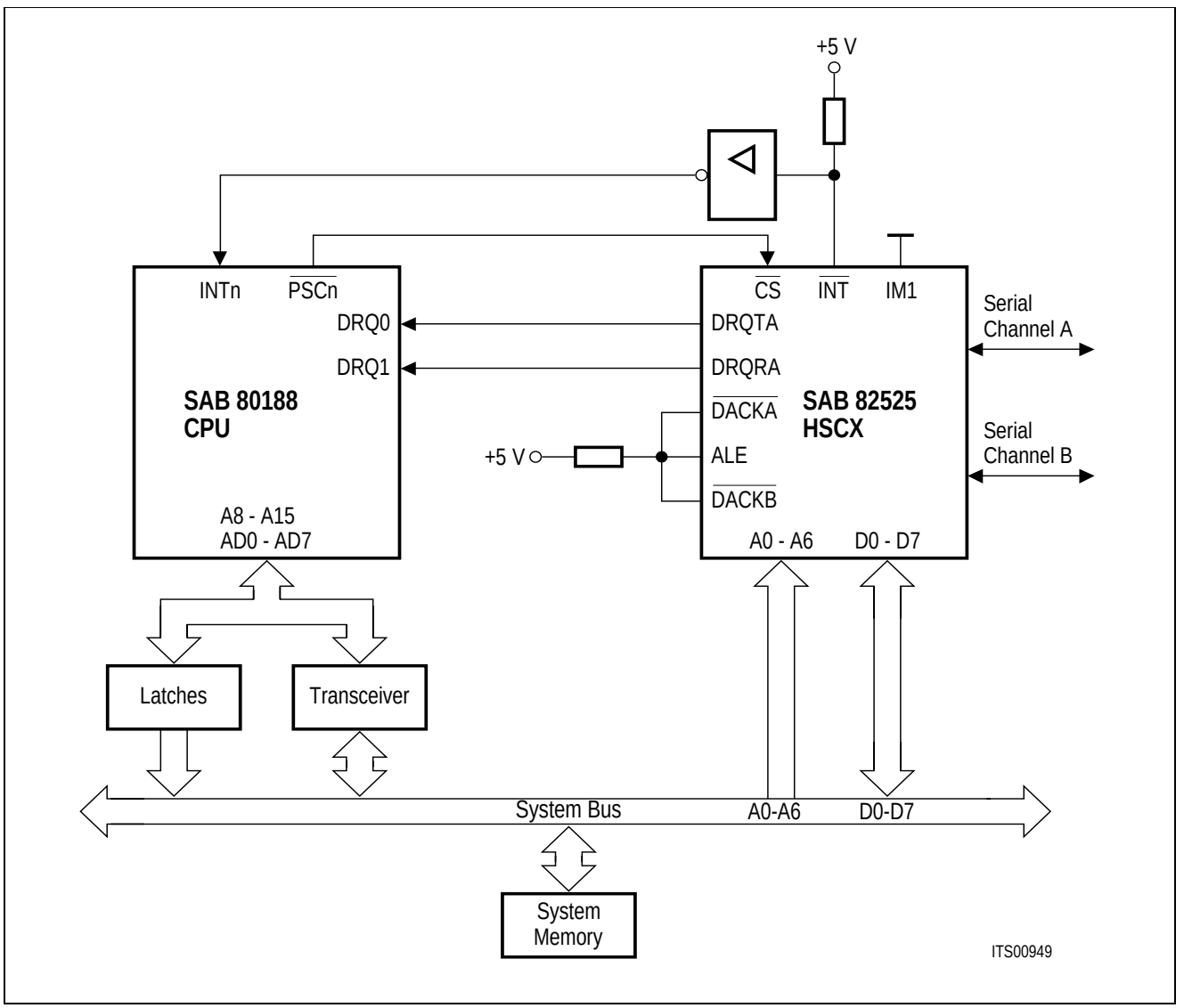


Figure 4
HSCX with SAB 80188 CPU

The HSCX is connected to the demultiplexed system bus. Data transfer for one serial channel can be done by the 2-channel on-chip DMA controller of the SAB 80188, the other channel is serviced by interrupt. Since the SAB 80188 does not provide DMA acknowledge outputs, data transfer from/to HSCX is controlled via $\overline{CS}$, $\overline{RD}$ or $\overline{WR}$ address information (A0 … A6) and the $\overline{DACKA}$, $\overline{DACKB}$ inputs are not used.

This solution supports applications with a high speed data rate in one serial channel with minimum hardware expense making use of the on-chip peripheral functions of the SAB 80188 (chip select logic, interrupt controller, DMA controller).

HSCX with SAB 80186 Microprocessor and SAB 82258 Advanced DMA Controller (ADMA)

In applications, where two high-speed channels are required, a 16-bit system with SAB 80186 CPU and SAB 82258 ADMA is suitable. This is shown in **figure 5.**

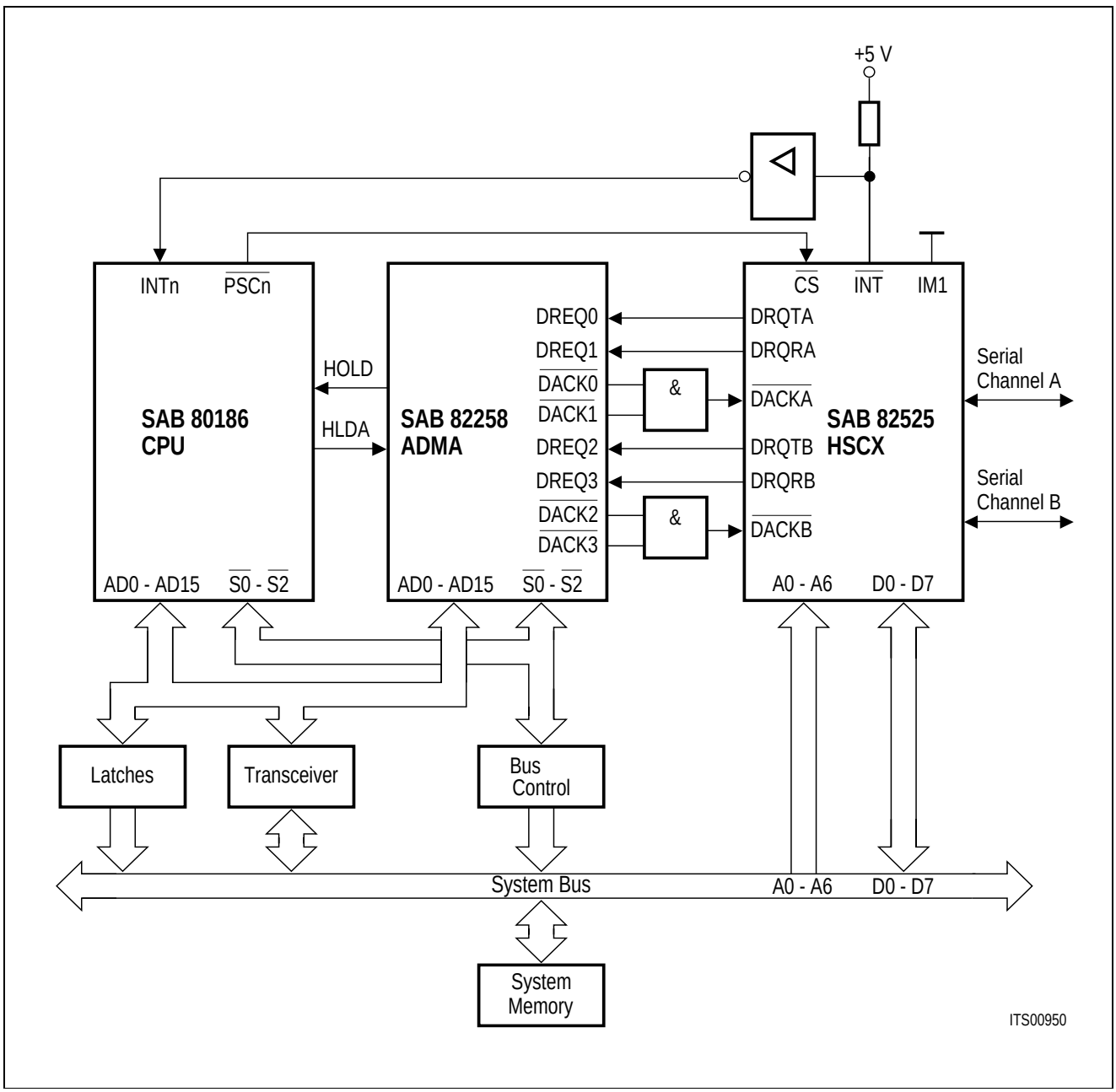


Figure 5
HSCX with SAB 80186 CPU/SAB 82258 ADMA

The four selector channels of ADMA are used for serving the four DMA request sources of HSCX, allowing very high data rates at both the system bus and the serial channels.

Another big advantage of the ADMA is it's data chaining feature, providing an optimized memory management for receive and transmit data. Recording the HSCX, a linked chain of 32 byte deep buffers can be set up, which are subsequently filled with the contents of the HSCX's FIFOs during reception. Not used buffers can be saved and linked to another buffer chain reserved for the reception of the next frame.

As a result, it's not necessary to reserve a very large space in system memory, determined by the maximum frame length of every received frame.

In this example, the ADMA works directly at the CPU's local bus and shares the same bus interface logic (address latches, transceivers, bus controller) with the SAB 80186. Since one DMA acknowledge line is provided for each DMA request, two DACK outputs must be ANDed together for input to the HSCX.

The HSCX's data lines are connected to the lower half of the system data bus (D0 … D7) and the address lines to A1 … A7, thus (from the CPU's point of view) all internal register addresses must be multiplied by two (even register addresses only).
e.g. CMDR register: HSCX address 61_H < = > system address $C2_H$.

1.3 Functional Description

General

The HSCX distinguishes from other low level HDLC devices by its advanced characteristics. The most important are:

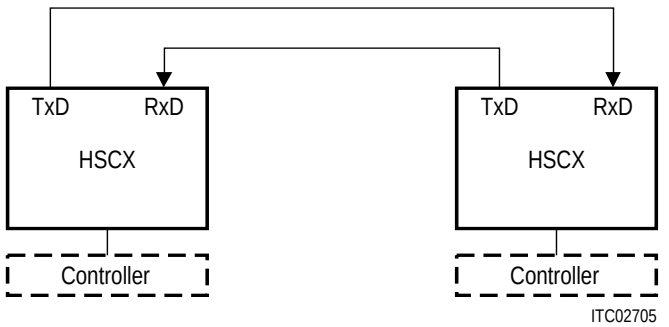
- Enlarged support of link configurations.

Beyond the point-to-point configurations, the HSCX directly enables point-to-multipoint or multimaster configurations without additional hardware or software expense.

In point-to-multipoint configurations, the HSCX can be used as a master as well as a slave station. Even when working as slave station, the HSCX can initiate the transmission of data at any time. An internal function block provides means of idle and collision detection and collision resolution, which are necessary if several stations start transmitting simultaneously.

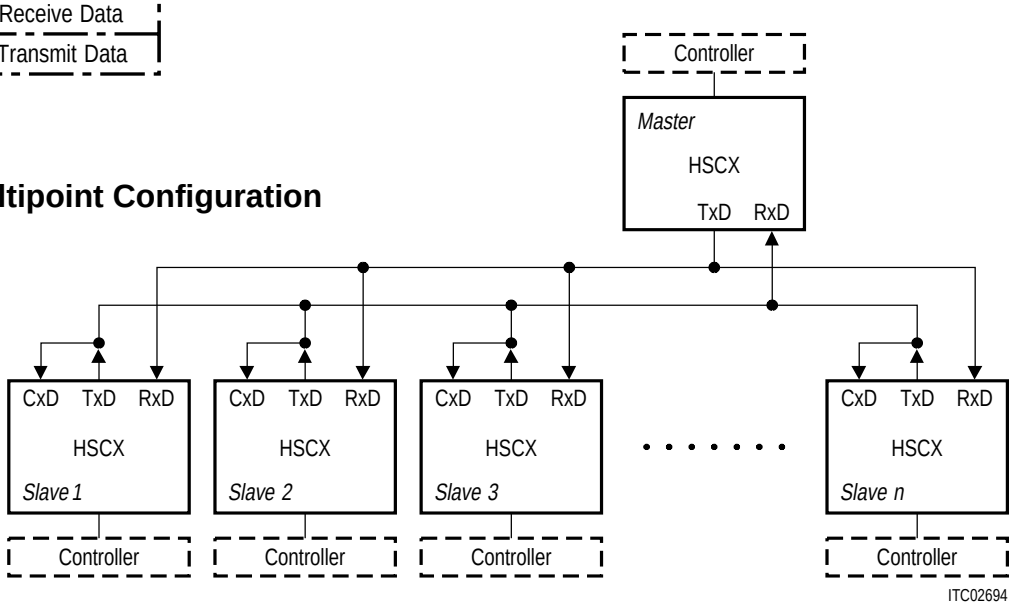
These features were integrated to support multimaster configurations.

Point-to-Point Configuration



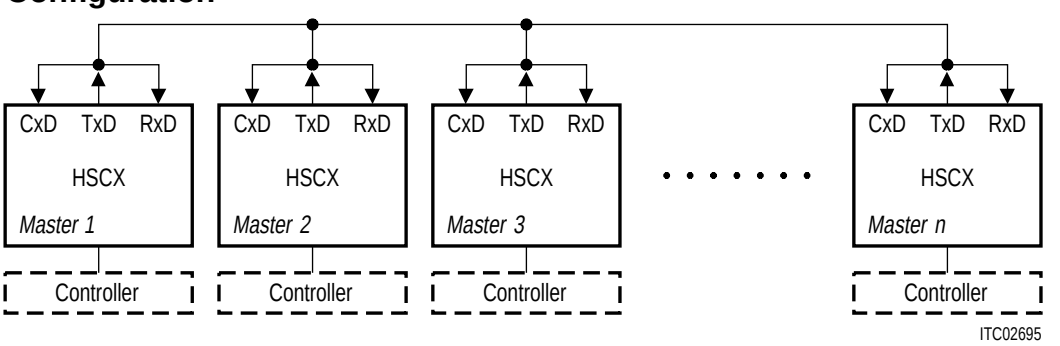
RxD - Receive Data
TxD - Transmit Data

Point-to-Multipoint Configuration



RxD - Receive Data
CxD - Collision Data
TxD - Transmit Data

Multimaster Configuration



RxD - Receive Data
CxD - Collision Data
TxD - Transmit Data

Figure 6
Link Configuration

- Support of layer-2 functions by HSCX

Beside those bit-oriented functions usually supported with the HDLC protocol, such as bit stuffing, CRC check, flag and address recognition, the HSCX provides a high degree of procedural support. In a special operating mode (auto-mode), the HSCX processes the information transfer and the procedure handshaking (I-, and S-frames of HDLC protocol) autonomously. The only restriction is, that the window size (= number of outstanding unacknowledged frames) is limited to 1, which will be sufficient in most applications. The communication procedures are mainly processed between the communication controllers and not between the processors. Thus the dynamic load of the CPU and the software expense is largely reduced.

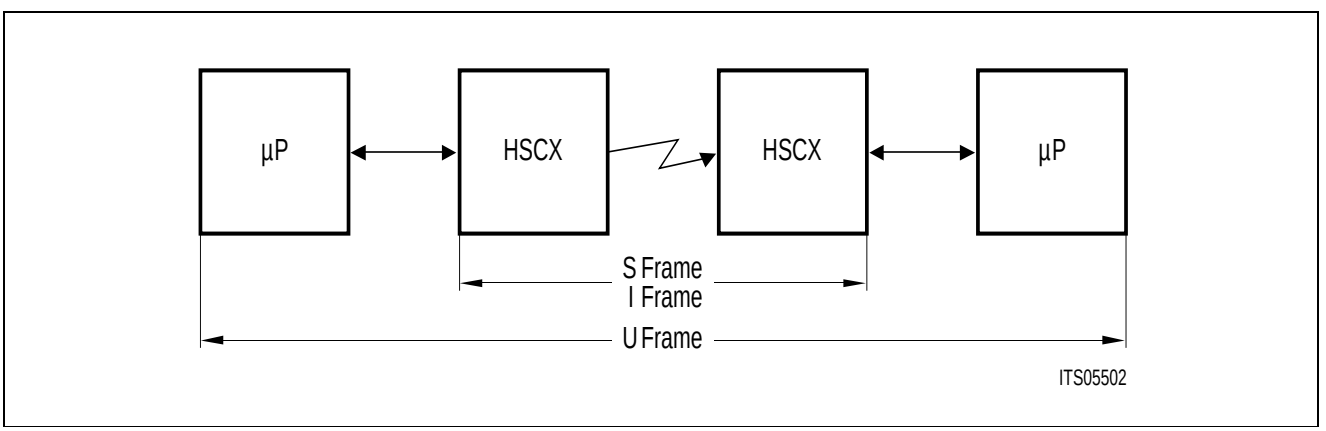


Figure 7
Procedural Support in Auto-Mode

The CPU is informed about the status of the procedure and has to manage the receive and transmit data mainly. In order to maintain cost effectiveness and flexibility, such functions as link setup/disconnection and error recovery in case of protocol errors (U-frames of HDLC protocols) are not implemented in hardware and must be done by user's software.

- Telecom specific features

In a special operating mode, the HSCX can transmit or receive data packets in one of up to 64 time-slots of programmable width (clock mode 5). Furthermore, the HSCX can transmit or receive variable data portions within a defined window of one or more clock cycles, which has to be selected by an external strobe signal (clock mode 1). These features make the HSCX especially suitable for all applications using time division multiplex methods, such as time-slot oriented PCM systems, systems designed for packet switching, or in ISDN applications.

- FIFO buffers to efficient transfer of data packets.

A further speciality of HSCX are the FIFO buffers used for the temporary storage of data packets transferred between the serial communications interface and the parallel system bus. Also because of the overlapping input/output operation (dual-port behaviour), the maximum message length is not limited by the size of the buffer. Together with the DMA capability, the dynamic load of the CPU is drastically reduced by transferring the data packets block by block via direct memory access. The CPU only has to initiate the data transmission by the HSCX and determine the status in case of completely received frames, but is not involved in data transfers.

2 Operating Modes

The HDLC controller of each channel can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be effected in a very flexible way, which satisfies most requirements.

There are 6 different operating modes which can be set via the MODE register.

2.1 Auto-Mode (MODE: MDS1, MDS0 = 00)

Characteristics: Window size 1, arbitrary message length, address recognition.

The HSCX processes autonomously all numbered frames (S-, I-frames) of an HDLC procedure.

The HDLC control field, data in the I-field of the frames and an additional status byte is temporarily stored in the RFIFO. The HDLC control field as well as additional information can also be read from special registers (RHCR, RSTA).

According to the selected address mode, the HSCX can perform a 2-byte or 1-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FE_H or FC_H (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address will be interpreted as COMMAND/RESPONSE bit (C/R), dependent on the setting of the CRI bit in RAH1, and will be excluded from the address comparison.

Similary, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the HSCX can be called (addressed) with 6 different address combinations, however, only the logical connection identified through the address combination RAH1, RAL1 will be processed in the auto-mode, all others in the non-auto mode. HDLC frames with address fields that do not match with any of the address combinations, are ignored by the HSCX.

In case of a 1-byte address, RAL1 and RAL2 will be used as compare registers. According to the X.25 LAPB protocol, the value in RAL1 will be interpreted as COMMAND and the value in RAL2 as RESPONSE.
After receiving a frame it takes 5 clock cycles to generate the response frame and to start transmission.

2.2 Non-Auto Mode (MODE: MDS1, MDS0 = 01)

Characteristics: address recognition, arbitrary window size.

All frames with valid addresses (address recognition identical to auto-mode) are forwarded directly to the system memory.

The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. The HDLC control field and additional information can also be read from special registers (RHCR, RSTA).

In non-auto mode, all frames are treated similarly.

2.3 Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 101)

Characteristics: address recognition high byte

Only the high byte of a 2-byte address field will be compared. The whole frame except the first address byte will be stored in RFIFO. RAL1 contains the second and RHCR the third byte following the opening flag.

2.4 Transparent Mode 0 (MODE: MDS1, MDS0, ADM = 100)

Characteristics: no address recognition

No address recognition is performed and each frame will be stored in the RFIFO. RAL1 contains the first and RHCR the second byte following the opening flag.

2.5 Extended Transparent Modes 0; 1 (MODE: MDS1, MDS0 = 11)

Characteristics: fully transparent

In extended transparent modes, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, bit-stuffing mechanism. This allows user specific protocol variations or the usage of Character Oriented Protocols (such as IBM BISYNC).

Data transmission is always performed out of the XFIFO. In extended transparent mode 0 (ADM = 0), data reception is done via the RAL1 register, which always contains the actual data byte assembled at the RxD pin. In extended transparent mode 1 (ADM = 1), the receive data are additional shifted into the RFIFO.
Also refer to chapter 6.1 and 6.2.