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SIEMENS

ICs for Communications

Enhanced Serial Communication Controller ESCC2

SAB 82532
SAF 82532

Version 3.2

User's Manual 07.96

SAB 82532 **SAF 82532** **Revision History:**		**Current Version: 07.96**
Previous Version: User's Manual 07.93		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)
-	10	new package provided: P-MQFP-80
-	72	Selectable out-of-band flow control in ASYNC mode: description added
-	75	In-band flow control transparency: description added
-	87	Selectable enhanced resolution BRG: description added
110, 141, 167	124, 170, 208	Timer register (TIMR): description extended for V3.x
107, 127	120, 149	RSTA register, ISR0 register (RME interrupt): description extended
115, 146, 172	133, 179, 217	XBCH, bit XC: description extended
124,152, 179	144, 187, 227	Baud rate generator register (BGR): description extended
133	157	Channel configuration register 4 (CCR4) in HDLC mode: description extended
138	164	STAR, bit XFW: description extended
140	168	Mode register (MODE) in ASYNC mode: new bits (FRTS, FRCS)
144	175	RFIFO Control Register (RFC) in ASYNC mode: new bit (DXS)
-	198, 237	Channel Configuration Register 4 (CCR4) in ASYNC and BISYNC mode: new register
204	256	XTAL1 clock period, high time and low time: min. values for N-10 version corrected

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1 Introduction

The Enhanced Serial Communication Controller ESCC2 (SAB 82532/SAF 82532) is a multiprotocol data communication controller with two symmetrical serial channels. It has been designed to implement high-speed communication links and to reduce hardware and software overhead needed for serial synchronous/asynchronous communications.

Each channel contains an independent clock generator, DPLL, encoder/decoder and programmable protocol hardware. Data communication with asynchronous, synchronous character oriented, and HDLC based protocols with extended support of X.25 LAPB, the ISDN LAPD, and SDLC protocols is implemented. Like the SAB 82525 (HSCX) which is a functional subset of the ESCC2, the ESCC2 is capable of handling a large set of layer-2 protocol functions independently of the host processor.

The version 82532N-10 of the Enhanced Serial Communication Controller (ESCC2) opens a wide area for applications which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications) by its programmable telecom-specific features. In this special operating mode (clock mode 5), which is applicable to all serial modes (HDLC/SDLC, ASYNC, BISYNC), the ESCC2 can transmit or receive data packets in one of up to 64 time-slots of programmable width.

The device is controlled via a parallel 16-bit wide interface which is directly compatible with the most popular 8/16 bit microprocessors (Siemens/Intel or Motorola type). The internal FIFOs (64 bytes per direction and channel) with additional DMA capability provide a powerful interface to the higher layers implemented in a microcontroller. For interrupt controlled systems, the ESCC2 supports daisy chaining and interrupt vector generation.

The ESCC2 is fabricated using SIEMENS advanced CMOS technology and is available in a P-LCC-68 and a P-MQFP-80 package.

Applications

- Universal, multiprotocol communication board for Workstation- and PC-boards
- Terminal controllers
- Computer peripherals
- Time slotted packet networks
- Multimaster communication networks
- LANs

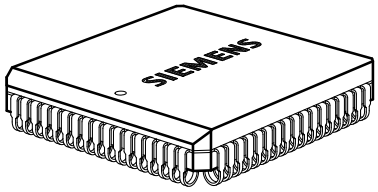
SIEMENS

Enhanced Serial Communication Controller ESCC2

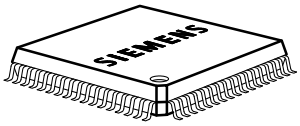
SAB 82532
SAF 82532

CMOS IC

1.1 Features



P-LCC-68



P-MQFP-80-1

Serial Interface

- Two independent full duplex serial channels
  - On chip clock generation or external clock source
  - On chip DPLL for clock recovery of each channel
  - Two independent baud rate generators
  - Independent time-slot assignment for each channel with programmable time-slot length (1 … 256 bits)
- Async, sync character oriented (MONOSYNC/BISYNC) or HDLC/SDLC modes (including SDLC LOOP)
- Transparent receive/transmit of data bytes without framing
- NRZ, NRZI, FM and Manchester encoding
- Modem control lines ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$, CD)
- CRC support:
  - HDLC/SDLC: CRC-CCITT or CRC-32 (automatic handling for transmit/receive direction)
  - BISYNC: CRC-16 or CRC-CCITT (support for transmit direction)

Type	Ordering Code	Package	Max. Data Rate		Time Slot Mode
			ext. clocked	int. (DPLL)	
SAB 82532 N	Q67101-H6790	P-LCC-68	2.048 Mbit/s	2 Mbit/s	no
SAB 82532 N-10	Q67101-H6791	P-LCC-68	10 Mbit/s	2 Mbit/s	yes
SAB 82532 H	Q67101-H6788	P-MQFP-80	2.048 Mbit/s	2 Mbit/s	no
SAB 82532 H-10	Q67101-H6789	P-MQFP-80	10 Mbit/s	2 Mbit/s	yes
SAF 82532 N-10	on request	P-LCC-68	10 Mbit/s	2 Mbit/s	yes
SAF 82532 H-10	on request	P-MQFP-80	10 Mbit/s	2 Mbit/s	yes

- Support of bus configuration by collision detection and resolution
- Statistical multiplexing
- Continuous transmission of 1 to 32 bytes possible
- Programmable preamble (8 bit) with selectable repetition rate (HDLC/SDLC and BISYNC)
- Data rate up to 10 Mbit/s
- Master clock mode with data rate up to 4 Mbit/s

Protocol Support (HDLC/SDLC)

- Various types of protocol support depending on operating mode
  - Auto mode (automatic handling of S- and I-frames)
  - Non-auto mode
  - Transparent mode
- Handling of bit oriented functions
- Support of LAPB/LAPD/SDLC/HDLC protocol in auto mode (I- and S-frame handling)
- Modulo-8 or modulo-128 operation
- Programmable time-out and retry conditions
- Programmable maximum packet size checking

MP Interface and Ports

- 64 byte FIFOs per channel and direction (byte or word access)
- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte and word access)
- Efficient transfer of data blocks from/to system memory via DMA or interrupt request
- Support of Daisy Chaining and Slave Operation with Interrupt Vector generation
- 8-bit programmable bi-directional universal port

General

- Advanced CMOS technology
- Low power consumption: active 40 mW at 2 MHz/standby 5 mW (typical values)
- P-LCC-68 Package
- P-MQFP-80 Package

1.2 Pin Configuration
(top view)

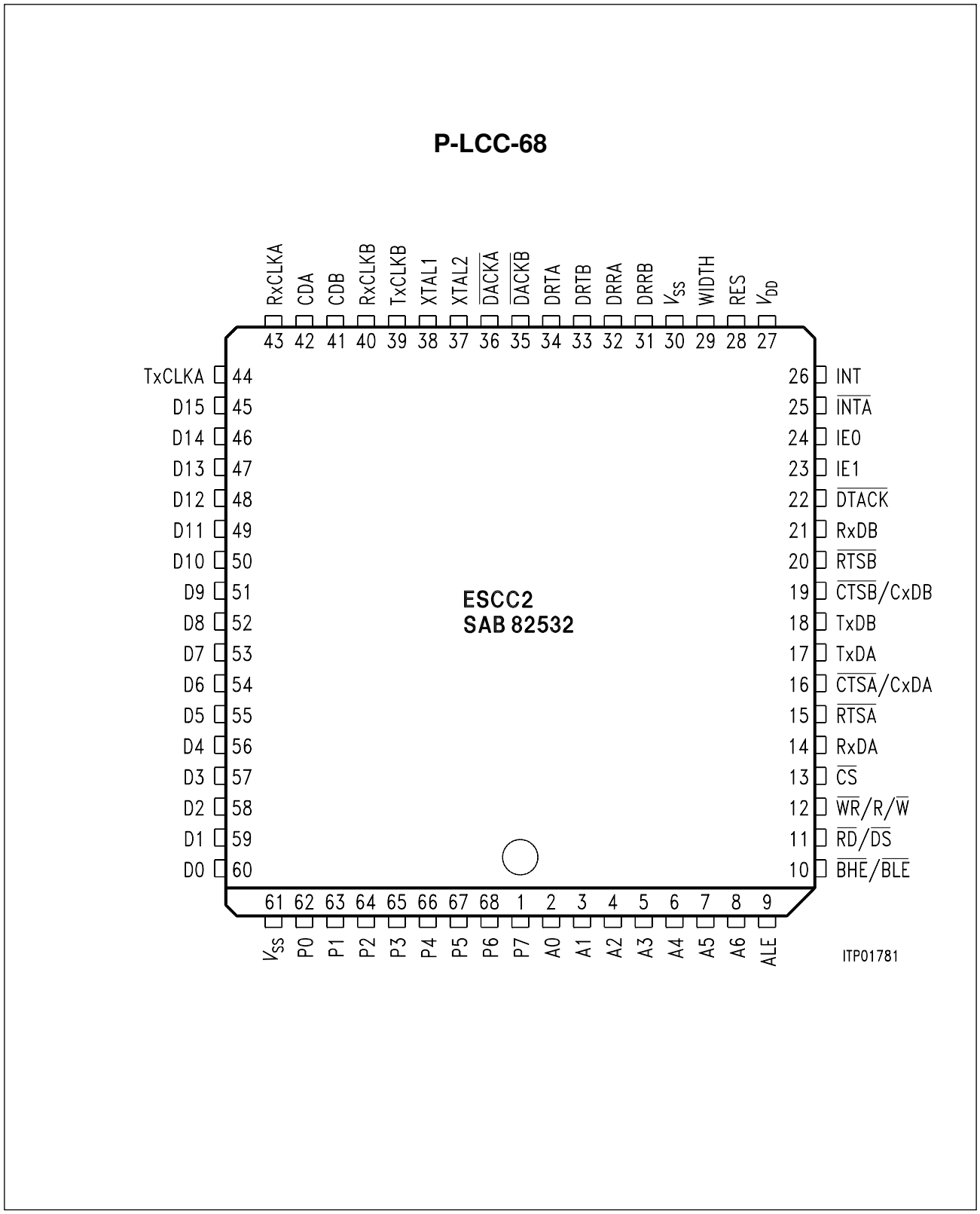


Figure 1

P-MQFP-80-1

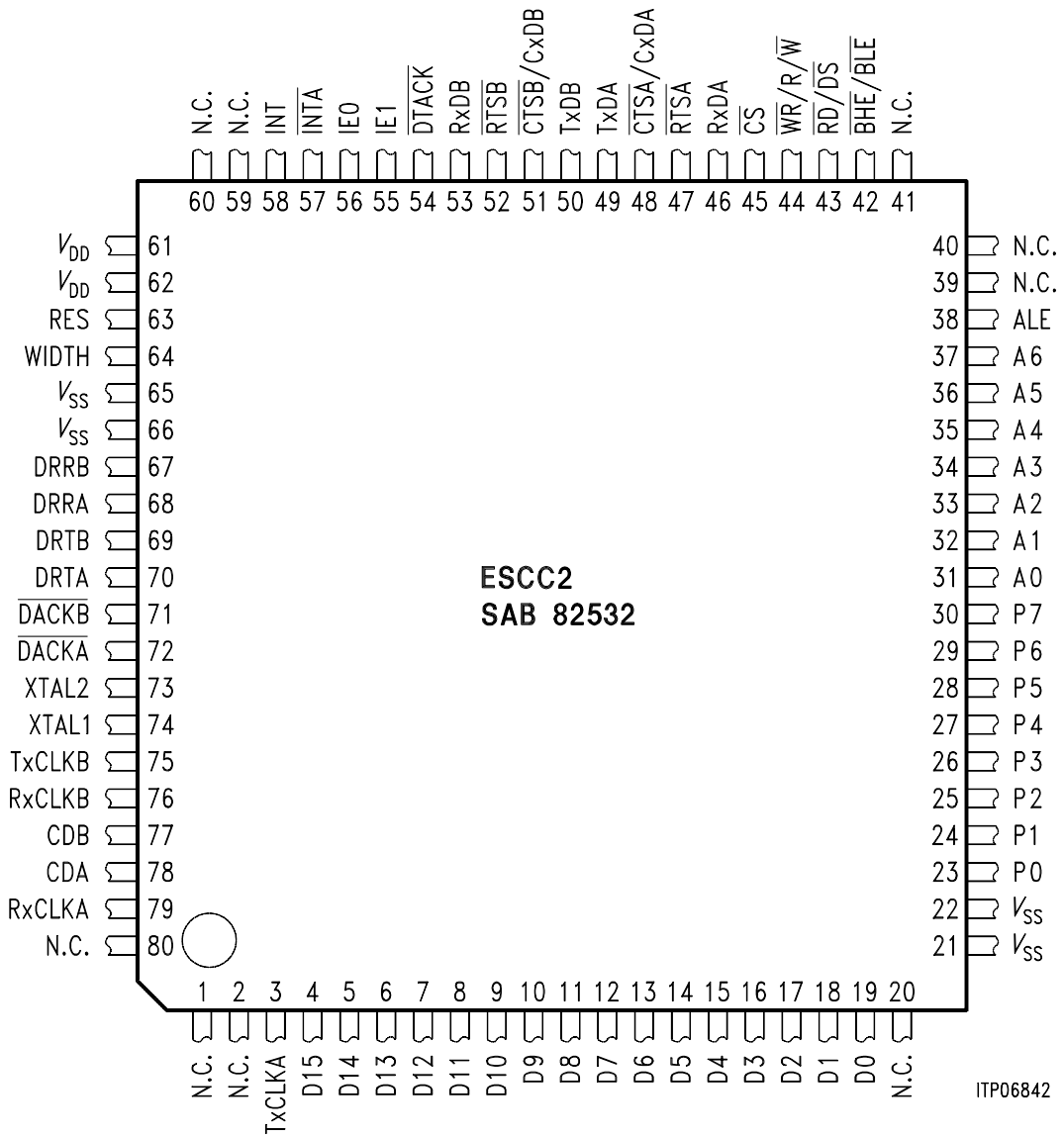


Figure 2

1.3 Pin Definitions and Functions

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
2 ... 8	31 … 37	A0 ... A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write.
60 ... 45	19 … 4	D0 ... D15	I/O	**Data Bus** Bi-directional three-state data lines which interface with the system's data bus. Their configuration is controlled by the level of pin WIDTH: – 8-bit mode (WIDTH = 0): D0 ... D7 are active. D8 ... D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. – 16-bit mode (WIDTH = 1): D0 ... D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via ALE). The unused half is in high impedance. For detailed information, refer to **chapter 3.1**.
9	38	ALE	I	**Address Latch Enable** The level at this pin defines the bus interface mode: **Fixed to V_{SS}:** Demultiplexed Siemens/Intel bus interface **Fixed to '1':** Demultiplexed Motorola bus interface **Switching:** Multiplexed Siemens/Intel bus interface The address information provided on lines A0 ... A6 is internally latched with the falling edge of ALE. This function allows the ESCC2 to be directly connected to a multiplexed address/data bus. In this case, pins A0 ... A6 must be externally connected to the Data Bus pins (e.g. D0 … D6 for 8-bit CPUs).

Note: All unused input pins have to be connected to a defined level.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
11	43	$\overline{RD}/\overline{DS}$	I	**Read Enable** (Siemens/Intel bus mode) This signal indicates a read operation. When the ESCC2 is selected via $\overline{CS}$ the READ signal enables the bus drivers to output data from an internal register addressed via A0 … A6 on to Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 2**. If DMA transfer is selected via $\overline{DACKA}$ or $\overline{DACKB}$, the $\overline{RD}$ signal enables the bus drivers to put data from the corresponding Receive FIFO on the Data Bus. Inputs A1 … A6 are ignored. A0 and $\overline{BHE}/\overline{BLE}$ are used to select byte or word access. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations.
12	44	$\overline{WR}/R/\overline{W}$	I	**Write Enable** (Siemens/Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the ESCC2 loads an internal register with data provided via the Data Bus. For more information about control/status register and FIFO access in the different bus interface modes refer to **chapter 2**. If DMA transfer is selected via $\overline{DACKA}$ or $\overline{DACKB}$, the $\overline{WR}$ signal enables latching data from the Data Bus on the top of the corresponding Transmit FIFO. Inputs A0 … A6 are ignored. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.
13	45	$\overline{CS}$	I	**Chip Select** A low signal selects the ESCC2 for read/write operations. $\overline{CS}$ has no function in interrupt acknowledge or DMA cycles.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
28	63	RES	I	**Reset** A high signal on this pin forces the ESCC2 into reset state. During Reset the ESCC2 is in power up mode, after Reset in power-down mode. Re-activation of each channel is done via bit CCR0:PU (refer to **chapter 9.2**). During Reset – all uni-directional output stages are in high-impedance state, – all bi-directional output stages (data bus) are in high-impedance state, – output XTAL2 is in high-impedance if input XTAL1 is 'high' (the internal oscillator is disabled during reset), – signals $\overline{RD}$ and $\overline{INTA}$ have to be 'high'
10	42	$\overline{BHE}$/ $\overline{BLE}$	I	**Bus High Enable** (Siemens/Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus (D8…D15). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 3.1** for detailed information. **Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus (D0 … D7). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. Refer to **chapter 3.1** for detailed information.
29	64	WIDTH	I	**Width Of Bus Interface** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Moreover, byte transfers (in conjunction with A0 and $\overline{BHE}$/$\overline{BLE}$) are allowed, too.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
22	54	$\overline{\text{DTACK}}$	O (oD)	**Data Transfer Acknowledge** During a bus cycle (read/write, asynchronous bus), this signal indicates that ESCC2 is ready for data transfer. The signal remains active until the data strobe ($\overline{\text{DS}}$, $\overline{\text{RD}}$ or $\overline{\text{WR}}$) and/or the Chip Select signal ($\overline{\text{CS}}$) or the Interrupt Acknowledge ($\overline{\text{INTA}}$) go inactive. An external resistor has to be tied to V_{DD} if this function is used.
26	58	INT	O (oD)	**Interrupt Request** INT serves as general interrupt request which may include all serial mode specific interrupt sources and the requests of the 8-bit universal port if programmed. These interrupt sources can be masked via registers IMR0, IMR1 (channel) and PIM (universal port). Interrupt status is reported via registers GIS (Global Interrupt Status), ISR0, ISR1 (channel) and PIS (universal port). Output characteristics (push-pull active low/high, open drain) are determined by programming the IPC register. In Daisy Chain cascading mode INT signal generation is only enabled if the Interrupt Enable input IE1 is active (logical '1'). INT is reset if – interrupts are disabled in Daisy Chain cascading mode (pin IE1 = '0'), – no further interrupt is pending, i.e. all interrupt status bits are reset.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
25	57	$\overline{\text{INTA}}$	I	**Interrupt Acknowledge** If the interrupt is acknowledged via pin $\overline{\text{INTA}}$, an interrupt vector is output on D0 … D7. All interrupt sources are organized in 8 groups with fixed priority (refer to **chapter 2**). The generated interrupt vector refers to the interrupt group with currently highest priority (although more than one interrupt source/group may be active). Reaction on $\overline{\text{INTA}}$ signal depends on the bus interface mode and the cascading mode in conjunction with the Interrupt Enable pins IE0 and IE1 (ref. to IPC register): Motorola bus mode: INT is reset with the rising edge of the following valid $\overline{\text{INTA}}$ cycle if no further interrupt is pending. The interrupt vector is output with signal $\overline{\text{DS}}$. Siemens/Intel bus mode: INT is reset with the rising edge of the **second** valid $\overline{\text{INTA}}$ cycle (2-cycle '86 mode) if no further interrupt is pending. Slave mode: Interrupt acknowledge is accepted if an interrupt signal has been generated and the slave address provided via IE0, IE1 corresponds to the programmed value (IPC register). Daisy Chaining mode: Interrupt acknowledge is accepted if an interrupt signal has been generated and Interrupt Enable input IE1 is active during the following $\overline{\text{INTA}}$ cycle. *Note: Pins $\overline{CS}$, $\overline{DACKA}$ and $\overline{DACKB}$ have to be inactive during an $\overline{INTA}$ cycle. If pin $\overline{INTA}$ is not used, it has to be tied to V_{DD}.*

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
24 23	56 55	IE0 IE1	I/O I	**Interrupt Enable 0, 1** The function depends on the selected cascading mode: **Slave mode:** IE0 and IE1 are inputs. Interrupt acknowledge is accepted if an interrupt signal has been generated and the slave address provided via IE0, IE1 corresponds to the programmed value (IPC register). If not used, IE0 and IE1 should be tied to GND and the slave address should be set to '0' (e.g. single device application). **Daisy Chaining mode:** IE0 is output, IE1 is input. Normally, IE1 is connected to the IE0 pin of devices with higher priority. If not used, IE1 has to be fixed to '1'. If IE1 is reset ('0') – the IE0 output is reset immediately, – an active INT signal will be prohibited or aborted. As long as $\overline{\text{INTA}}$ input is inactive, IE1 = '1' enables INT signal generation. If INT goes active, pin IE0 immediately is set to '0'. Interrupt acknowledge is accepted if the Interrupt Enable input IE1 is active during the following $\overline{\text{INTA}}$ cycle. During this cycle, and additionally 'till the end of the second $\overline{\text{INTA}}$ cycle in Siemens/Intel bus mode, triggering of INT signal generation is prohibited, i.e. no interrupt will be generated while (another) device is under service. This is valid even for devices with higher priority. Pin IE0 returns to active state (logical '1') when INT is reset and IE1 input is high.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
34 33	70 69	DRTA DRTB	O	**DMA Request Transmitter** (channel A/channel B) The transmitter of ESCC2 requests a DMA transfer by activating this line. The request remains active as long as the respective Transmit FIFO requires data transfers. The amount of data bytes to be transferred from the system memory to the ESCC2 (= byte count) must be written first to the XBCH, XBCL registers. Always blocks of data (n × 32 bytes + REST, n = 0, 1, …) are transferred 'till the Byte Count is reached. DRTn is deactivated with the beginning of the last write cycle.
32 31	68 67	DRRA DRRB	O	**DMA Request Receiver** (channel A/channel B) The receiver of ESCC2 requests a DMA transfer by activating this line. The request remains active as long as the corresponding Receive FIFO requires data transfers, thus always blocks of data are transferred. DRRn is deactivated immediately following the falling edge of the last read cycle.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
36 35	72 71	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/channel B) A low signal on these pins informs the ESCC2 that the requested DMA cycle controlled via DRTA/B or DRRA/B is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either write or read). In conjunction with a read or write operation these inputs serve as Access Enable (similar to $\overline{\text{CS}}$) to the respective FIFOs. If $\overline{\text{DACK}}$ is active, the input to pins A1 … A6 is ignored and the FIFOs are implicitly selected. A0 and $\overline{\text{BHE}}$/$\overline{\text{BLE}}$ are used to select byte or word access. If not used, these pins must be connected to V_{DD}.
14 21	46 53	RxDA RxDB	I (O/oD)	**Receive Data** (channel A/channel B) Serial data is received on these pins. May be switched to TxD function via bit CCR2:SOC1.
43 40	79 76	RxCLKA RxCLKB	I	**Receive Clock** (channel A/channel B) The function of these pins depends on the selected clock mode. In each channel, RxCLKn may supply either – the receive clock (clock mode 0), or – the receive and transmit clock (clock mode 1, 5), or – the clock input for the baud rate generator (clock mode 2, 3).

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
15 20	47 52	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O	**Request to Send** (channel A/channel B) When the RTS bit in the MODE register is set, the $\overline{\text{RTS}}$ signal goes low. When the RTS bit is reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In bus configuration, $\overline{\text{RTS}}$ can be programmed via CCR2 to: – go low during the actual transmission of a frame shifted by one clock period, excluding collision bits. – go low during reception of a data frame. – stay always high ($\overline{\text{RTS}}$ disabled).
16 19	48 51	$\overline{\text{CTSA}}$/ CxDA $\overline{\text{CTSB}}$/ CxDB	I	**Clear to Send** (channel A/channel B) A low on the $\overline{\text{CTSn}}$ input enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the $\overline{\text{CTSn}}$ pin (programmable feature). If no 'Clear To Send' function is required, the $\overline{\text{CTSn}}$ inputs can be directly connected to GND. **Collision Data** (channel A/channel B) In a bus configuration, the external serial bus must be connected to the corresponding CxDn pin for collision detection.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
42 41	78 77	CDA CDB	I	**Carrier Detect** (channel A/channel B) The function of this pin depends on the selected clock mode. It can supply – either a modem control or a general purpose input (clock modes 0, 2, 3, 4, 6, 7). If auto-start is programmed, it functions as a receiver enable signal. – or a receive strobe signal (clock mode 1). – or a frame synchronization signal in time-slot oriented operation mode (clock mode 5). Additionally, an interrupt may be issued if a state transition occurs at the CDn pin (programmable feature).
17 18	49 50	TxDA TxDB	O/oD (I)	**Transmit Data** (channel A/channel B) Transmit data is shifted out via these pins. They can be programmed to be either a push-pull or open drain output to support bus configurations. *Note: Pin TxD is 'OR'ed with pin $\overline{RTS}$ if NRZI encoding and IDLE as Interframe* *Note: Time Fill are selected and bit MODE:RTS is reset.* *May be switched to RxD function via bit CCR2:SOC1.*

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
44 39	3 75	TxCLKA TxCLKB	I/O	**Transmit Clock** (channel A/channel B) The function of this pin depends on the selected clock mode and the value of the SSEL bit (CCR2 register). For detailed information about the clock modes refer to **chapter 2**. If programmed as an input, this pin supplies either – the transmit clock for the channel (clock mode 0, 2, 6; SSEL bit in CCR2 is reset), or – a transmit strobe signal for the channel (clock mode 1). If programmed as an output (bit CCR2:TOE is set), this pin supplies either – the transmit clock for the channel which is generated • either from the baud rate generator (clock mode 2, 3, 6, 7; SSEL bit in CCR2 is set), • or from the DPLL circuit (clock mode 3, 7; SSEL bit in CCR2 is reset) • or from the crystal oscillator (clock mode 4), • or an active-low tri-state control signal marking the programmed transmit time-slot (clock mode 5) if bit CCR2:TOE is set.
38 37	74 73	XTAL1 XTAL2	I (O)	**Crystal Connection** If the internal oscillator is used for clock generation the external crystal has to be connected to these pins. Moreover, XTAL1 may be used as common clock input for channel A and channel B provided by an external clock generator. All versions: common use for both channels in clock modes 4, 6, 7. Version 2 upward: additionally used in clock mode 0b and for master clock applications.

1.3 Pin Definitions and Functions (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-LCC-68	P-MQFP-80			
62 ... 68,1	23 … 30	P0 … P7	I/O	**Parallel Port** A general purpose 8-bit bi-directional parallel port is provided on pins P0 … P7. Every pin is individually programmable to operate as an output or an input (Port Configuration Register PCR). – If defined as output, the state of the pin is directly controlled via the microprocessor interface (Port Value Register PVR). – If defined as input, its state can be read via PVR. All changes may be indicated via an interrupt status (Port Interrupt Mask register PIM, Port Interrupt Status register PIS, interrupt is output on pin INT).
30 61	21, 22, 65, 66	V_{SS}	I	**Ground** (0 V) For correct operation, **all** pins have to be connected to ground.
27	61, 62	V_{DD}	I	Positive power supply

Note: All unused input pins have to be connected to a defined level.

1.4 Logic Symbol

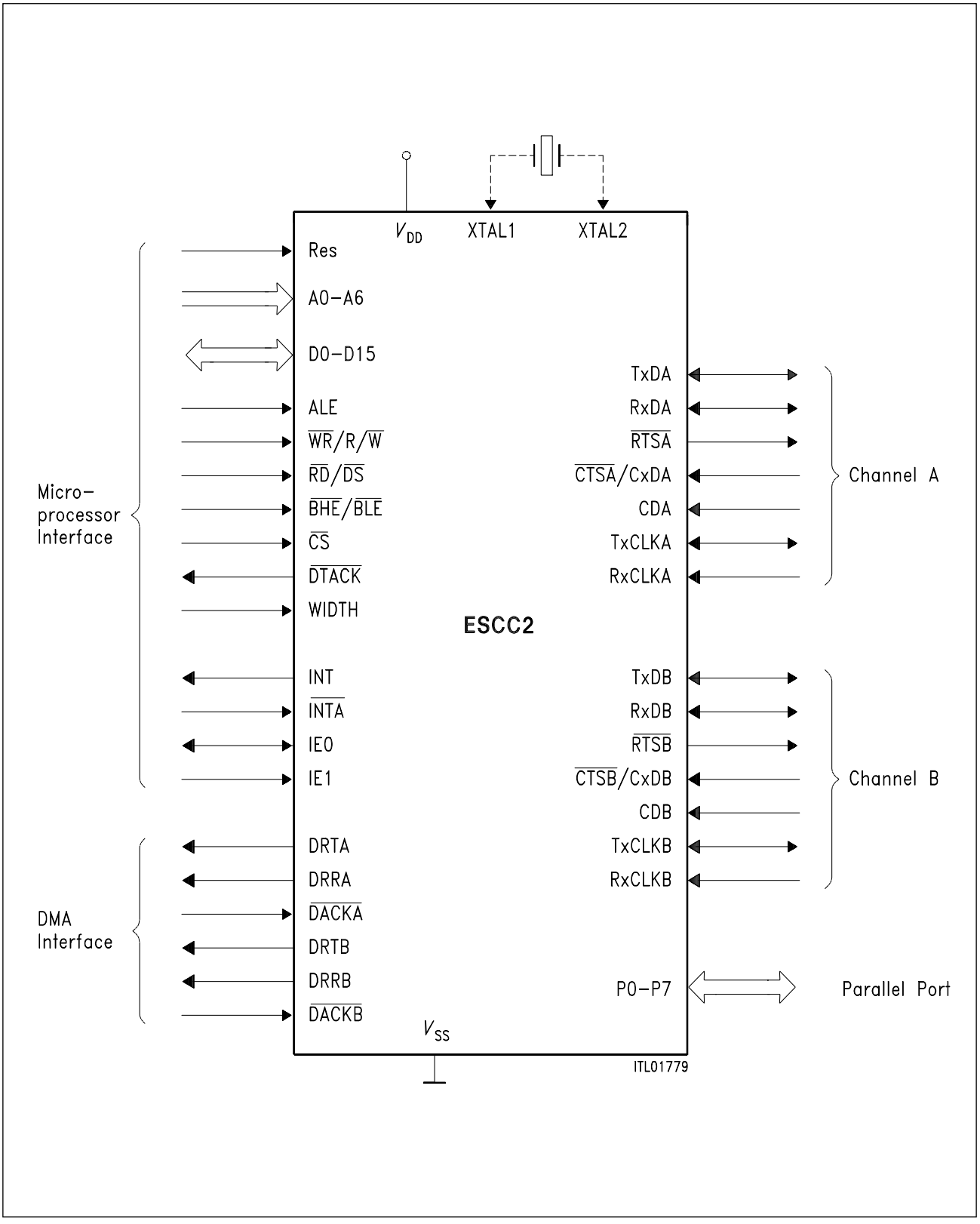


Figure 3
ESCC2 Logic Symbol

1.5 Functional Block Diagram

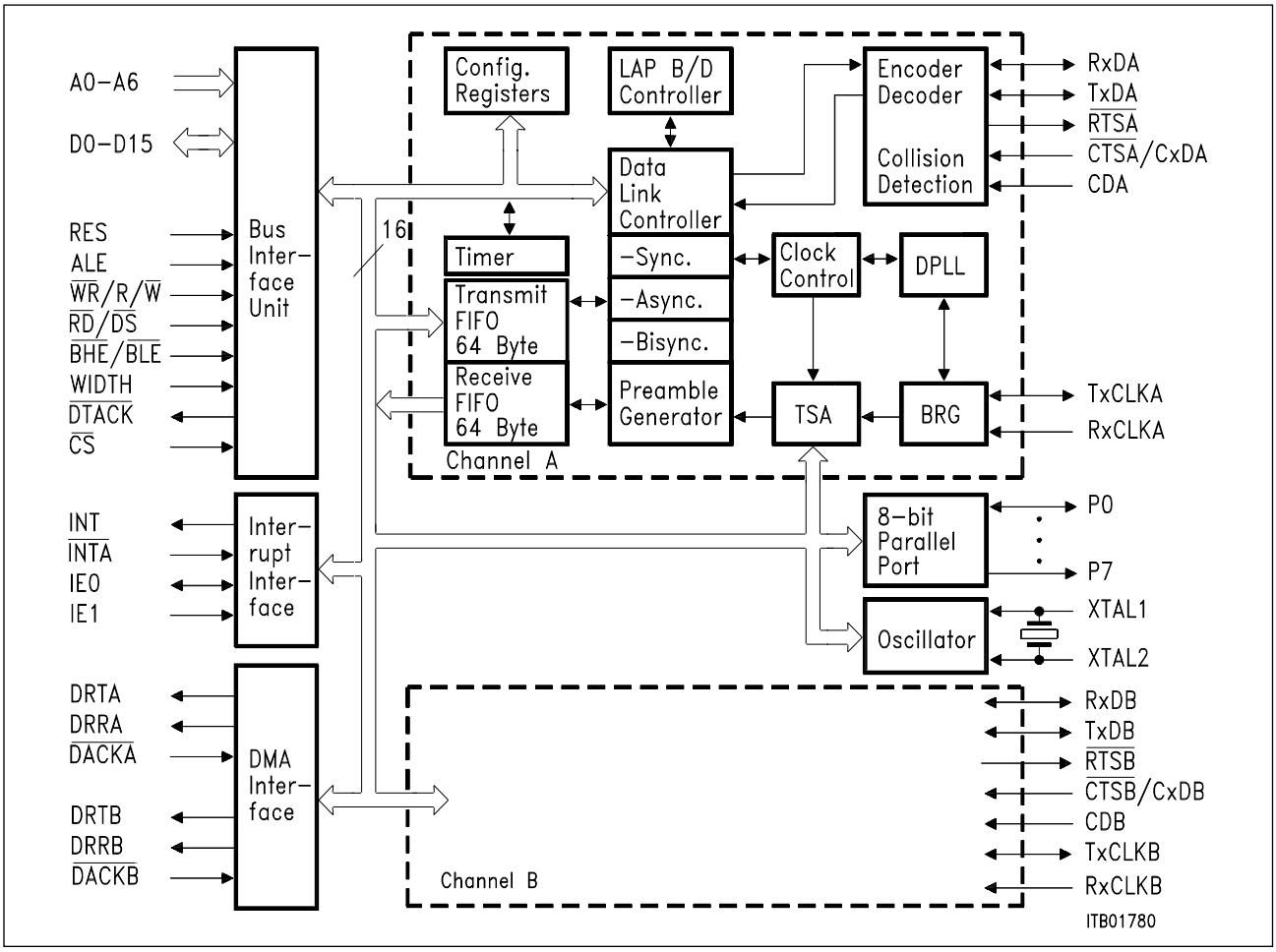


Figure 4
Functional Block Diagram SAB 82532/SAF 82532

The ESCC2 (SAB 82532/SAF 82532) comprises two completely independent full-duplex serial interfaces (channel A and channel B) which support HDLC/SDLC, BISYNC and ASYNC protocols. Layer-1 functions are performed by means of internal oscillator, Baud Rate Generator (BRG), Digital Phase Locked Loop (DPLL), and Time-Slot Assignment circuits (TSA, only available for versions SAB/SAF 82532 N-10 and SAB/SAF 82532 H-10). Encoding/decoding of serial data can be done by using NRZ, NRZI, FM0, FM1 and Manchester encoding schemes. An 8-bit universal bi-directional port is provided which can be used for additional modem control lines or for general I/O purposes.

Associated with each serial channel is a set of independent command and status registers and 64-byte deep FIFOs for transmit and receive direction. Access is done via the flexible 8/16-bit microprocessor interface. DMA capability has been added to the ESCC2 by means of a 4-channel DMA interface with one DMA request line for each transmitter and receiver of both channels. The interrupt structure of ESCC2 supports interrupt driven systems using interrupt polling, daisy chaining or interrupt vector control.

1.6 System Integration

1.6.1 General Aspects

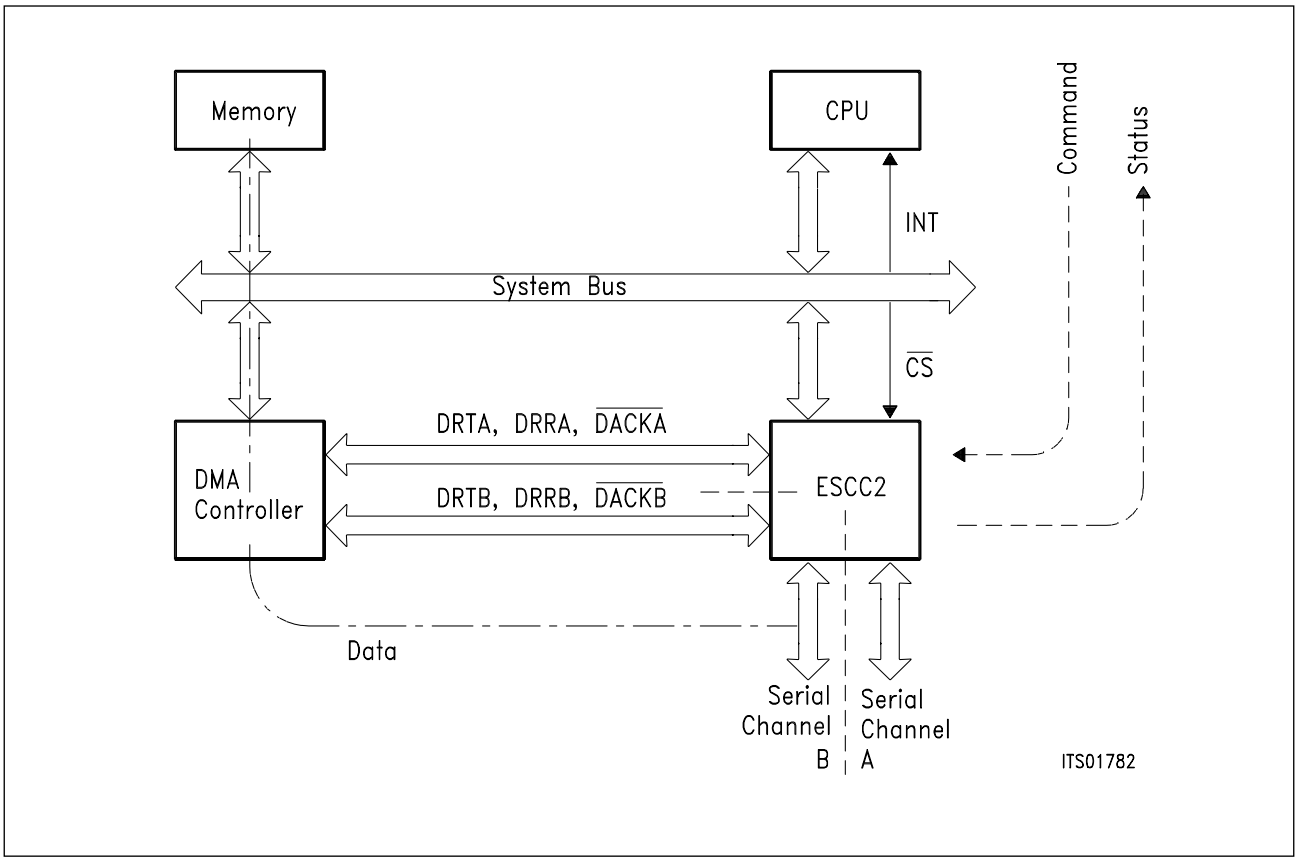


Figure 5
General System Integration of ESCC2

Figure 5 gives a general overview of system integration of ESCC2.

The ESCC2's bus interface consists of an 8/16-bit bidirectional data bus (D0 … D15), seven Address Line inputs (A0 … A6), three control inputs (RD/DS, WR/R/W, CS), four signals for interrupt support (INT, INTA, IE0, IE1) and a 4-channel DMA interface (DRTA, DRRA, DACKA, DRTB, DRRB, DACKB). Mode input pins (strapping options) allow the bus interface to be configured for 8/16-bit bus width and for either Siemens/Intel or Motorola environment.

Generally, there are two types of transfers occurring via the system bus:

– Command/Status transfers, which are always controlled by the CPU. The CPU sets the operation mode (initialization), controls function sequences and gets status information by writing or reading the ESCC2's registers (via CS, WR or RD, and register address via A0 … A6).
– Data Transfers, which are effectively performed by DMA without CPU interaction using the ESCC2's DMA interface (DMA mode). Optionally, interrupt controlled data transfer can be done by the CPU (interrupt mode).