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Data Sheet, DS 1, April 2001

C165H
Embedded C166 with USART, IOM-2 and HDLC Support

Version 1.3

Wired Communications

Never stop thinking.

Edition 2001-04-01

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Data Sheet, DS 1, April 2001

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Revision History: **2001-04-01** DS 1

Previous Version:	This is the first non-preliminary version. [1)]
Page	Subjects (major changes since last revision)

[1)]All previous distributed versions are *preliminary*. They have been replaced by this version.

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Embedded C166 with USART, IOM-2 and HDLC Support
C165H

Device Version 1.3 **CMOS**

1 Overview

C165H is a new low cost member of the Infineon Communication Controller family using low power CMOS technology. The device combines the successful Infineon C166 16-bit full-static core with four independent HDLC controllers, IOM-2 interface and 3-kbyte of Dual-Port on-chip RAM to a Intelligent **T**erminal **A**dapter with **H**DLC support.

P-TQFP-144

C165H adresses all high feature ISDN TA, Intelligent NT or SOHO PBX designs, offering up to 18 MIPS along with legacy peripherals such as USART, SCI and Timers.

C165H provides:

- On-Chip full-static C166 Core supporting a 16- or 8-bit C16x Family System running up to 36 MHz
- ISDN BRI supporting data rates of 56 kbit/s, 64 kbit/s, 128 kbit/s and 144 kbit/s
- IOM-2/PCM Interface
  - Terminal Mode Type Interface to CODEC and S/U Transceiver
  - Linecard Mode Type Interface up to 8 IOM-2 channels or 32 PCM channels
  - 1536/786 kHz and 1536 kHz...4096 kHz in 512 kHz steps
  - Access to two Intercommunication channels (IC1, IC2)
  - Access to two MON channels (MON0, MON1)
  - Access to two C/I channels (CI0, CI1)
  - S/G access support
- Four On-Chip Independent Full-Duplex HDLC Formatters
  - 8 independent 8-byte FIFOs for each transmit and receive channel
- USART Interface with AutoBaud Support (1,200 bit/s - 230,400 bit/s)
  - AT-Command sensitive AutoBaud Detection

Type	Package
C165H	P-TQFP-144

1.1 Key Features

C165H is a new low-cost member of the Infineon Communication Controller family. The device has the following features:

- C166 Static Core with Peripherals including:
  - Full-static core up to 18 MIPS (@36 MHz)
  - Peripheral Event Controller (PEC) for 8 independent DMA channels
  - 16 Dynamically Programmable Priority-Level Interrupt System
  - Eight External Interrupts
  - Up to 72 SW-configurative Input/Output (I/O) Ports, some with Interrupt Capabilities
  - 8-bit or 16-bit External Data Bus
  - Multiplexed or Demultiplexed Address/Data Bus
  - Up to 8-Mbyte Linear Address Space for Code and Data
  - Five Programmable Chip-Select Lines with Wait-State Generator Logic
  - On-Chip 3,072-Byte Dual-Port SRAM for user applications
  - On-Chip 1,024-Byte Special Function Register Area
  - On-Chip PLL with Output Clock Signal
  - Five Multimode General Purpose Timers
  - On-Chip Programmable Watchdog Timer
  - Glueless Interface to EPROM, Flash EPROM and SRAM
  - Low-Power Management Supporting Idle-, Power-Down- and Sleep-Mode and additional CPU clock slow-down mode with mode control for each peripheral
  - USART interface with Auto Baud Rate detection up to 230.4 kbit/s
  - USART Baud Rate generation in asynchronous mode up to 2.25 MBaud @ 36 MHz
  - USART Baud Rate generation in synchronous mode up to 4.5 MBaud @ 36 MHz
  - USART standard Baud Rates generation with very small deviation (230.4 kBaud < 0.01%, 460.8 kBaud < 0.15 %, 691.2 kBaud < 0.04 %, 921.6 kBaud < 0.15 %) @ 36 MHz
  - High speed Serial Synchronous Channel Interface (SSC) with ALIS-3.0 and AC97 compatibility up to 18 MBaud in SSC Master Mode and up to 9 MBaud in SSC Slave Mode @ 36 MHz

- ISDN Terminal Adapter Features including:
  - Four Independent Full-Duplex HDLC Controllers
  - IOM-2/PCM interface supporting TE, LT and PCM mode
  - MON and CI1/CI2-Handler
  - Two D-Channels
  - Two B-Channels Supported
  - Concatenated 2B+D channel Support
  - Two Intercommunication Channels IC1, IC2
  - D-Channel Access Control to first IOM channel-0 by S/G bit
  - CDA Channel Access to individual IOM-2/PCM channels by SW

- On-Chip PLL for CPU clock generation
- External crystal and direct driven input clock frequency can vary between 4 and 20 MHz dependent on the CPU target clock frequency.
- Single and variable crystal clock input frequency
- Bootstrap Loader support via USART interface
- On-Chip Debug Support (OCDS)
- JTAG Boundary Scan Test support according to IEEE 1149.1
- 3.3 V single supply voltage
- 5 V (TTL-) tolerant I/Os
- C165H is available in 144-Pin P-TQFP package
- Operating temperature range: -40°C to + 85°C.

Power Management

Besides the basic power-save (power-reduction) modes Idle mode and Power down mode, the C165H offers a number of additional power management features, which can be selectively used for effective power reduction. Refer to **Table 1**.

Table 1 Overview of Power Management Modes

Mode	Description	CPU Wake-up
Running mode	The system is fully operational. All clocks and peripherals are set and enabled, as determined by software. Full power consumption.	----
Slow down mode	The CPU runs slower. The oscillator runs at a lower frequency; the clock is divided by a programmable factor (1...32). Peripherals management is possible; incl. PLL On/Off. Refer to register SYSCON 2.	Controlled by software.
Idle mode	When the processor has no active tasks to perform, it enters Idle mode by the IDLE command. All peripherals remain powered and clocked, however, peripherals management is possible. For detailed description see Chapter 18.1, "Idle Mode".	• Any interrupt • Reset
Sleep mode	The program stops execution and turns off the clocks for: • almost the entire chip, but RTC, or • the entire chip. The whole clock system is stopped. Refer to register SYSCON 1.	• All enabled external interrupts • NMI • RTC timer (in asynchronous mode) • PEC requests • ASC interface • SSC interface
Power down mode	The program stops execution (instruction PWRDN) and turns off the clocks for the CPU and for all peripherals; ports optionally.	• Reset

Note: Peripherals Management enables the user to control (via software) the clock of selected peripherals. Refer to register SYSCON 3.

- C165H power requirement in individual modes is described in **DC Characteristics, Table 77**

1.2 Logic Symbol

The C165H logic symbol is shown in **Figure 1** below.

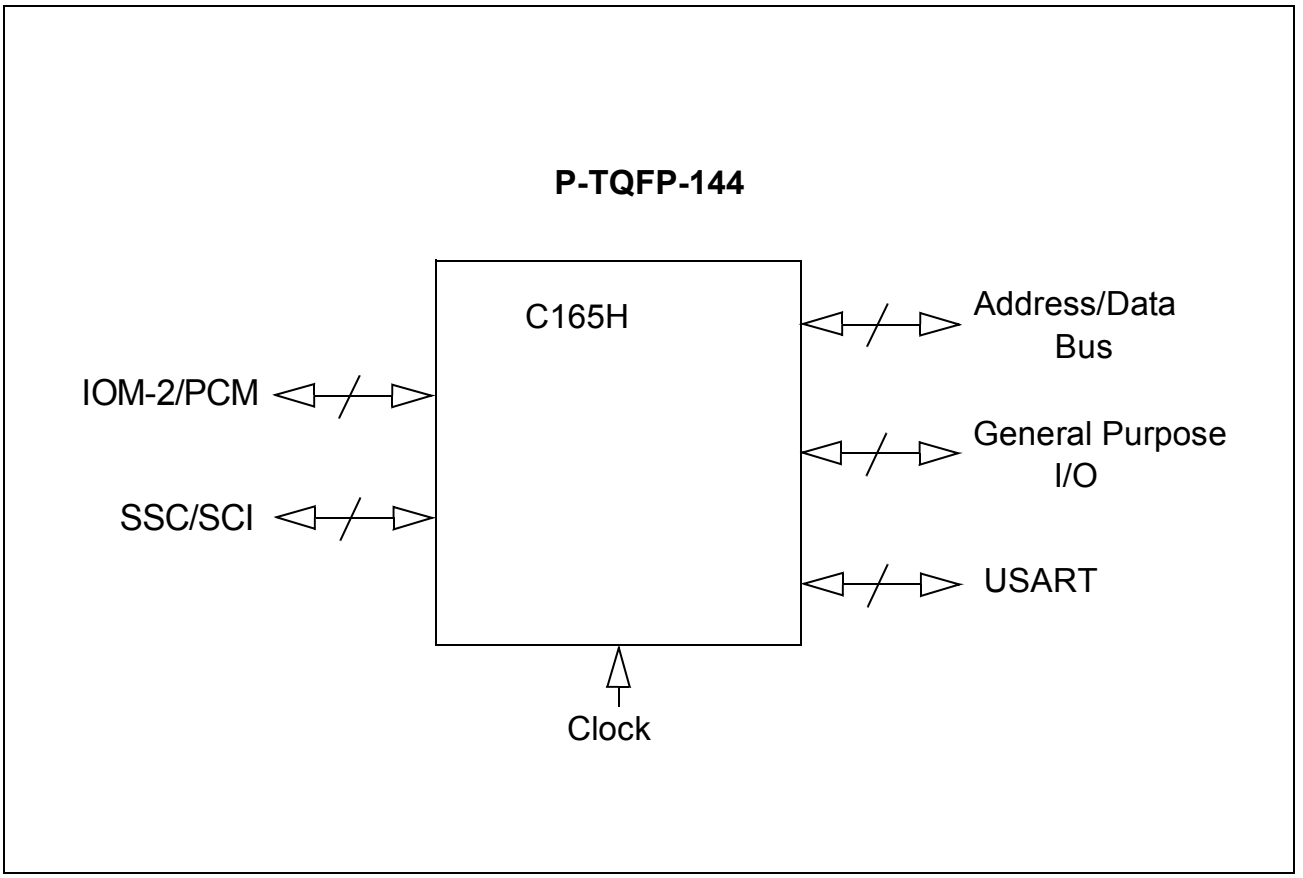

Figure 1 C165H Logic Symbol

1.3 Pinning Diagram

Figure 2 shows the pinning diagram of the C165H.

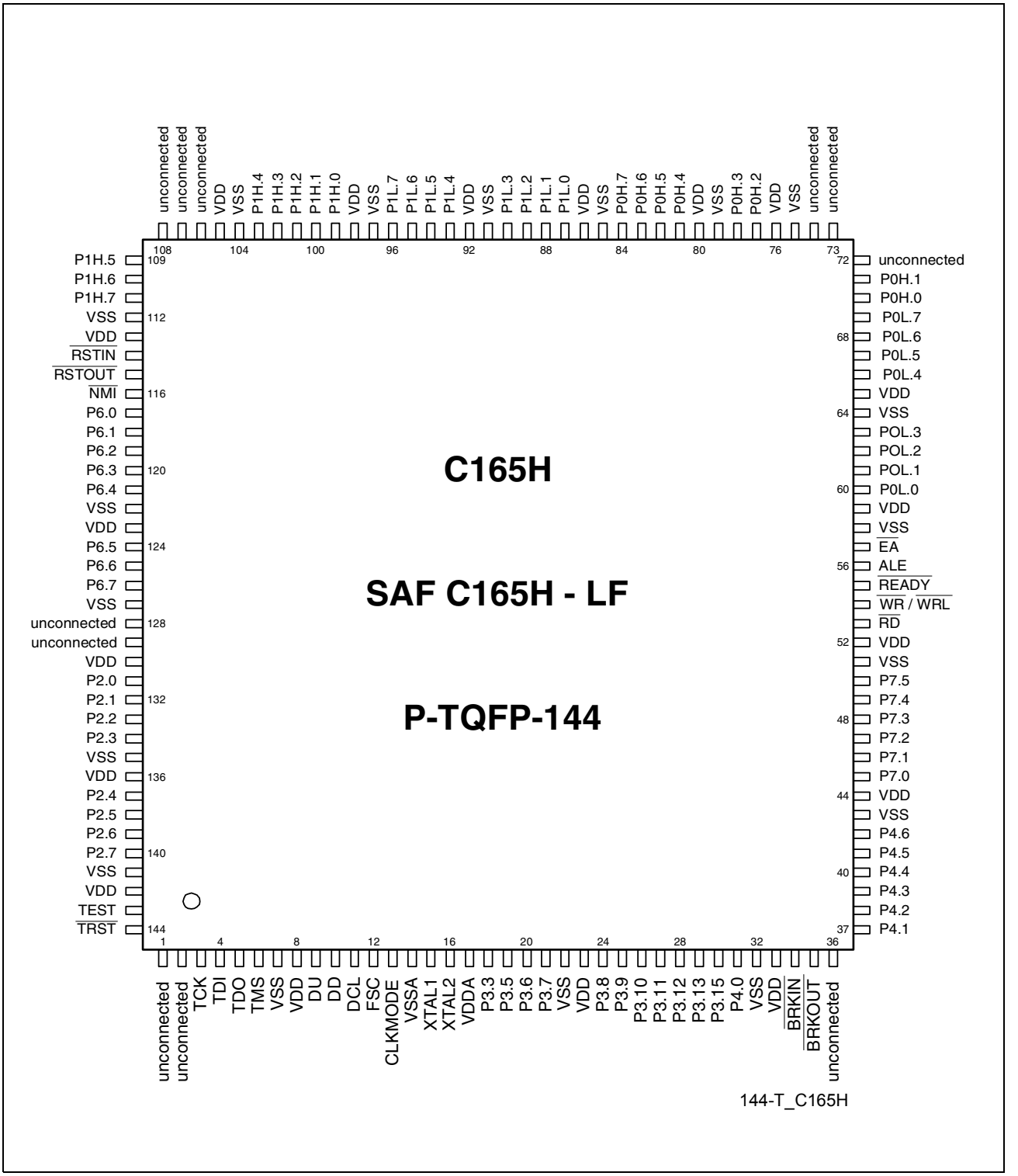

Figure 2 Pinning Diagram of the C165H

1.4 Typical Applications

1.4.1 ISDN NT and PBX Applications

C165H is designed to manage control message and data flow between the ISDN S/U transceiver and a Personal Computer. Data and message transfer is possible between either two of the following physical interfaces: IOM-2 interface or local memory via 16-bit µP-interface. Since the IOM-2 is transparently accessible, additional IOM-2 devices such as CODEC, Voice-Encrypter or Voice-Codec devices can be accessed e.g. via the second IOM-2 channel (IC1/IC2).

Figure 3 gives a general overview of the ISDN NT/PBX application for C165H.

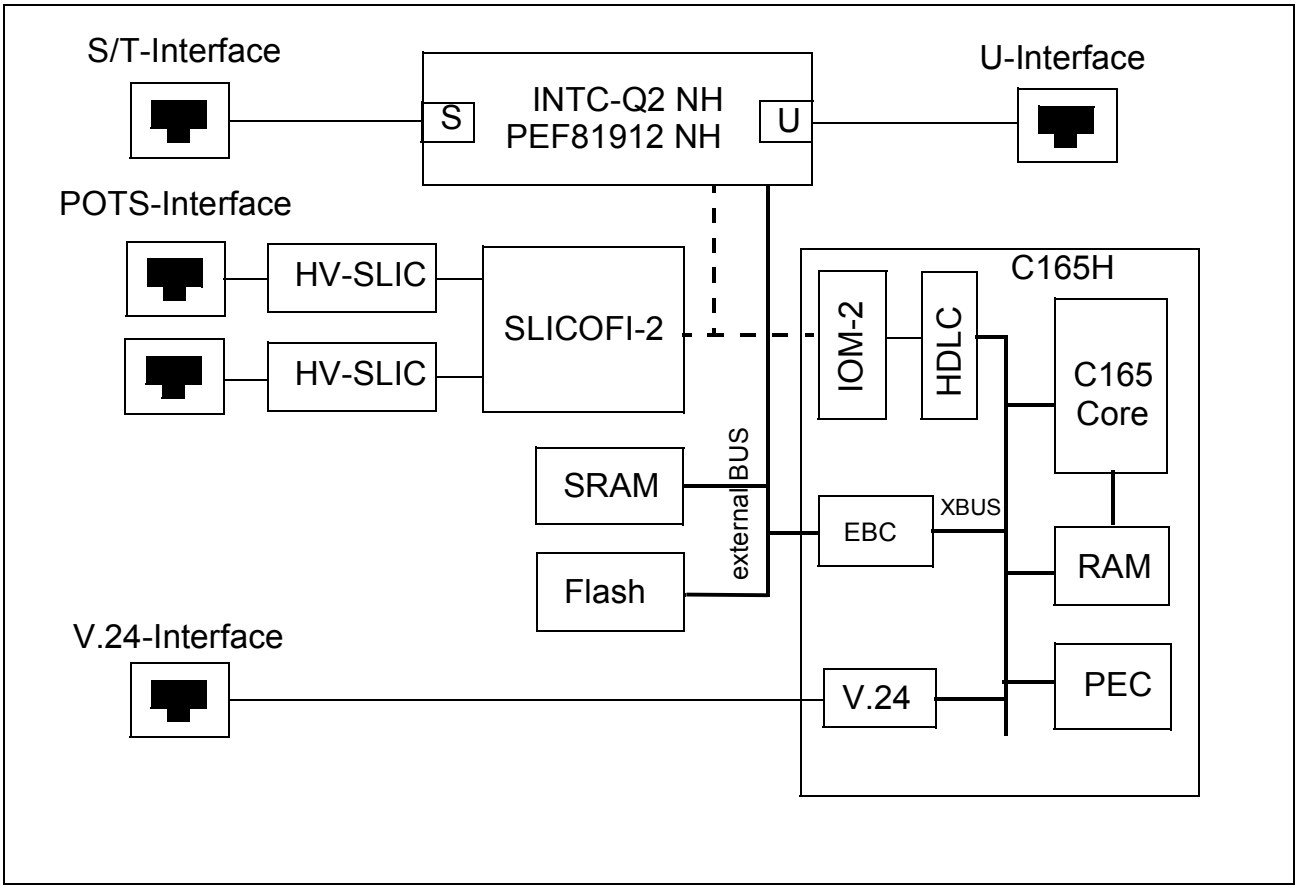

Figure 3 C165H in High Feature Intelligent Network Terminations

Note: In IOM-2 LT mode for PBX systems, when additional external D-channel controllers are used, the DRDY signal to control the access has to be connected to an external fast interrupt. Within the terminal mode, this arbitration can be done with the Stop/Go bit on IOM-2.

2 Pin Descriptions

2.1 C165H Pin Diagram

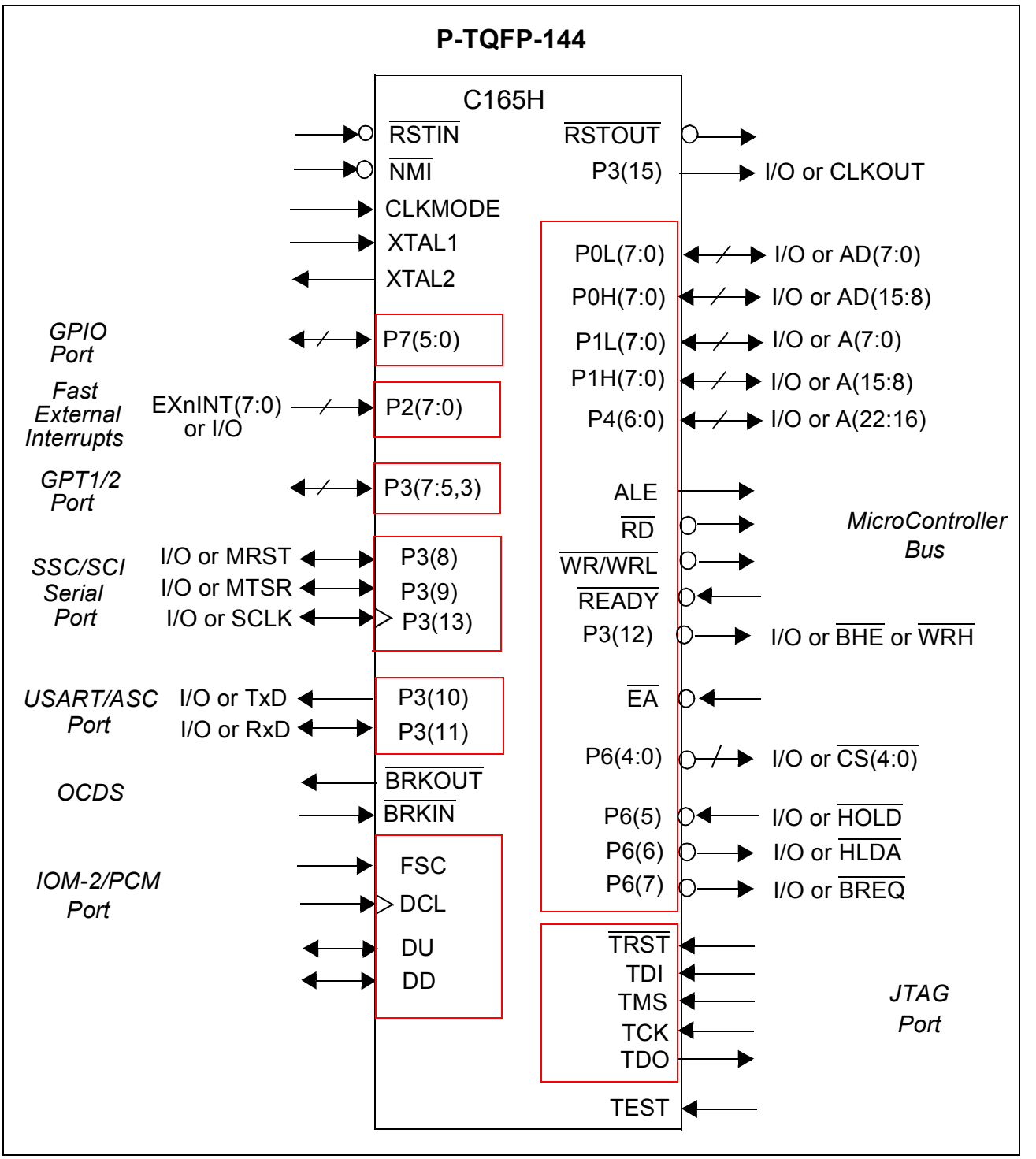

Figure 4 C165H Pin Configuration

2.2 C165H Pin Definitions and Functions

Table 2 Microprocessor Bus and Control Signals

Pin No.	Symbol	Input (I) Output (O)	Function
60-63, 66-69, 70-71, 77-78, 81-84	PORT0: P0L0-P0L7, P0H0-P0H7	I/O	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bitwise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L0-P0L7: D0-D7 D0-D7 P0H0-P0H7: I/O D8-D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L0-P0L7: AD0-AD7 AD0-AD7 P0H0-P0H7: A8-A15 AD8-AD15
87-90, 93-96, 99-103, 109-111	PORT1: P1L0-P1L7, P1H0-P1H7	I/O	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bitwise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode (see Chapter 7.3).

Table 2 Microprocessor Bus and Control Signals (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
31, 37-42	P4.0 - P4.6	I/O	PORT4 is an 7-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port4 can be used to output the segment address lines:
		O	P40 A16 Least Significant Segment Address Line
			... ...
		O	P4.6 A22 Most Significant Segment Address Line
114	$\overline{\text{RSTIN}}$	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running resets the device. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}.
115	$\overline{\text{RSTOUT}}$	O	Internal Reset Indication Output. This pin is set to a low level when the C165H is executing either a hardware-, software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the C165H has initialized itself.
116	$\overline{\text{NMI}}$	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the CPU to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the device will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Table 2 Microprocessor Bus and Control Signals (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
117-121, 124-126	P6.0- P6.7	O I/O	Port6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port6 outputs can be configured as push/pull or open-drain drivers.
		O	P6.0 $\overline{CS0}$ Chip Select 0 Output
		...	... ...
		O	P6.4 $\overline{CS4}$ Chip Select 4 Output
		I	P6.5 $\overline{HOLD}$ External Master Hold Request Input
		O	P6.6 $\overline{HLDA}$ Hold Acknowledge Output
		O	P6.7 $\overline{BREQ}$ Bus Request Output
131-134, 137-140	P2.0- P2.7	I/O	PORT2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port2 outputs can be configured as push/pull or open-drain drivers.
		I	P2.0 EX0IN Fast External Interrupt 0 Input
		I	P2.7 EX7IN Fast External Interrupt 7 Input
53	$\overline{RD}$	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
54	$\overline{WR}$/$\overline{WRL}$	O	External Memory Write Strobe. In $\overline{WR}$ mode this pin is activated for every external data write access. In $\overline{WRL}$ mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
56	ALE	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.

Table 2 Microprocessor Bus and Control Signals (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
55	$\overline{\text{READY}}$	I	Ready Input. When the ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to an low level.
57	$\overline{\text{EA}}$	I	External Access Enable pin. A low level at this pin during and after Reset forces the CPU to begin instruction execution out of external memory. **Note:** This pin must always be set to '0'.
45-50	P7.0- P7.5	I/O	PORT7 is an 6-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port7 outputs are push/pull drivers. P7.0 GPIO0 ... P7.5 GPIO5

Table 3 General Purpose I/O and Control Signals

Pin No.	Symbol	Input (I) Output (O)	Function
18-21, 24-30	P3.3, P3.5- P3.13, P3.15	I/O I/O I/O	PORT3 is a 11-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port3 outputs can be configured as push/pull or open-drain drivers. The following PORT3 pins also serve for alternate functions:
		O	P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output
		I	P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture
		I	Input for Timer 3 T3EUD Input for Timer 2 T2EUD
		I	P3.6 T3IN GPT1 Timer T3 Count/Gate/ Input
		I/O	P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture
		I/O	P3.8 MRST SSC Master-Rec./Slave-Transmit I/O
		O	P3.9 MTSR SSC Master-Transmit/Slave-Rec. O/I
		I/O	P3.10 TxD0 ASC Clock/Data Output (Async./Sync.)
		O	P3.11 RxD0 ASC Data Input (Async.) or I/O (Sync.)
		O	P3.12 $\overline{BHE}$ External Memory High Byte Enable Signal
		I/O	$\overline{WRH}$ External Memory High Byte Write Strobe
		O	P3.13 SCLK SSC Master Clock Output/ Slave Clock Input (CPU Clock)
			P3.15 CLKOUT System Clock Output (CPU Clock)

Table 4 IOM-2 Interface Signals

Pin No.	Symbol	Input (I) Output (O)	Function
9	DU	I/O, OD	IOM-2 Data Upstream Signal pin. (From subscriber to network). For the pin configured as input, the output driver is put into high-impedance state. Open-drain.
10	DD	I/O, OD	IOM-2 Data Downstream Signal pin. (From network to subscriber). For the pin configured as input, the output driver is put into high-impedance state. Open-drain.
11	DCL	I	IOM-2 Data Clock Signal Input pin
12	FSC	I	IOM-2 Frame Sync. Clock Signal Input pin

Table 5 Clock Interface Signals

Pin No.	Symbol	Input (I) Output (O)	Function
15	XTAL1	I	External crystal input to the on-chip oscillator. Clock input for direct driven clock without using an external crystal. Function is determined by the CLKMODE pin.
16	XTAL2	O	Output from the oscillator amplifier circuit. To clock the C165H from an external source, drive XTAL1, while XTAL2 leaving unconnected. Minimum and maximum high/ low and rise/fall times specified in the AC characteristics must be observed.
13	CLKMODE	I	Clock Mode Select pin. CLKMODE must be set to LOW if an external crystal is used. Set to HIGH signal enables the direct clock input path and switches the internal oscillator in power down mode.

Table 6 Boundary Scan / JTAG / Test Interface Signals/OCDS

Pin No.	Symbol	Input (I) Output (O)	Function
3	TCK	I	Boundary Scan Test Clock Input. There is no internal pull device implemented. During normal operation, it is recommended to connect TCK to VSS.
4	TDI	I	Boundary Scan Test Data Input. An internal pull-up device is connected to TDI. During normal operation, TDI can be left open.
5	TDO	O	Boundary Scan Test Data Output. During normal operation, the output TDO can be left open.
6	TMS	I	Boundary Scan Test Mode Select Input, internal pull-up.
144	$\overline{\text{TRST}}$	I	Boundary Scan Test Reset. There is an internal pull-up device implemented. $\overline{\text{TRST}}$ is low active, which means the boundary scan tap controller resets while $\overline{\text{TRST}}$ = ’0’. For normal operation, • $\overline{\text{TRST}}$ can be connected to LOW signal (using ’0’ signal or external pull-down device) to keep the tap controller in reset mode, or • $\overline{\text{TRST}}$ can be left open. In this case, the reset is performed using the TMS/TCK signals according to IEEE 1149.1 In boundary scan test mode, $\overline{\text{TRST}}$ can be left open, since the internal pull-up device provides the necessary HIGH signal.
143	TEST	I	Test Mode Enable Pin. HIGH signal enables the chip internal test mode. **Note:** In normal operation, TEST must be connected to VSS (LOW signal) since no internal Pull-Down resistor is provided.