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32-Bit

TC1767

32-Bit Single-Chip Microcontroller

Data Sheet

V1.4 2012-07

Microcontrollers



**Edition 2012-07**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

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# 32-Bit

# TC1767

32-Bit Single-Chip Microcontroller

Data Sheet

V1.4 2012-07

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**TC1767 Data Sheet****Revision History: V1.4 2012-07**

Previous Versions: V1.3

Page	Subjects (major changes since last revision)
<b>Page 6</b>	Salescode for Copper-bonded device is added

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## 1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 8 Kbyte Parameter Memory (PRAM)
  - 16 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 72 Kbyte Data Memory (LDRAM)
  - 24 Kbyte Code Scratchpad Memory (SPRAM)
  - 2 Mbyte Program Flash Memory (PFlash)
  - 64 Kbyte Data Flash Memory (DFlash, represents 16 Kbyte EEPROM)
  - Instruction Cache: up to 8 Kbyte (ICACHE, configurable)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 8-Channel DMA Controller
- Sophisticated interrupt system with  $2 \times 255$  hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 2 CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC

---

## Summary of Features

- 2 independent kernels (ADC0, ADC1)
- Analog supply voltage range from 3.3 V to 5 V (single supply)
- Performance for 12 bit resolution (@ $f_{\text{ADCI}} = 10 \text{ MHz}$ )
- 4 different FADC input channels
- Extreme fast conversion, 21 cycles of  $f_{\text{FADC}}$  clock (262.5 ns @  $f_{\text{FADC}} = 80 \text{ MHz}$ )
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 88 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1767ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range:  $-40^{\circ}$  to  $+125^{\circ}\text{C}$
- Package variant: PG-LQFP-176-5

Summary of Features

**Ordering Information**

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1767 please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

This document describes the derivatives of the device. The **Table 1** enumerates these derivatives and summarizes the differences.

**Table 1 TC1767 Derivative Synopsis**

Derivative	Ambient Temperature Range	CPU frequency	Wire Bond Material
SAK-TC1767-256F133HL	T <sub>A</sub> = -40°C to +125°C	133 MHz	Gold
SAK-TC1767-256F80HL	T <sub>A</sub> = -40°C to +125°C	80 MHz	Gold
SAK-TC1767-256F133HR	T <sub>A</sub> = -40°C to +125°C	133 MHz	Copper

## 2 Introduction

This Data Sheet describes the Infineon TC1767, a 32-bit microcontroller DSP, based on the Infineon TriCore Architecture.

### 2.1 About this Document

This document is designed to be read primarily by design engineers and software engineers who need a detailed description of the interactions of the TC1767 functional units, registers, instructions, and exceptions.

This TC1767 Data Sheet describes the features of the TC1767 with respect to the TriCore Architecture. Where the TC1767 directly implements TriCore architectural functions, this manual simply refers to those functions as features of the TC1767. In all cases where this manual describes a TC1767 feature without referring to the TriCore Architecture, this means that the TC1767 is a direct implementation of the TriCore Architecture.

Where the TC1767 implements a subset of TriCore architectural features, this manual describes the TC1767 implementation, and then describes how it differs from the TriCore Architecture. Such differences between the TC1767 and the TriCore Architecture are documented in the section covering each such subject.

#### 2.1.1 Related Documentations

A complete description of the TriCore architecture is found in the document entitled "TriCore Architecture Manual". The architecture of the TC1767 is described separately this way because of the configurable nature of the TriCore specification: Different versions of the architecture may contain a different mix of systems components. The TriCore architecture, however, remains constant across all derivative designs in order to preserve compatibility.

This Data Sheets together with the "TriCore Architecture Manual" are required to understand the complete TC1767 micro controller functionality.

#### 2.1.2 Text Conventions

This document uses the following text conventions for named components of the TC1767:

- Functional units of the TC1767 are given in plain UPPER CASE. For example: "The SSC supports full-duplex and half-duplex synchronous communication".
- Pins using negative logic are indicated by an overline. For example: "The external reset pin,  $\overline{\text{ESR0}}$ , has a dual function."
- Bit fields and bits in registers are in general referenced as "Module\_Register name.Bit field" or "Module\_Register name.Bit". For example: "The Current CPU Priority Number bit field CPU\_ICR.CCPN is cleared". Most of the

## Introduction

register names contain a module name prefix, separated by an underscore character “\_” from the actual register name (for example, “ASC0\_CON”, where “ASC0” is the module name prefix, and “CON” is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.

- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name “MSGCFGn” refers to multiple “MSGCFG” registers with variable n. The bounds of the variables are always given where the register expression is first used (for example, “n = 0-31”), and are repeated as needed in the rest of the text.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter “H”, as in 100<sub>H</sub>. Binary constants are suffixed with a subscript letter “B”, as in: 111<sub>B</sub>.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as “NAME[A:B]”, which defines a range for the named group from B to A. Individual bits, signals, or pins are given as “NAME[C]” where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].
- Units are abbreviated as follows:
  - **MHz** = Megahertz
  - **μs** = Microseconds
  - **kBaud, kbit** = 1000 characters/bits per second
  - **MBaud, Mbit** = 1,000,000 characters/bits per second
  - **Kbyte, KB** = 1024 bytes of memory
  - **Mbyte, MB** = 1048576 bytes of memory

In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576, and μ scales by .000001. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.
- Data format quantities are defined as follows:
  - **Byte** = 8-bit quantity
  - **Half-word** = 16-bit quantity
  - **Word** = 32-bit quantity
  - **Double-word** = 64-bit quantity

### 2.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in [Table 2](#).

**Table 2 Bit Function Terminology**

Function of Bits	Description
<b>Unimplemented, Reserved</b>	Register bit fields named <b>0</b> indicate unimplemented functions with the following behavior. <ul style="list-style-type: none"> <li>• Reading these bit fields returns 0.</li> <li>• These bit fields should be written with 0 if the bit field is defined as r or rh.</li> <li>• These bit fields have to be written with 0 if the bit field is defined as rw.</li> </ul> These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
<b>rw</b>	The bit or bit field can be read and written.
<b>rwh</b>	As rw, but bit or bit field can be also set or reset by hardware.
<b>r</b>	The bit or bit field can only be read (read-only).
<b>w</b>	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
<b>rh</b>	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.
<b>s</b>	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
<b>f</b>	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

### 2.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in [Table 3](#) are used.



**Table 3 Access Terms**

Symbol	Description
U	Access Mode: Access permitted in User Mode 0 or 1.
	Reset Value: Value or bit is not changed by a reset operation.
SV	Access permitted in Supervisor Mode.
R	Read-only register.
32	Only 32-bit word accesses are permitted to this register/address range.
E	Endinit-protected register/address.
PW	Password-protected register/address.
NC	No change, indicated register is not changed.
BE	Indicates that an access to this address range generates a Bus Error.
nBE	Indicates that no Bus Error is generated when accessing this address range, even though it is either an access to an undefined address or the access does not follow the given rules.
nE	Indicates that no Error is generated when accessing this address or address range, even though the access is to an undefined address or address range. True for CPU accesses (MTCR/MFCR) to undefined addresses in the CSFR range.

### 2.1.5 Abbreviations and Acronyms

The following acronyms and terms are used in this document:

ADC	Analog-to-Digital Converter
AGPR	Address General Purpose Register
ALU	Arithmetic and Logic Unit
ASC	Asynchronous/Synchronous Serial Controller
BCU	Bus Control Unit
BROM	Boot ROM & Test ROM
CAN	Controller Area Network
CMEM	PCP Code Memory
CISC	Complex Instruction Set Computing
CPS	CPU Slave Interface
CPU	Central Processing Unit

CSA	Context Save Area
CSFR	Core Special Function Register
DAP	Device Access Port
DAS	Device Access Server
DCACHE	Data Cache
DFLASH	Data Flash Memory
DGPR	Data General Purpose Register
DMA	Direct Memory Access
DMI	Data Memory Interface
ERU	External Request Unit
EMI	Electro-Magnetic Interference
FADC	Fast Analog-to-Digital Converter
FAM	Flash Array Module
FCS	Flash Command State Machine
FIM	Flash Interface and Control Module
FPI	Flexible Peripheral Interconnect (Bus)
FPU	Floating Point Unit
GPIO	General Purpose Input/Output
GPR	General Purpose Register
GPTA	General Purpose Timer Array
ICACHE	Instruction Cache
I/O	Input / Output
JTAG	Joint Test Action Group = IEEE1149.1
LBCU	Local Memory Bus Control Unit
LDRAM	Local Data RAM
LFI	Local Memory-to-FPI Bus Interface
LMB	Local Memory Bus
LTC	Local Timer Cell
MLI	Micro Link Interface
MMU	Memory Management Unit
MSB	Most Significant Bit
MSC	Micro Second Channel

NC	Non Connect
NMI	Non-Maskable Interrupt
OCDS	On-Chip Debug Support
OVRAM	Overlay Memory
PCP	Peripheral Control Processor
PMU	Program Memory Unit
PLL	Phase Locked Loop
PFLASH	Program Flash Memory
PMI	Program Memory Interface
PMU	Program Memory Unit
PRAM	PCP Parameter RAM
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
SBCU	System Peripheral Bus Control Unit
SCU	System Control Unit
SFR	Special Function Register
SPB	System Peripheral Bus
SPRAM	Scratch-Pad RAM
SRAM	Static Data Memory
SRN	Service Request Node
SSC	Synchronous Serial Controller
STM	System Timer
WDT	Watchdog Timer

## 2.2 System Architecture of the TC1767

The TC1767 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1767 include:

- Program Memory Unit – instruction memory and instruction cache
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

TC1767 clock frequencies:

- Maximum CPU clock frequency: 133 MHz<sup>1)</sup>
- Maximum PCP clock frequency: 133 MHz<sup>2)</sup>
- Maximum SPB frequency: 80 MHz<sup>3)</sup>

The TC1767 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor, a DMA controller and several on-chip peripherals. The TC1767 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1767 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1767, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1767 ports are reserved for these peripheral units to communicate with the external world.

1) For CPU frequencies > 80 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means:  $f_{SPB} = 0.5 * f_{CPU}$

2) For PCP frequencies > 80 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means:  $f_{SPB} = 0.5 * f_{PCP}$

3) CPU 1:1 Mode means:  $f_{SPB} = f_{CPU}$ . PCP 1:1 mode means:  $f_{SPB} = f_{PCP}$

### 2.2.1 TC1767 Block Diagram

Figure 1 shows the block diagram of the TC1767.

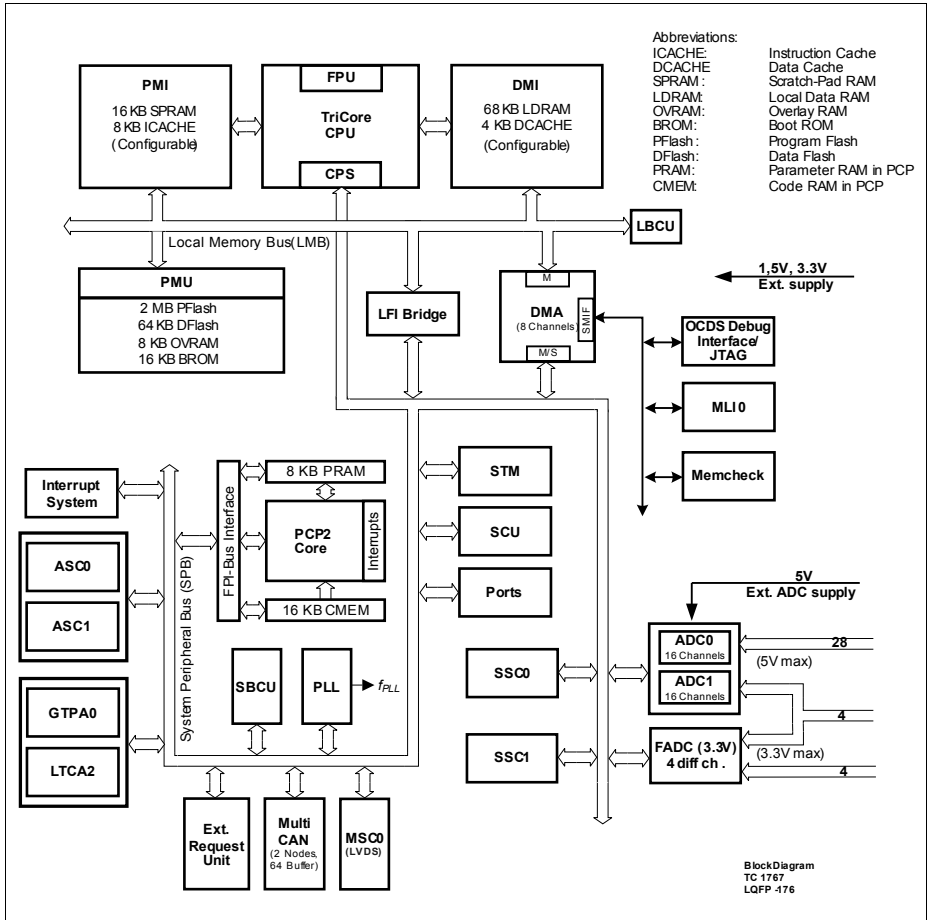


Figure 1 TC1767 Block Diagram

## 2.2.2 System Features of the TC1767 device

The TC1767 has the following features:

### Packages

- PG-LQFP-176-5 package, 0.5 mm pitch

### Clock Frequencies

- Maximum CPU clock frequency: 133 MHz<sup>1)</sup>
- Maximum PCP clock frequency: 133 MHz<sup>2)</sup>
- Maximum SPB clock frequency: 80 MHz<sup>3)</sup>

1) For CPU frequencies > 80 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means:  $f_{SPB} = 0.5 * f_{CPU}$

2) For PCP frequencies > 80 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means:  $f_{SPB} = 0.5 * f_{PCP}$

3) CPU 1:1 Mode means:  $f_{SPB} = f_{CPU}$ . PCP 1:1 mode means:  $f_{SPB} = f_{PCP}$



### 2.2.3 On Chip CPU Cores

The TC1767 includes a high Performance CPU and a Peripheral Control Processor.

#### 2.2.3.1 High-performance 32-bit CPU

This chapter gives an overview about the TriCore 1 architecture.

##### TriCore (TC1.3.1) Architectural Highlights

- Unified RISC MCU/DSP
- 32-bit architecture with 4 Gbytes unified data, program, and input/output address space
- Fast automatic context-switching
- Multiply-accumulate unit
- Floating point unit
- Saturating integer arithmetic
- High-performance on-chip peripheral bus (FPI Bus)
- Register based design with multiple variable register banks
- Bit handling
- Packed data operations
- Zero overhead loop
- Precise exceptions
- Flexible power management

##### High-efficiency TriCore Instruction Set

- 16/32-bit instructions for reduced code size
- Data types include: Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double-word integers, and IEEE-754 single-precision floating point
- Data formats include: Bit, 8-bit byte, 16-bit half-word, 32-bit word, and 64-bit double-word data formats
- Powerful instruction set
- Flexible and efficient addressing mode for high code density

##### Integrated CPU related On-Chip Memories

- Instruction memory: 24 KB total. After reset, configured into:<sup>1)</sup>
  - 24 Kbyte Scratch-Pad RAM (SPRAM)
  - 0 Kbyte Instruction Cache (ICACHE)
- Data memory: 72 KB total. After reset, configured into:<sup>1)</sup>

<sup>1)</sup> Software configurable. Available options are described in the CPU chapter.

- 72 Kbyte Local Data RAM (LDRAM)
- 0 Kbyte Data Cache (DACHE)
- On-chip SRAMs with parity error detection

### 2.2.3.2 High-performance 32-bit Peripheral Control Processor

The PCP is a flexible Peripheral Control Processor optimized for interrupt handling and thus unloading the CPU.

#### Features

- Data move between any two memory or I/O locations
- Data move with predefined limit supported
- Read-Modify-Write capabilities
- Full computation capabilities including basic MUL/DIV
- Read/move data and accumulate it to previously read data
- Read two data values and perform arithmetic or logical operation and store result
- Bit-handling capabilities (testing, setting, clearing)
- Flow control instructions (conditional/unconditional jumps, breakpoint)
- Dedicated Interrupt System
- PCP SRAMs with parity error detection
- PCP/FPI clock mode 1:1 and 2:1 available

#### Integrated PCP related On-Chip Memories

- 16 Kbyte Code Memory (CMEM)
- 8 Kbyte Parameter Memory (PRAM)
- 

## 2.3 On Chip System Units

The TC1767 micro controller offers several versatile on-chip system peripheral units such as DMA controller, embedded Flash module, interrupt system and ports.

### 2.3.1 Flexible Interrupt System

The TC1767 includes a programmable interrupt system with the following features:

#### Features

- Fast interrupt response
- Hardware arbitration
- Independent interrupt systems for CPU and PCP
- Programmable service request nodes (SRNs)
- Each SRN can be mapped to the CPU or PCP interrupt system

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- Flexible interrupt-prioritizing scheme with 255 interrupt priority levels per SRN to choose from

### 2.3.2 Direct Memory Access Controller

The TC1767 includes a fast and flexible DMA controller with independent DMA channels (DMA Move engine).

#### Features

- independent DMA channels
  - Up to 16 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within the DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- 3-level programmable priority of the DMA Sub-Block at the on chip bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
  - Two shadow register modes (with / w/o automatic re-set and direct write access).
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Data block move supports > 32 Kbyte moves per DMA transaction
  - Circular buffer addressing mode with flexible circular buffer sizes
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channel is also implemented in the DMA module)
- DMA module is working on SPB frequency, LMB interface on LMB frequency.
- Dependant on the target/destination address, Read/write requests from the Move Engine are directed to the SPB, LMB, MLI or to the the Cerberus.

### 2.3.3 System Timer

The TC1767's STM is designed for global system timing applications requiring both high precision and long range.

#### Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by maximum 80 MHz ( $= f_{\text{SYS}}$ , default after reset  $= f_{\text{SYS}}/2$ )
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM is not reset.
- STM can be halted in debug/suspend mode

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum clock period is  $2^{56} \times f_{\text{STM}}$ . At  $f_{\text{STM}} = 80$  MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

In case of a power-on reset, a watchdog reset, or a software reset, the STM is reset. After one of these reset conditions, the STM is enabled and immediately starts counting up. It is not possible to affect the content of the timer during normal operation of the TC1767. The timer registers can only be read but not written to.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1767 (initiated by writing an appropriate value to STM\_CLC register), the STM clock is stopped but all registers are still readable.

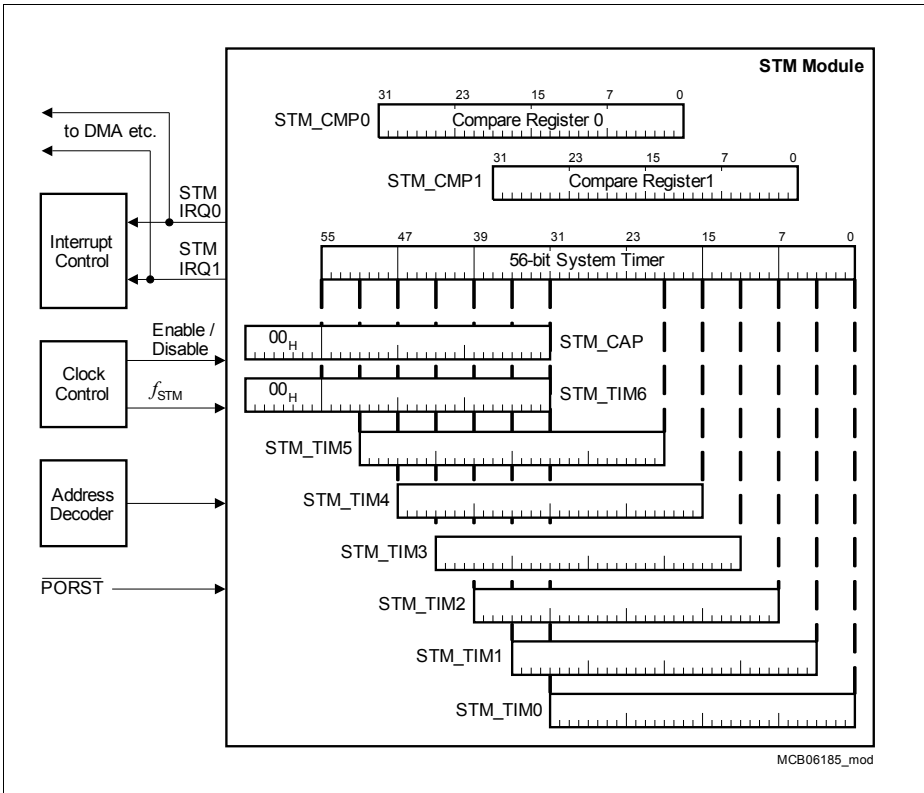
Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM\_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM\_TIM0 to STM\_TIM5 is read. Thus, STM\_CAP holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the content of the STM\_CAP to get the complete timer value.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM\_CMP0 and STM\_CMP1 registers. Interrupts can be

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generated on a compare match of the STM with the STM\_CMP0 or STM\_CMP1 registers.

**Figure 2** provides an overview on the STM module. It shows the options for reading parts of STM content.



**Figure 2 General Block Diagram of the STM Module Registers**

### 2.3.4 System Control Unit

The following SCU introduction gives an overview about the TC1767 System Control Unit (SCU).

#### 2.3.4.1 Clock Generation Unit

The Clock Generation Unit (CGU) allows a very flexible clock generation for the TC1767. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption.

#### 2.3.4.2 Features of the Watchdog Timer

The main features of the WDT are summarized here.

- 16-bit Watchdog counter
- Selectable input frequency:  $f_{FPI}/256$  or  $f_{FPI}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1767 is held in reset until a system / class 0 reset occurs.

#### 2.3.4.3 Reset Operation

The following reset request triggers are available:

- 1 External power-on hardware reset request trigger;  $\overline{\text{PORST}}$ , (cold reset)
- 2 External System Request reset triggers;  $\overline{\text{ESR0}}$  and  $\overline{\text{ESR1}}$  (warm reset)
- Watchdog Timer (WDT) reset request trigger, (warm reset)
- Software reset (SW), (warm reset)
- Debug (OCDS) reset request trigger, (warm reset)
- JTAG reset (special reset)
- Resets via the JTAG interface

*Note: The JTAG and OCDS resets are described in the OCDS chapter.*

There are two basic types of reset request triggers: