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8-Bit

SAL-XC886CLM

8-Bit Single Chip Microcontroller

Data Sheet

V1.0 2010-05

Microcontrollers

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Page	Subjects (major changes since last revision)

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Table of Contents

1 Summary of Features

The SAL-XC886 has the following features:

- High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- On-chip memory
  - 12 Kbytes of Boot ROM
  - 256 bytes of RAM
  - 1.5 Kbytes of XRAM
  - 24/32 Kbytes of Flash
    (includes memory protection strategy)
- I/O port supply at 5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(more features on next page)

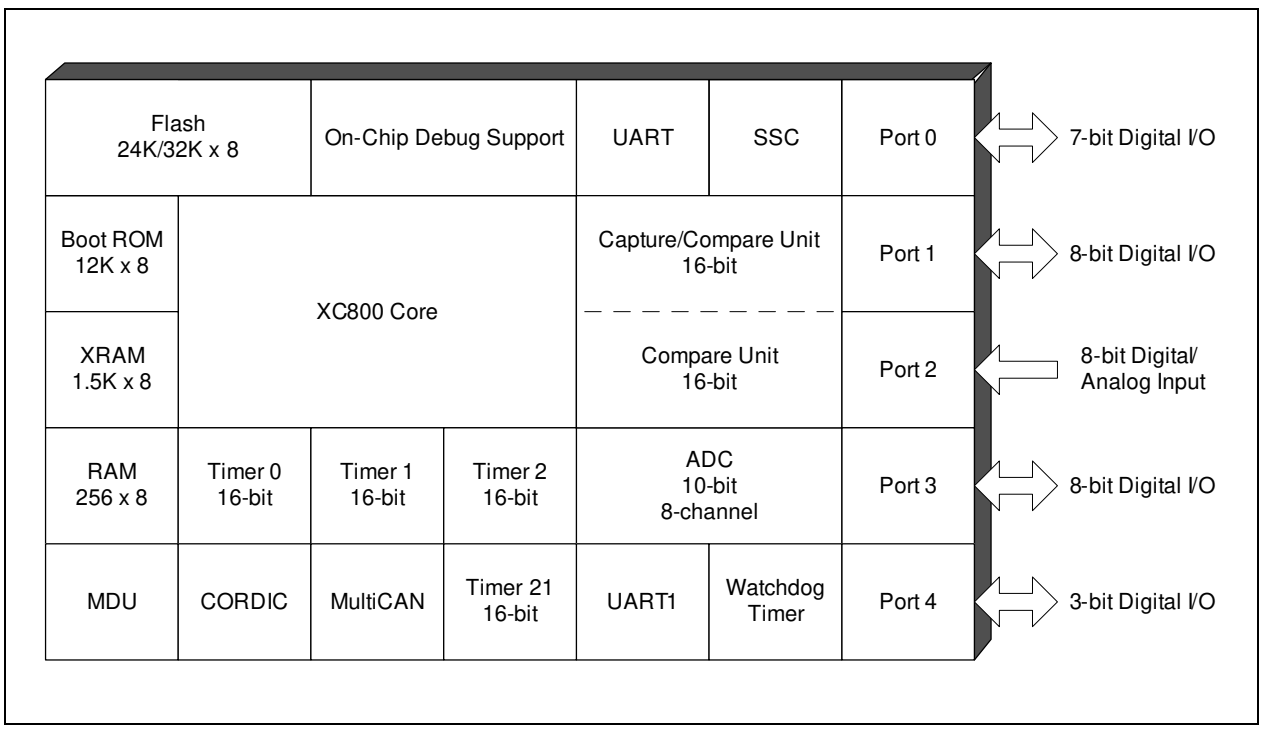

Figure 1 SAL-XC886 Functional Units

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- Power saving modes
  - slow-down mode
  - idle mode
  - power-down mode with wake-up capability via RXD or EXINT0
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Six ports
  - Up to 48 pins as digital I/O
  - 8 pins as digital/analog input
- 8-channel, 10-bit ADC
- Four 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- Software libraries to support floating point and MDU calculations
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Capture/compare unit for PWM signal generation (CCU6)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
  - 1 Kbyte of monitor ROM (part of the 12-Kbyte Boot ROM)
  - 64 bytes of monitor RAM
- Package:
  - PG-TQFP-48
- Temperature range T_A:
  - SAL (-40 to 150 °C)

SAL-XC886 Variant Devices

The SAL-XC886 product family features devices with different configurations and program memory sizes, to offer cost-effective solutions for different application requirements.

The list of SAL-XC886 device configurations are summarized in **Table 1**.

Table 1 Device Profile

Device Type	Sales Type	Program Memory (Kbytes)	CAN Module	LIN BSL Support	MDU Module
Flash	SAL-XC886-8FFA 5V	32	No	No	No
	SAL-XC886C-8FFA 5V	32	Yes	No	No
	SAL-XC886CM-8FFA 5V	32	Yes	No	Yes
	SAL-XC886LM-8FFA 5V	32	No	Yes	Yes
	SAL-XC886CLM-8FFA 5V	32	Yes	Yes	Yes
	SAL-XC886-6FFA 5V	24	No	No	No
	SAL-XC886C-6FFA 5V	24	Yes	No	No
	SAL-XC886CM-6FFA 5V	24	Yes	No	Yes
	SAL-XC886LM-6FFA 5V	24	No	Yes	Yes
	SAL-XC886CLM-6FFA 5V	24	Yes	Yes	Yes

Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term SAL-XC886 throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the SAL-XC886, please refer to your responsible sales representative or your local distributor.

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the SAL-XC886.

2.1 Block Diagram

The block diagram of the SAL-XC886 is shown in **Figure 2**.

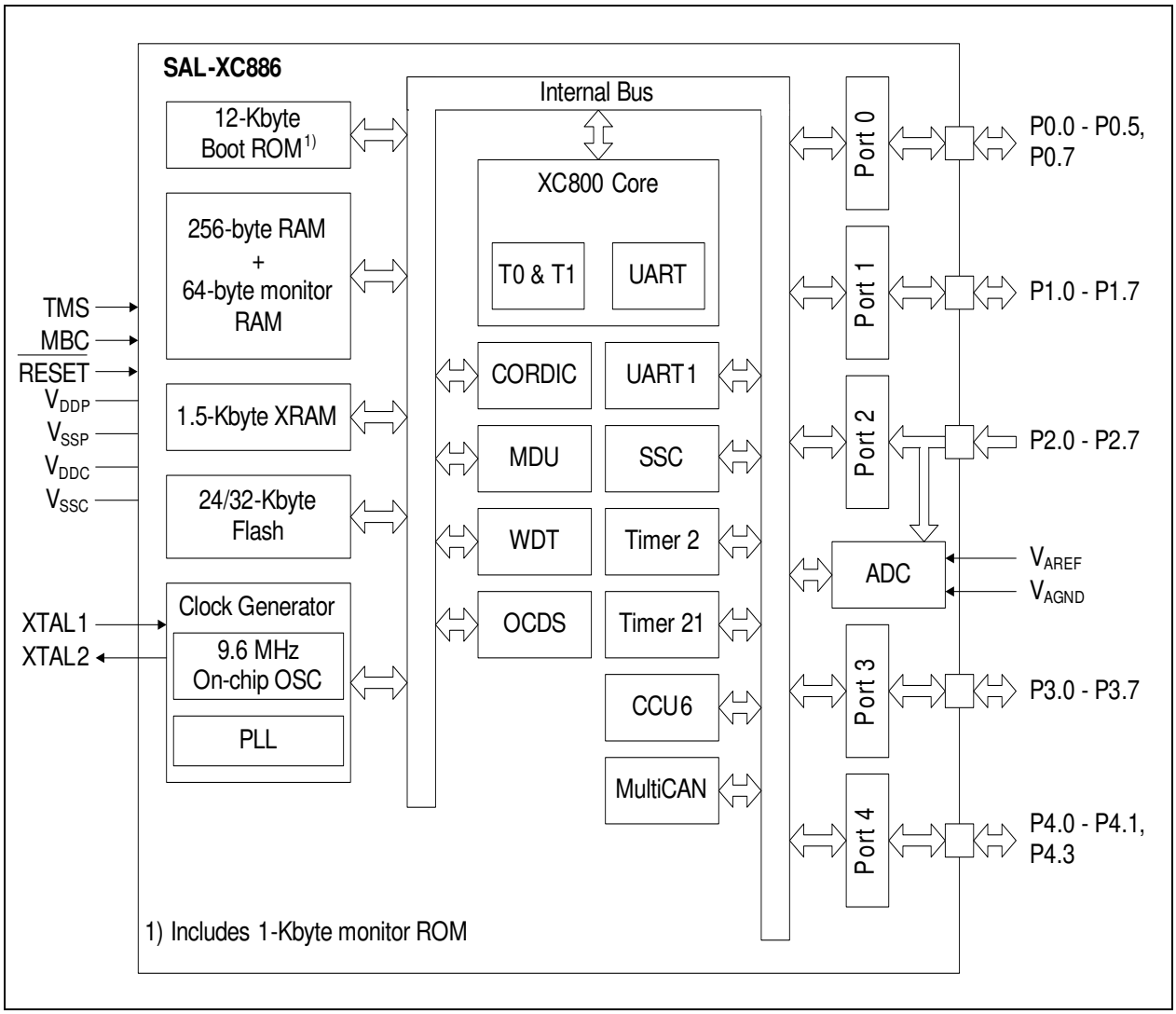

Figure 2 SAL-XC886 Block Diagram

2.2 Logic Symbol

The logic symbols of the SAL-XC886 are shown in **Figure 3**.

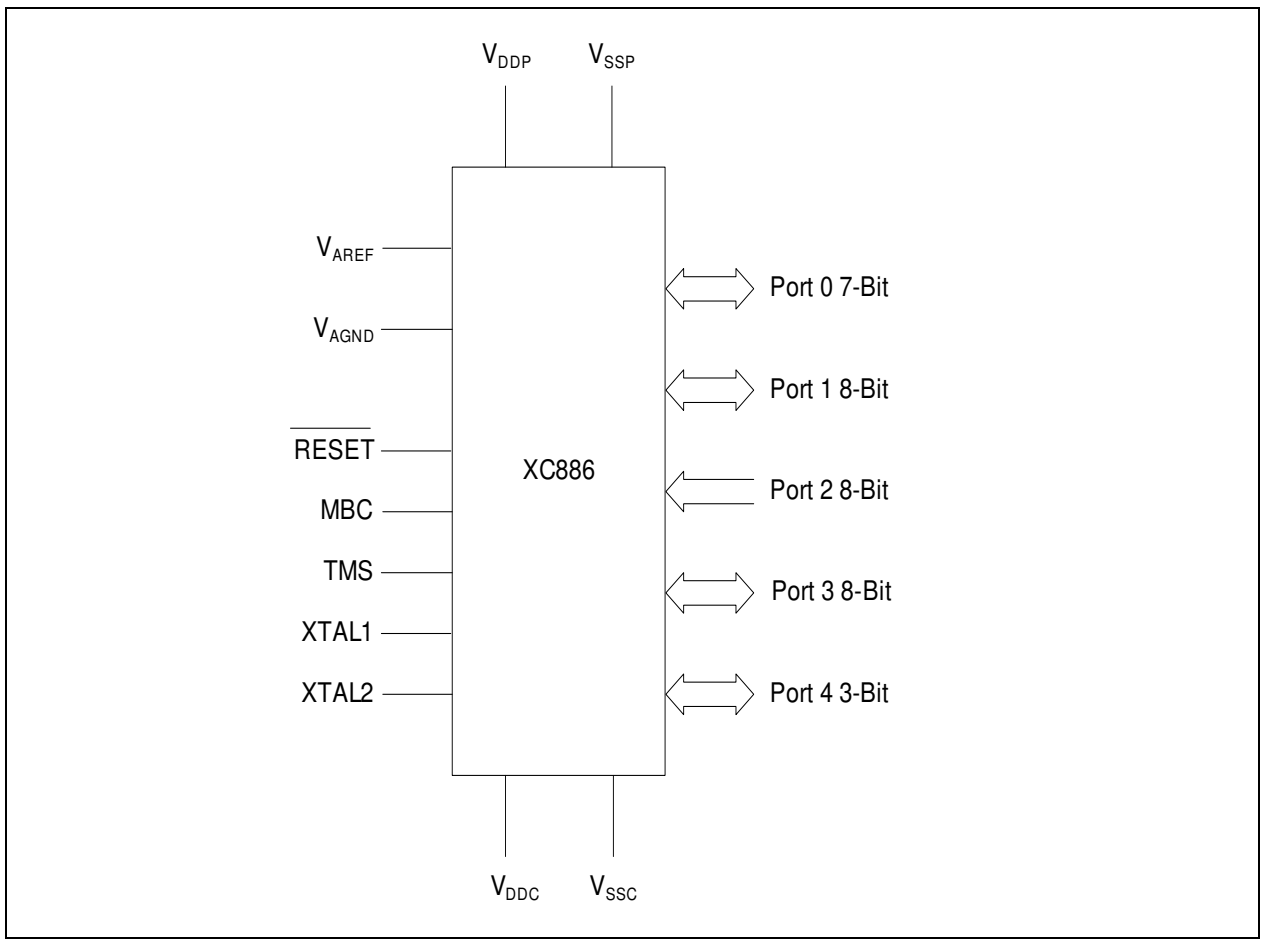

Figure 3 SAL-XC886 Logic Symbol

2.3 Pin Configuration

The pin configuration of the XC886, which is based on the PG-TQFP-48 package, is shown in **Figure 4**.

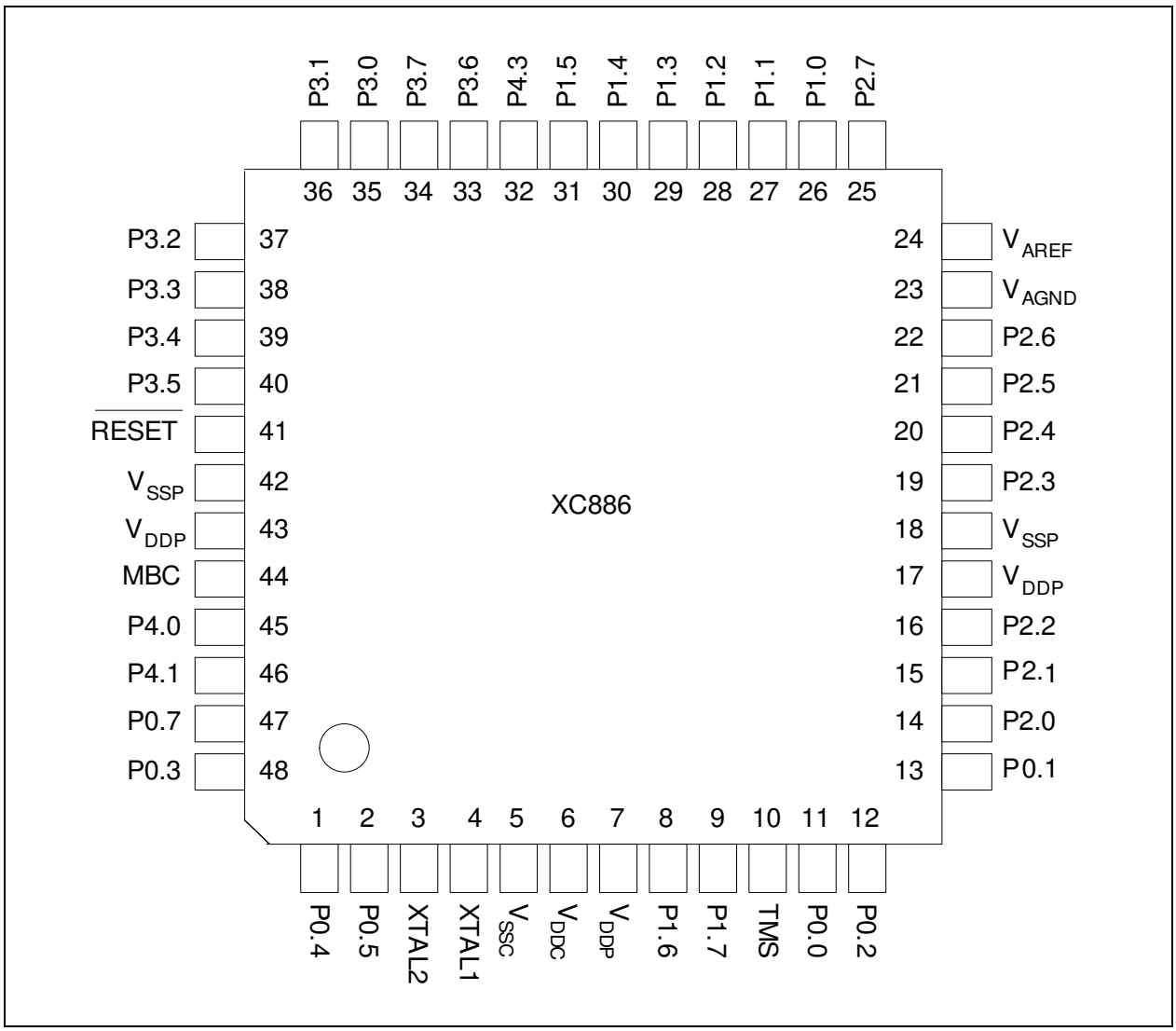

Figure 4 XC886 Pin Configuration, PG-TQFP-48 Package (top view)

2.4 Pin Definitions and Functions

The functions and default states of the SAL-XC886 external pins are provided in **Table 2**.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State	Function
P0		I/O		**Port 0** Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, Timer 2, Timer 21, MultiCAN and SSC.
P0.0	11		Hi-Z	TCK_0 JTAG Clock Input T12HR_1 CCU6 Timer 12 Hardware Run Input CC61_1 Input/Output of Capture/Compare channel 1 CLKOUT_0 Clock Output RXDO_1 UART Transmit Data Output
P0.1	13		Hi-Z	TDI_0 JTAG Serial Data Input T13HR_1 CCU6 Timer 13 Hardware Run Input RXD_1 UART Receive Data Input RXDC1_0 MultiCAN Node 1 Receiver Input COUT61_1 Output of Capture/Compare channel 1 EXF2_1 Timer 2 External Flag Output
P0.2	12		PU	$\overline{\text{CTRAP}}$_2 CCU6 Trap Input TDO_0 JTAG Serial Data Output TXD_1 UART Transmit Data Output/Clock Output TXDC1_0 MultiCAN Node 1 Transmitter Output
P0.3	48		Hi-Z	SCK_1 SSC Clock Input/Output COUT63_1 Output of Capture/Compare channel 3 RXDO1_0 UART1 Transmit Data Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P0.4	1		Hi-Z	MTSR_1	SSC Master Transmit Output/ Slave Receive Input
				CC62_1	Input/Output of Capture/Compare channel 2
				TXD1_0	UART1 Transmit Data Output/Clock Output
P0.5	2		Hi-Z	MRST_1	SSC Master Receive Input/Slave Transmit Output
				EXINT0_0	External Interrupt Input 0
				T2EX1_1	Timer 21 External Trigger Input
				RXD1_0	UART1 Receive Data Input
				COUT62_1	Output of Capture/Compare channel 2
P0.7	47		PU	CLKOUT_1	Clock Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P1		I/O		**Port 1** Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, Timer 2, Timer 21, MultiCAN and SSC.	
P1.0	26		PU	RXD_0 T2EX RXDC0_0	UART Receive Data Input Timer 2 External Trigger Input MultiCAN Node 0 Receiver Input
P1.1	27		PU	EXINT3 T0_1 TDO_1 TXD_0 TXDC0_0	External Interrupt Input 3 Timer 0 Input JTAG Serial Data Output UART Transmit Data Output/Clock Output MultiCAN Node 0 Transmitter Output
P1.2	28		PU	SCK_0	SSC Clock Input/Output
P1.3	29		PU	MTSR_0 TXDC1_3	SSC Master Transmit Output/Slave Receive Input MultiCAN Node 1 Transmitter Output
P1.4	30		PU	MRST_0 EXINT0_1 RXDC1_3	SSC Master Receive Input/ Slave Transmit Output External Interrupt Input 0 MultiCAN Node 1 Receiver Input
P1.5	31		PU	CCPOS0_1 EXINT5 T1_1 EXF2_0 RXDO_0	CCU6 Hall Input 0 External Interrupt Input 5 Timer 1 Input Timer 2 External Flag Output UART Transmit Data Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P1.6	8		PU	CCPOS1_1 CCU6 Hall Input 1 T12HR_0 CCU6 Timer 12 Hardware Run Input EXINT6_0 External Interrupt Input 6 RXDC0_2 MultiCAN Node 0 Receiver Input T21_1 Timer 21 Input
P1.7	9		PU	CCPOS2_1 CCU6 Hall Input 2 T13HR_0 CCU6 Timer 13 Hardware Run Input T2_1 Timer 2 Input TXDC0_2 MultiCAN Node 0 Transmitter Output P1.5 and P1.6 can be used as a software chip select output for the SSC.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P2		I		**Port 2** Port 2 is an 8-bit general purpose input-only port. It can be used as alternate functions for the digital inputs of the JTAG and CCU6. It is also used as the analog inputs for the ADC.
P2.0	14		Hi-Z	CCPOS0_0 CCU6 Hall Input 0 EXINT1_0 External Interrupt Input 1 T12HR_2 CCU6 Timer 12 Hardware Run Input TCK_1 JTAG Clock Input CC61_3 Input of Capture/Compare channel 1 AN0 Analog Input 0
P2.1	15		Hi-Z	CCPOS1_0 CCU6 Hall Input 1 EXINT2_0 External Interrupt Input 2 T13HR_2 CCU6 Timer 13 Hardware Run Input TDI_1 JTAG Serial Data Input CC62_3 Input of Capture/Compare channel 2 AN1 Analog Input 1
P2.2	16		Hi-Z	CCPOS2_0 CCU6 Hall Input 2 CTRAP_1 CCU6 Trap Input CC60_3 Input of Capture/Compare channel 0 AN2 Analog Input 2
P2.3	19		Hi-Z	AN3 Analog Input 3
P2.4	20		Hi-Z	AN4 Analog Input 4
P2.5	21		Hi-Z	AN5 Analog Input 5
P2.6	22		Hi-Z	AN6 Analog Input 6
P2.7	25		Hi-Z	AN7 Analog Input 7

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P3		I/O		**Port 3** Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, Timer 21 and MultiCAN.
P3.0	35		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0 RXDO1_1 UART1 Transmit Data Output
P3.1	36		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0 TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	37		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input CC61_0 Input/Output of Capture/Compare channel 1
P3.3	38		Hi-Z	COUT61_0 Output of Capture/Compare channel 1 TXDC1_1 MultiCAN Node 1 Transmitter Output
P3.4	39		Hi-Z	CC62_0 Input/Output of Capture/Compare channel 2 RXDC0_1 MultiCAN Node 0 Receiver Input T2EX1_0 Timer 21 External Trigger Input
P3.5	40		Hi-Z	COUT62_0 Output of Capture/Compare channel 2 EXF21_0 Timer 21 External Flag Output TXDC0_1 MultiCAN Node 0 Transmitter Output
P3.6	33		PD	$\overline{\text{CTRAP\_0}}$ CCU6 Trap Input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P3.7	34		Hi-Z	EXINT4 COUT63_0	External Interrupt Input 4 Output of Capture/Compare channel 3

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function	
P4		I/O		**Port 4** Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, Timer 21 and MultiCAN.	
P4.0	45		Hi-Z	RXDC0_3 CC60_1	MultiCAN Node 0 Receiver Input Output of Capture/Compare channel 0
P4.1	46		Hi-Z	TXDC0_3 COUT60_1	MultiCAN Node 0 Transmitter Output Output of Capture/Compare channel 0
P4.3	32		Hi-Z	EXF21_1 COUT63_2	Timer 21 External Flag Output Output of Capture/Compare channel 3

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
V_{DDP}	7, 17, 43	–	–	**I/O Port Supply (5.0 V)** Also used by EVR and analog modules. All pins must be connected.
V_{SSP}	18, 42	–	–	**I/O Port Ground** All pins must be connected.
V_{DDC}	6	–	–	**Core Supply Monitor (2.5 V)**
V_{SSC}	5	–	–	**Core Supply Ground**
V_{AREF}	24	–	–	**ADC Reference Voltage**
V_{AGND}	23	–	–	**ADC Reference Ground**
XTAL1	4	I	Hi-Z	**External Oscillator Input (backup for on-chip OSC, normally NC)**
XTAL2	3	O	Hi-Z	**External Oscillator Output (backup for on-chip OSC, normally NC)**
TMS	10	I	PD	**Test Mode Select**
RESET	41	I	PU	**Reset Input**
MBC[1)]	44	I	PU	**Monitor & BootStrap Loader Control**

1) An external pull-up device in the range of 4.7 kΩ to 100 kΩ. is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.

3 Functional Description

Chapter 3 provides an overview of the SAL-XC886 functional description.

3.1 Processor Architecture

The SAL-XC886 is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the SAL-XC886 CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. Access to the Flash memory, however, requires an additional wait state (one machine cycle). The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The SAL-XC886 CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and Special Function Registers (SFRs).

Figure 5 shows the CPU functional blocks.

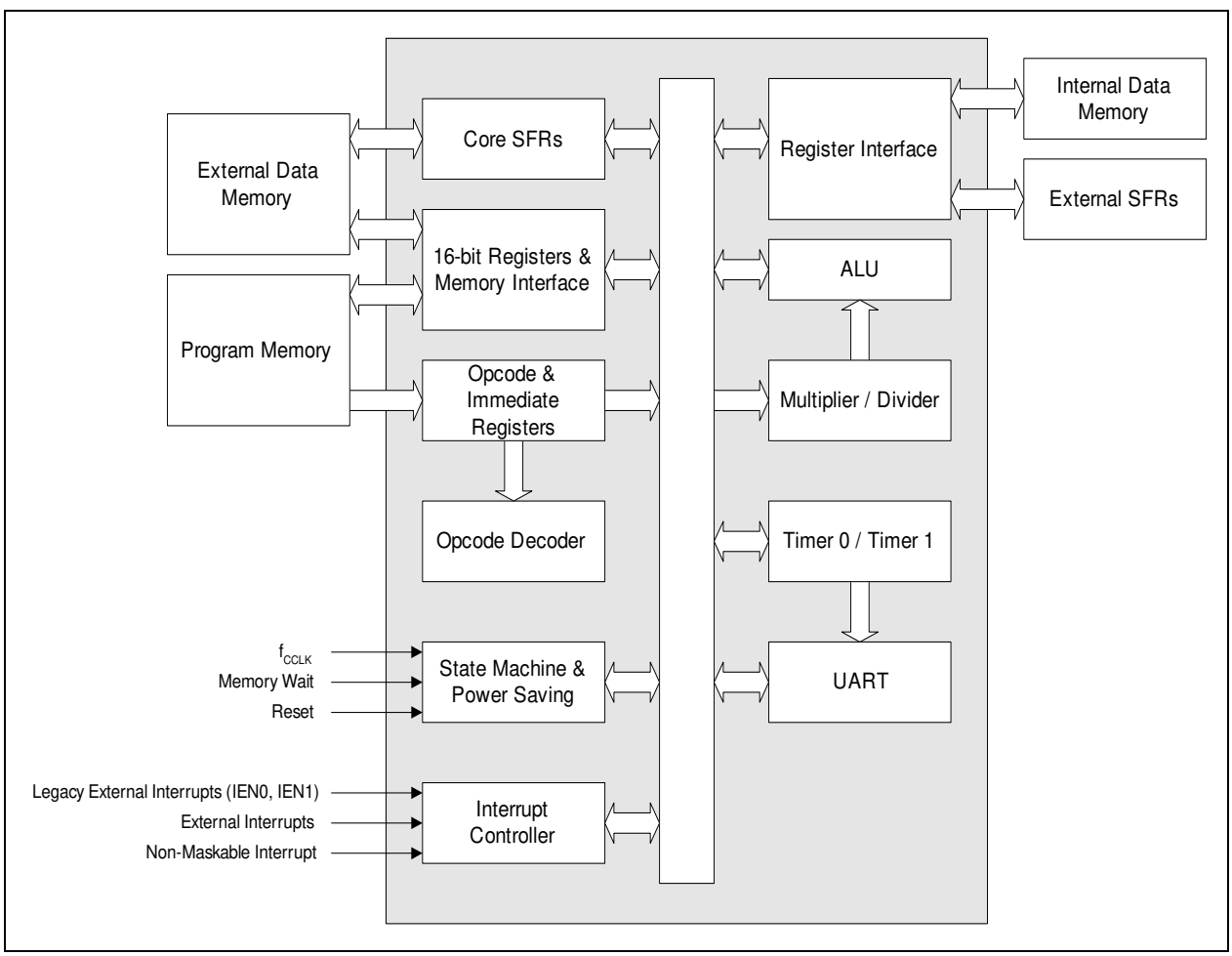

Figure 5 CPU Block Diagram

3.2 Memory Organization

The SAL-XC886 CPU operates in the following five address spaces:

- 12 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 1.5 Kbytes of XRAM memory
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 24/32 Kbytes of Flash program memory

Figure 6 illustrates the memory address spaces of the 32-Kbyte Flash devices. For the 24-Kbyte Flash devices, the shaded banks are not available.

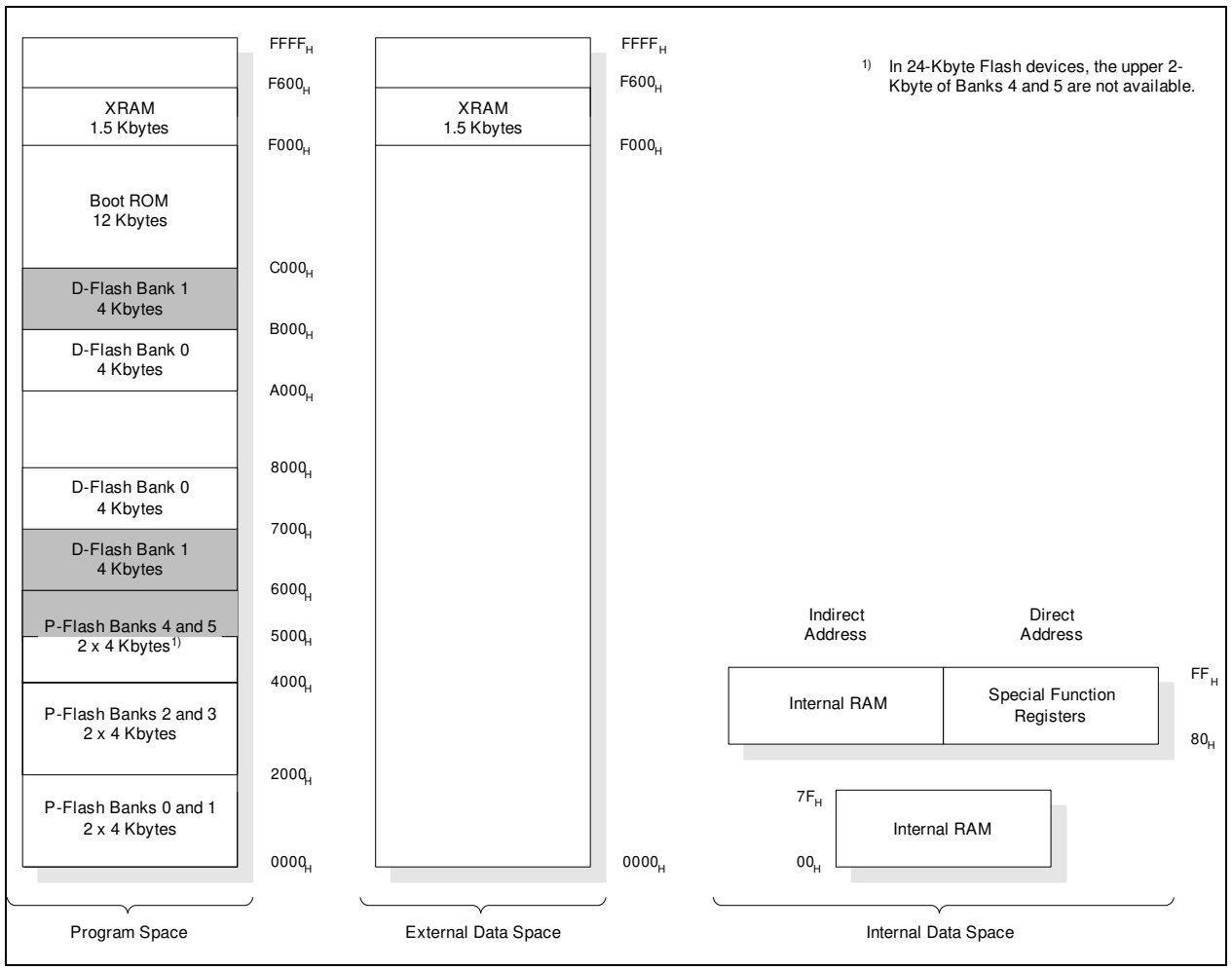

Figure 6 Memory Map of SAL-XC886 Flash Device

3.2.1 Memory Protection Strategy

The SAL-XC886 memory protection strategy includes:

- Read-out protection: The user is able to protect the contents in the Flash memory from being read
  – Flash protection is enabled by programming a valid password (8-bit non-zero value) via BSL mode 6.
- Flash program and erase protection.

3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in Table 3.

Table 3 Flash Protection Modes

Flash Protection	Without hardware protection	With hardware protection	
Hardware Protection Mode	-	0	1
Activation	Program a valid password via BSL mode 6		
Selection	Bit 4 of password = 0	Bit 4 of password = 1 MSB of password = 0	Bit 4 of password = 1 MSB of password = 1
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
External access to P-Flash	Not possible	Not possible	Not possible
P-Flash program and erase	Possible	Not possible	Not possible
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash