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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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SC1112
Triple Low Dropout Regulator Controllers

POWER MANAGEMENT

Description

The SC1112 was designed for the latest high speed motherboards. It includes three low dropout regulator controllers. The controllers provide the power for the system AGTL bus Termination Voltage, Chipset, and clock circuitry.

An adjustable controller with a 1.2V reference is available, while two selectable outputs are provided for the VTT (1.25 V or 1.5V, SC1112) or (1.2V or 1.5V, SC1112A) and the AGP (1.5V or 3.3V). The SC1112 low dropout regulators are designed to track the 3.3V power supply as the VTTIN supply is cycled On and Off. A latched short circuit protection is also available for the VTT output.

Other features include an integrated charge pump that provides adequate gate drives for the external MOSFETs, and a capacitive programable delay for the power good signal.

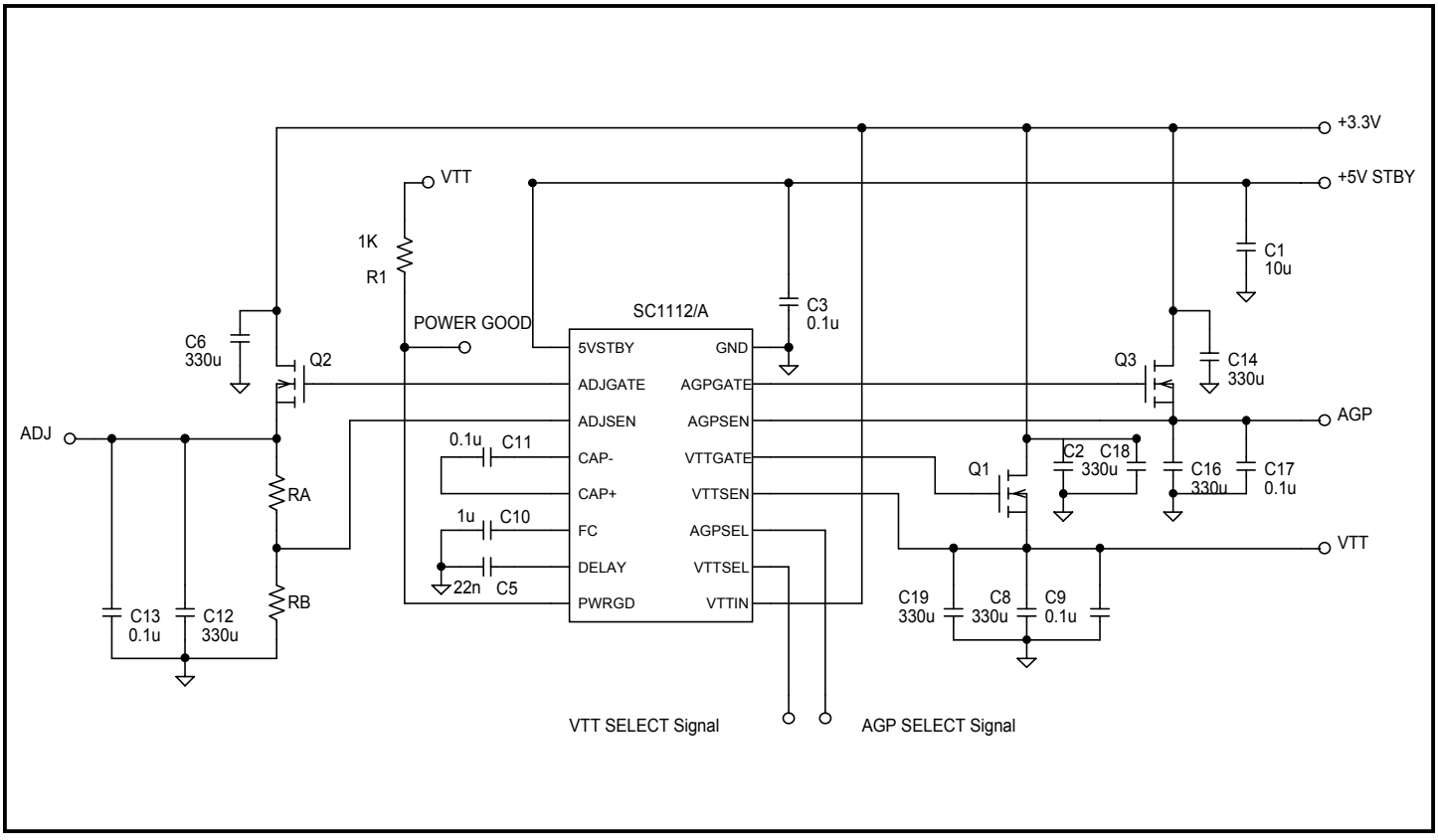
Features

- Triple linear controllers
- Selectable and adjustable output voltages
- LDOs track input voltage within 200mV (Function of the MOSFETs used) until regulation
- Integrated charge pump
- Programmable power good delay signal
- Latched over current protection (VTT)
- Pb-free package available, fully WEEE and RoHS compliant

Applications

- Pentium® III Motherboards
- Triple power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
5VSTBY to GND		-0.3 to +7	V
VTTSEN to GND		-0.3 to 5	V
AGPSEN to GND		-0.3 to 5	V
ADJSEN to GND		-0.3 to 5	V
Operating Temperature Range	T_A	0 to +70	°C
Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_L	300	°C
Thermal Resistance Junction to Ambient SOIC TSSOP	θ_{JA}	 130 115	°C/W
Thermal Impedance Junction to Case SOIC TSSOP	θ_{JC}	 30 38	°C/W
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: 5VSTBY=4.75V to 5.25V; VTTIN=3.3V; T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply (5VSTBY)						
Supply Voltage	5VSTBY		4.75	5	5.25	V
Supply Current	I_{5VSTBY}	5VSTBY= 5V	6	8	12	mA
VTT Short Circuit Protection						
VTT Short Circuit Delay Timer Threshold(4)	SC_{Th}			1.5		V
VTT Short Circuit Delay Time(4)	SC_{td}			$(Cdelay*SC_{TH})/I_{SC}$		S
VTT Short Circuit Delay Source Current(4)	I_{SC}		16	22	28	µA
VTT Short Circuit Threshold(4)	$VTTSC_{Th}$		650	700	750	mV
VTT Power Good						
PWRGD Delay Timer Threshold(5)	PG_{Delay_TH}		1.450	1.500	1.550	V
PWRGD Threashold(5)	$PG_{TH\_1.2}$		1.060	1.085	1.110	V
PWRGD Threashold(5)	$PG_{TH\_1.5}$		1.330	1.350	1.390	V
PWRGD Delay Time(5)	$PG_{td\_1.2}$			$(Cdelay*PG_{TH\_1.2})/I_{PG}$		S
PWRGD Delay Time(5)	$PG_{td\_1.5}$			$(Cdelay*PG_{TH\_1.5})/I_{PG}$		S
PWRGD Source Current(5)	I_{PG}		16	22	28	µA
Linear Sections						
VTT Input Supply Threshold	$VTTIN_{TH}$		1.45	1.52	1.55	V
Tracking Difference (1)(3)	$Delta_{TRACK}$	V_{IN} = 3.30V, I_O = 0A		200		mV

Electrical Characteristics (Cont.)

Unless specified: 5VSTBY=4.75V to 5.25V; VTTIN=3.3V; T_A = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linear Sections (Cont.)						
Output Voltage VTT	(SC1112A) $VTT_{1.2}$	I_O = 0 to 2A, VTTSEL = LOW	1.176	1.200	1.224	V
	(SC1112) $VTT_{1.25}$	I_O = 0 to 2A, VTTSEL = LOW	1.225	1.250	1.275	
	$VTT_{1.5}$	I_O = 0 to 2A, VTTSEL = HIGH	1.470	1.500	1.530	V
Output Voltage AGP	$AGP_{1.5}$	I_O = 0 to 2A, AGPSEL = LOW	1.470	1.500	1.530	V
	$AGP_{3.3}$	I_O = 0 to 2A, AGPSEL = HIGH	3.234	3.300		V
Output Voltage ADJ	ADJ	I_O = 0 to 2A	-2%	1.2*(1+RA/RB)	+2%	V
VTTSEN Bias Current (SC1112)	$Ibias_{VTTSEN}$		90	120	140	µA
VTTSEN Bias Current (SC1112A)	$Ibias_{VTTSEN}$			1	5	µA
AGPSEN Bias Current	$Ibias_{AGPSEN}$		110	150	170	µA
ADJSEN Bias Current	$Ibias_{ADJSEN}$			1	5	µA
VTT Gate Current	$Isource_{VTTgate}$	5VSTBY = 4.75V, Vgate = 3.0V		500		µA
	$Isink_{VTTgate}$			500		µA
AGP Gate Current	$Isource_{AGPgate}$	5VSTBY = 4.75V, Vgate = 3.0V		500		µA
	$Isink_{AGPgate}$			500		µA
ADJ Gate Current	$Isource_{ADJgate}$	5VSTBY = 4.75V, Vgate = 3.0V		500		µA
	$Isink_{ADJgate}$			500		µA
Load Regulation	$LOAD_{REG}$	VTTIN = 3.30V, I_O = 0 to 2A		0.3		%
Line Regulation	$LINE_{REG}$	VTTIN = 3.13V to 3.47V, Io = 2A		0.3		%
Gain (AOL)(2)	$GAIN_{LDO}$	LDOS Output to GATE		50		dB

Notes:

(1) All electrical characteristics are for the application circuit on page 19.

(2) Guaranteed by design

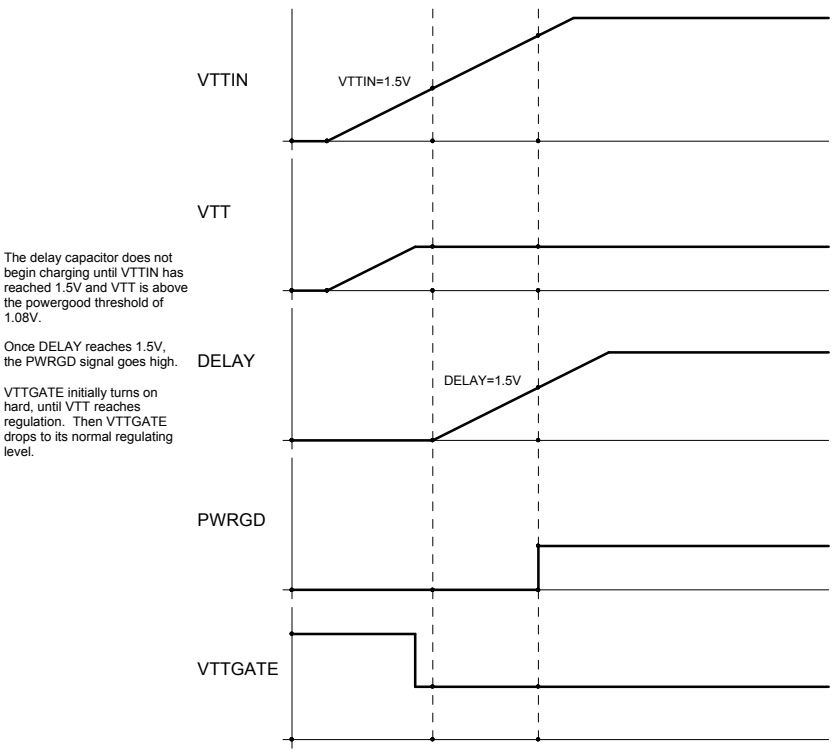
(3) Tracking Difference is defined as the delta between 3.3V Vin and the VTT, AGP, ADJ output voltages during the linear ramp up until regulation is achieved. The Tracking Voltage difference might vary depending on MOSFETs Rdson, and Load Conditions.

(4) During power up, an internal short circuit glitch timer will start once the VTT Input Voltage exceeds the $VTTIN_{TH}$ (1.5V). During the glitch timer immunity time, determined by the Delay capacitor (Delay time is approximately equal to (Cdelay*SCTH)/ISC), the short circuit protection is disabled to allow VTT output to rise above the trip threshold (0.7V). If the VTT output has not risen above the trip threshold after the immunity time has elapsed, the VTT output is latched off and will only be enabled again if either the VTT input voltage or the 5VSTBY is cycled.

(5) PWRGD pin is kept low during the power up, until the VTT output has reached its $PG_{td1.2}$ or $PG_{td1.5}$ level. At that time the PWRGD source current I_{PG} (20uA) is enabled and will start charging the external PWRGD delay capacitor connected to the DELAY pin. Once the capacitor is charged above the PG_{Delay_TH} (1.5V), the PWRGD pin is released from ground.

Timing Diagrams

NORMAL STARTUP CONDITION

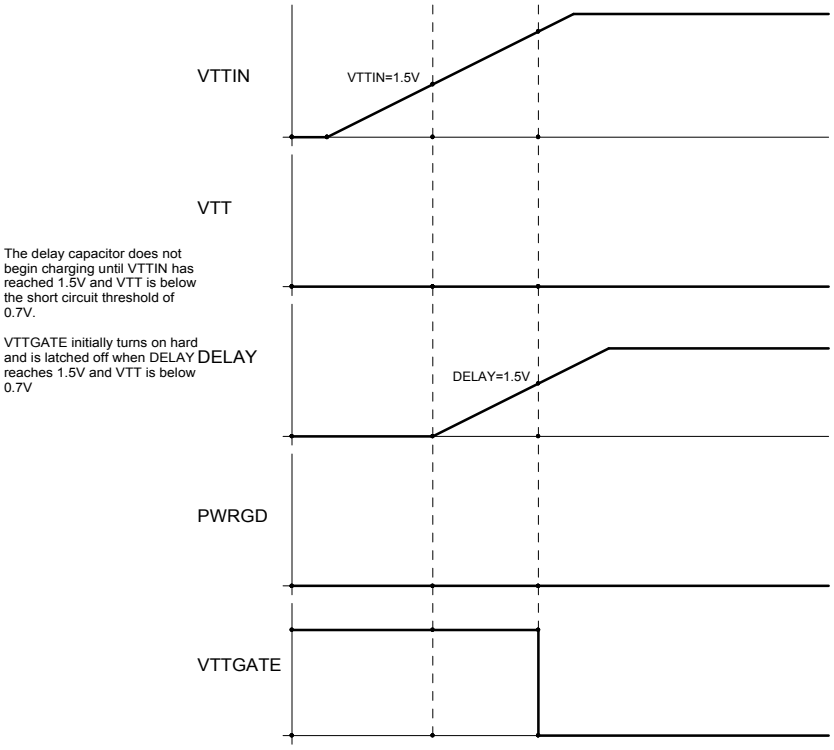


The delay capacitor does not begin charging until VTTIN has reached 1.5V and VTT is above the powergood threshold of 1.08V.

Once DELAY reaches 1.5V, the PWRGD signal goes high.

VTTGATE initially turns on hard, until VTT reaches regulation. Then VTTGATE drops to its normal regulating level.

SHORT-CIRCUIT STARTUP

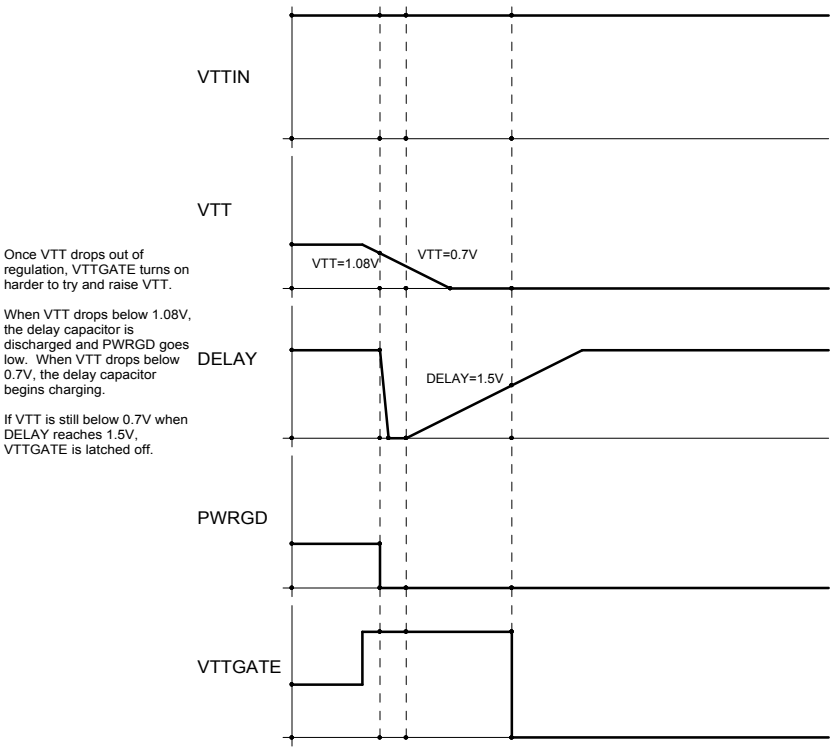


The delay capacitor does not begin charging until VTTIN has reached 1.5V and VTT is below the short circuit threshold of 0.7V.

VTTGATE initially turns on hard and is latched off when DELAY reaches 1.5V and VTT is below 0.7V

Timing Diagrams (Cont.)

SHORT-CIRCUIT DURING NORMAL OPERATION

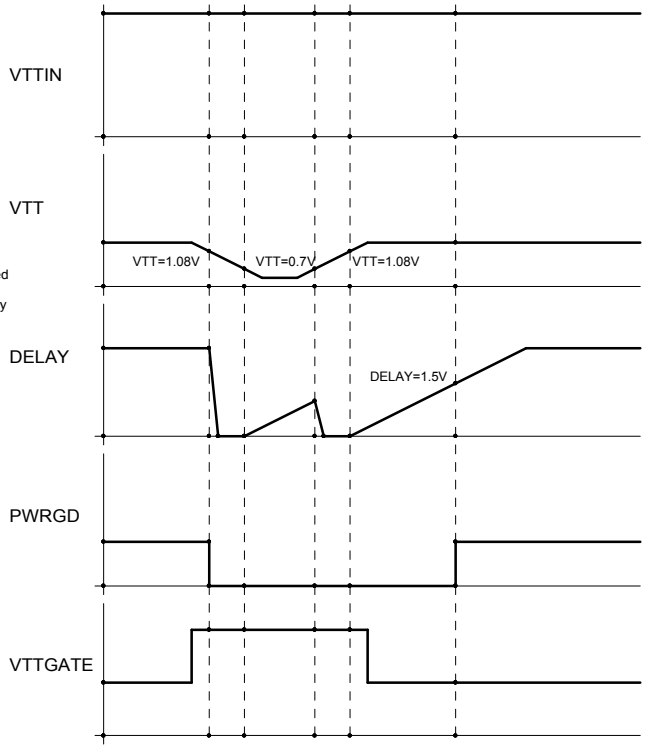


Once VTT drops out of regulation, VTTGATE turns on harder to try and raise VTT.

When VTT drops below 1.08V, the delay capacitor is discharged and PWRGD goes low. When VTT drops below 0.7V, the delay capacitor begins charging.

If VTT is still below 0.7V when DELAY reaches 1.5V, VTTGATE is latched off.

SHORT-CIRCUIT AND RECOVERY DURING NORMAL OPERATION



Once VTT drops out of regulation, VTTGATE turns on harder to try and raise VTT.

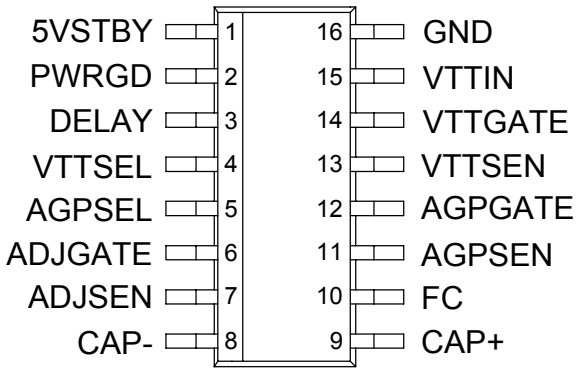
When VTT drops below 1.08V, the delay capacitor is discharged and PWRGD goes low. When VTT drops below 0.7V, the delay capacitor begins charging.

If VTT recovers above 0.7V before DELAY reaches 1.5V, DELAY is again discharged.

If VTT reaches 1.08V the delay capacitor begins charging and normal operation continues.

Pin Configuration

Top View



(16-Pin SOIC or TSSOP)

Ordering Information

Part Number (1)(2)	Package	Temp Range (T_J)
SC1112STR	SO-16	0° to 125°C
SC1112STRT(3)		
SC1112ASTR		
SC1112TSTR	TSSOP-16	0° to 125°C
SC1112TSTRT(3)		
SC1112ATSTR		
SC1112EVB	Evaluation Board	

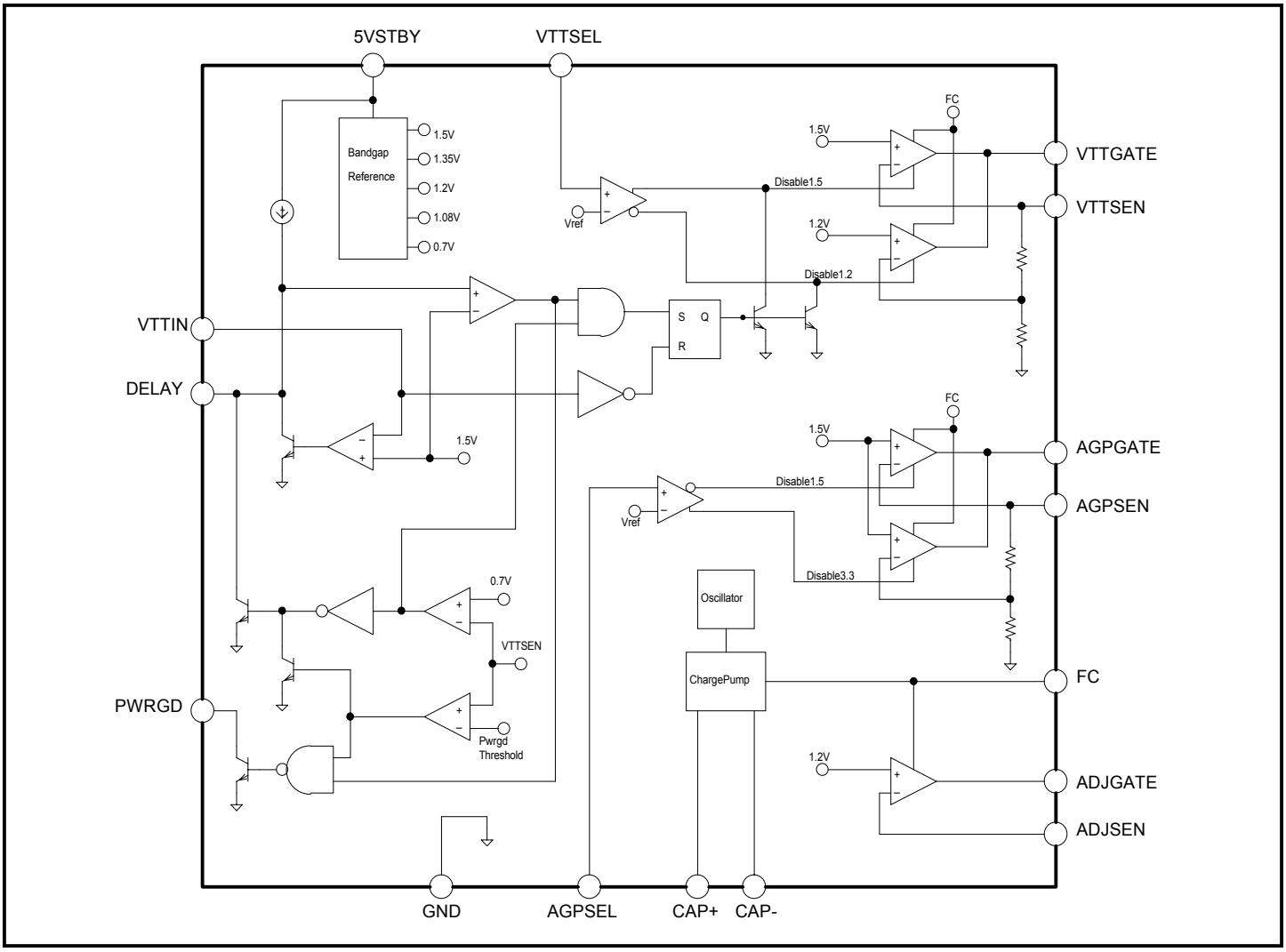
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Part Number (SO-16): SC1112STR and SC1112STRT = 1.25V and SC1112ASTR = 1.2V.
Part Number (TSSOP-16): SC1112TSTR = 1.25V and SC1112ATSTR = 1.2V.
(3) Pb-free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	5VSTBY	5V Standby input, supplies power for Ref, Charge Pump, Oscillator and FET controllers.
2	PWRGD	Open collector Power Good Flag for VTT output.
3	DELAY	A capacitor from this pin to GND will program the delay for the Power Good Flag of VTT output and the glitch immunity time.
4	VTTSEL	TTL signal that programs the VTT output voltage: VTTSEL = LOW, VTT = 1.2XV VTTSEL = HIGH, VTT = 1.5V
5	AGPSEL	TTL signal that programs the AGP output voltage: AGPSEL = LOW, AGP = 1.5V AGPSEL = HIGH, AGP = 3.3V
6	ADJGATE	Gate drive output for AGP.
7	ADJSEN	Sense input for ADJ.
8	CAP-	Negative connection to boost capacitor.
9	CAP+	Positive connection to boost capacitor.
10	FC	Filter capacitor for the internal charge pump should be connected from this pin to GND.
11	AGPSEN	Sense input for AGP.
12	AGPGATE	Gate drive output for AGP.
13	VTTSEN	Sense input for VTT.
14	VTTGATE	Gate drive output for VTT.
15	VTTIN	Short circuit sense line connected to the 3.3Vin.
16	GND	Ground.

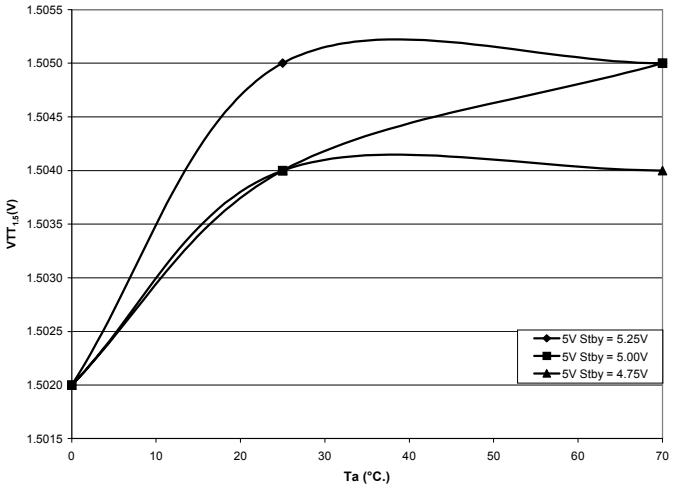
NOTE: (1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram

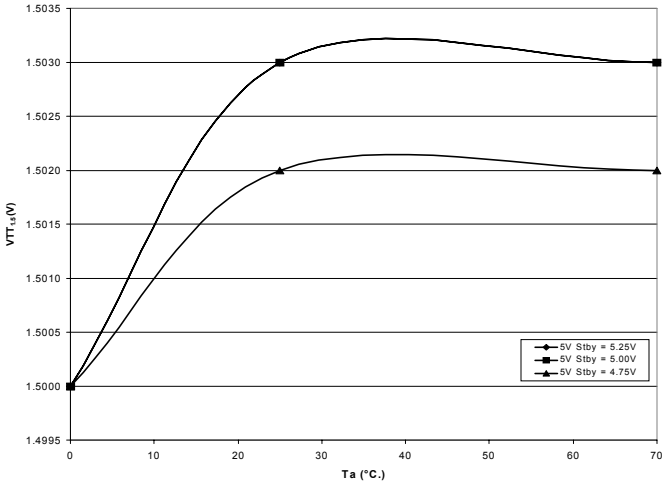


Typical Characteristics

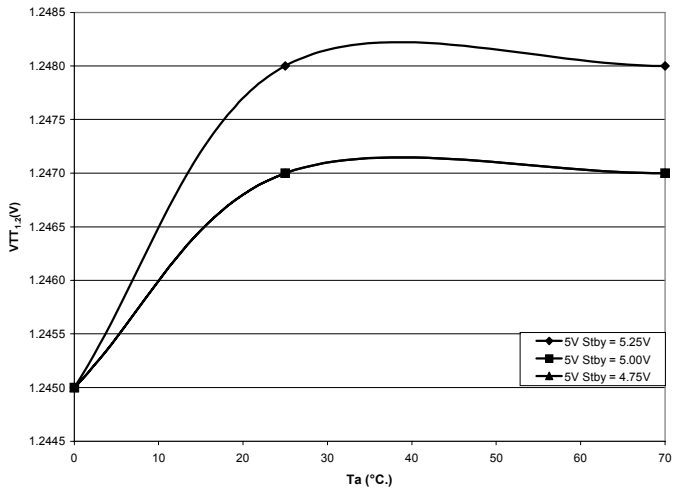
VTT(1.5V) Output Voltage @ Io = 0A vs Ta



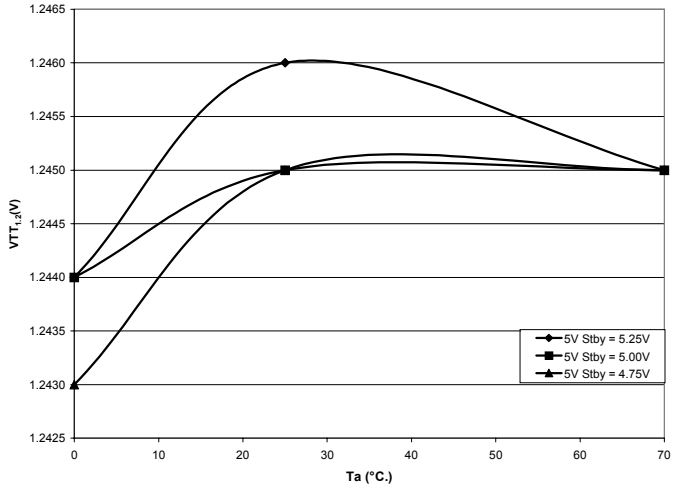
VTT(1.5V) Output Voltage @ Io = 2A vs Ta



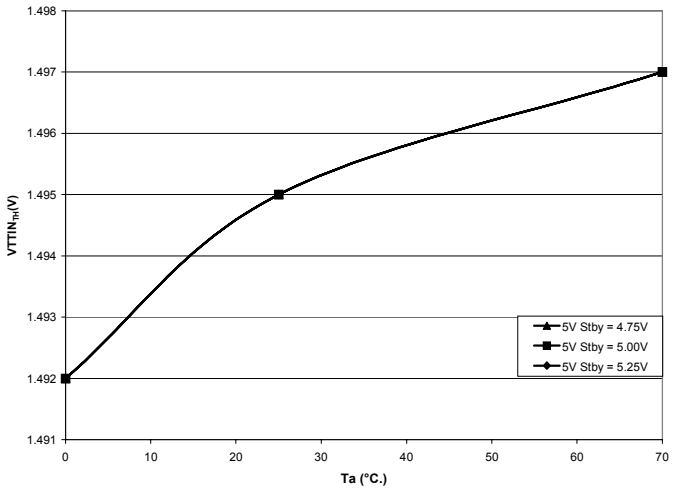
VTT(1.25V) Output Voltage @ Io = 0A vs Ta



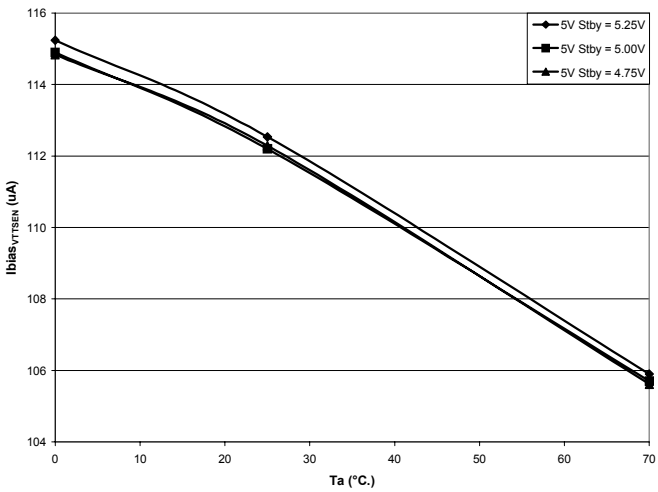
VTT(1.5V) Output Voltage @ Io = 2A vs Ta



VTT Input Supply Threshold vs Ta

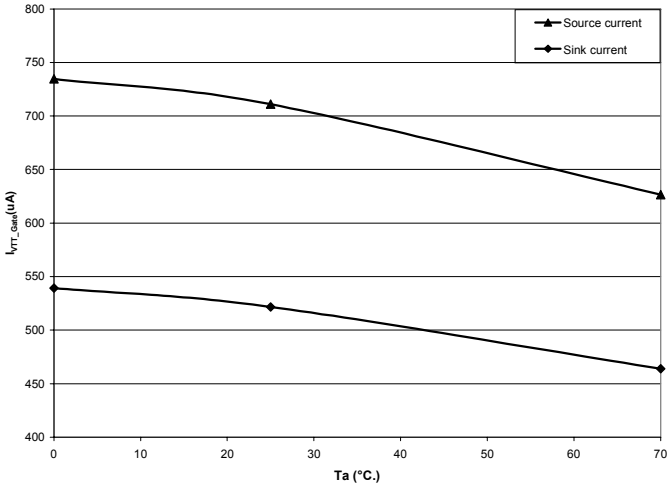


VTT Sense Bias current vs Ta

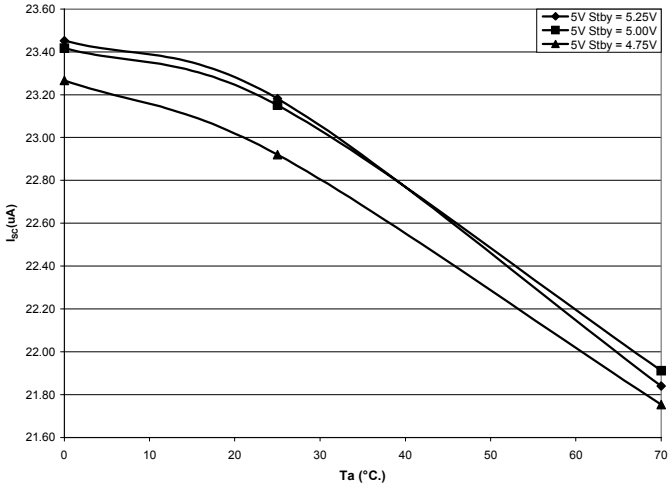


Typical Characteristics (Cont.)

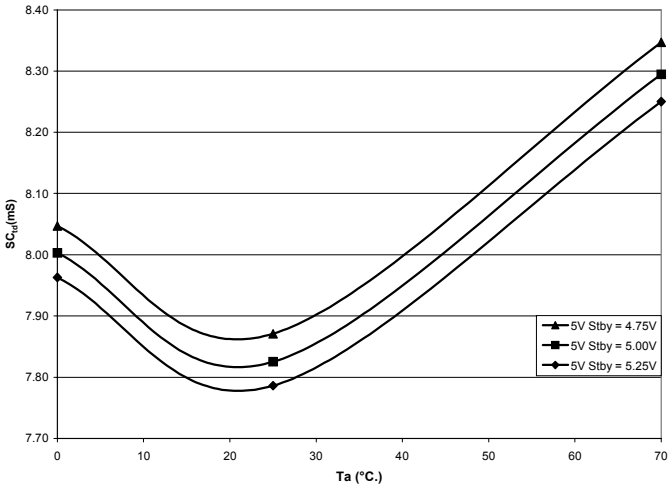
VTT Gate Current @ Vgate = 3V, 5V Stby = 4.75V vs Ta



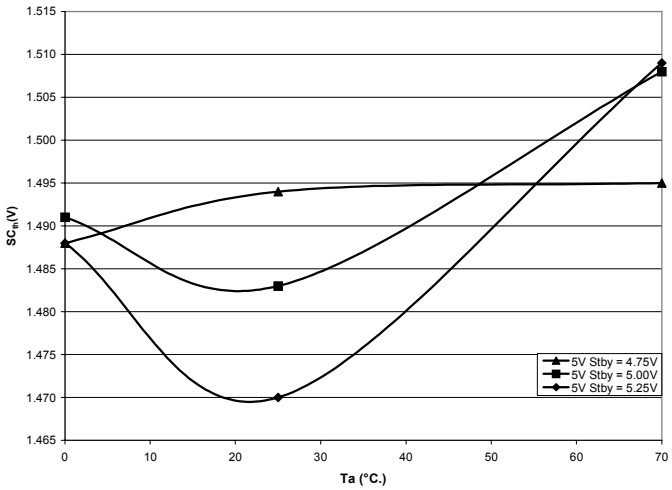
VTT Short circuit Delay source current vs Ta



VTT Short circuit Delay Time (Cdelay = 0.1uF) vs Ta

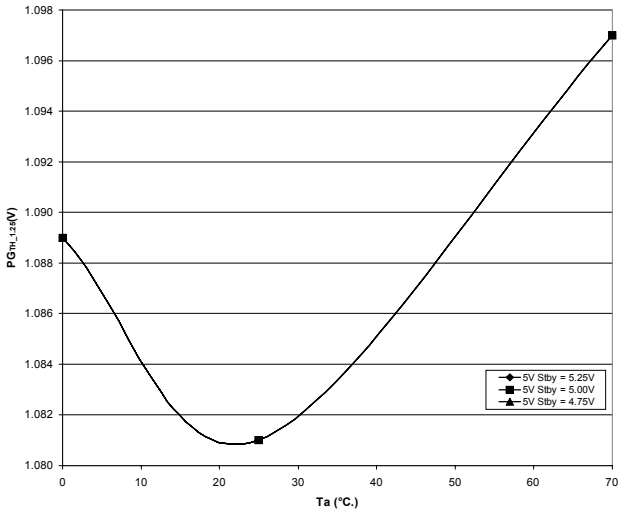


VTT Short circuit Delay Timer Threshold vs Ta

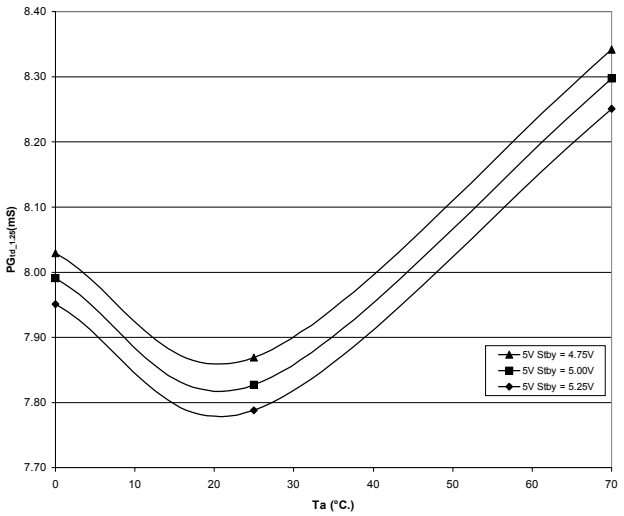


Typical Characteristics (Cont.)

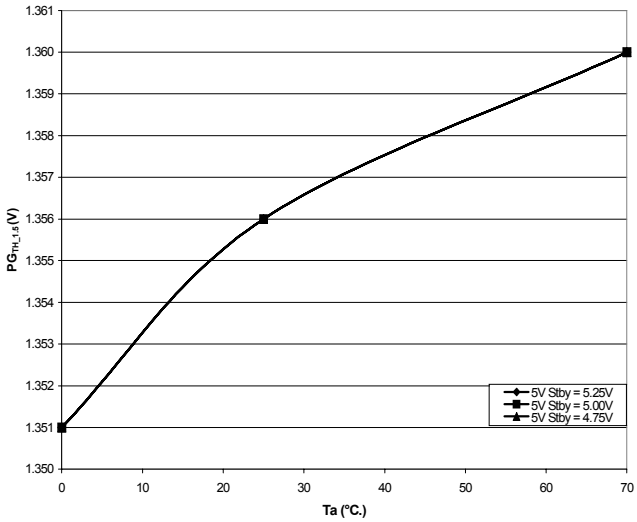
VTT (1.25V) Power Good Threshold vs Ta



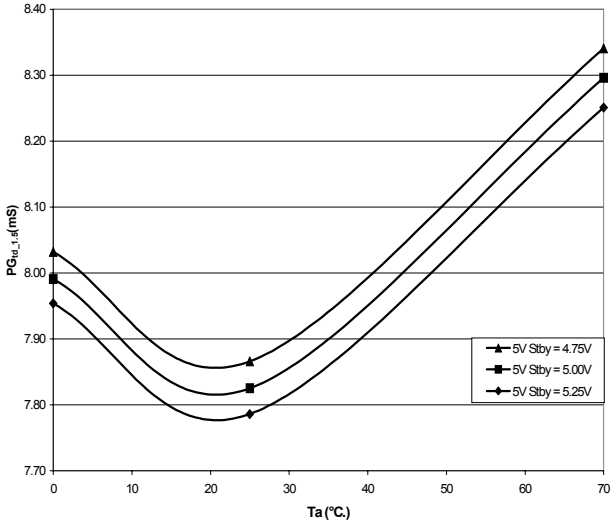
VTT (1.25V) Power Good Delay Time vs Ta



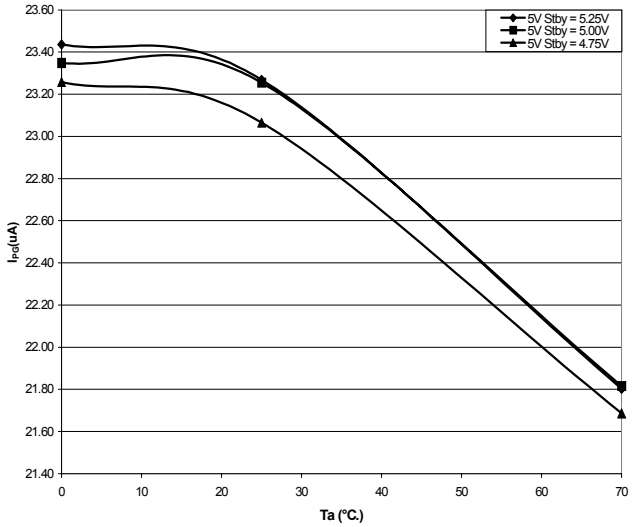
VTT (1.5V) Power Good Threshold vs Ta



VTT (1.5V) Power Good Delay Time vs Ta

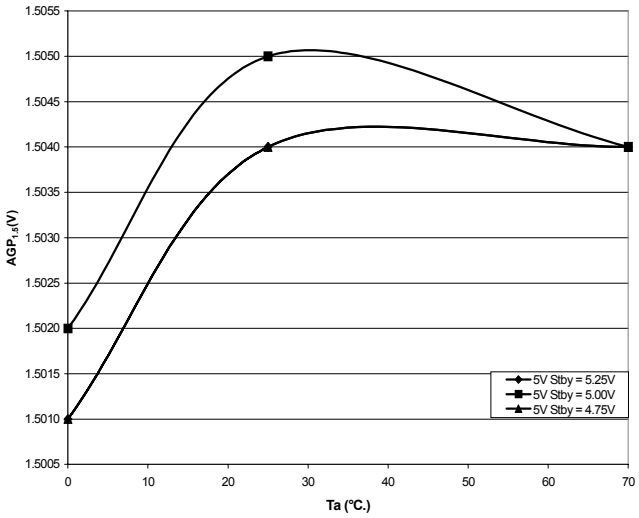


VTT Power Good Source current vs Ta

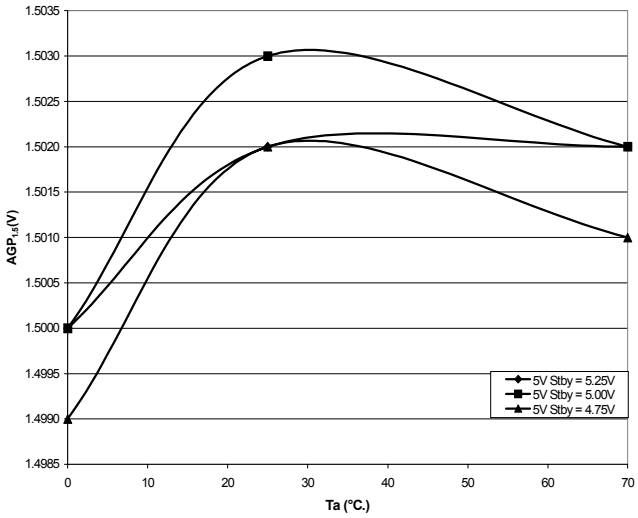


Typical Characteristics (Cont.)

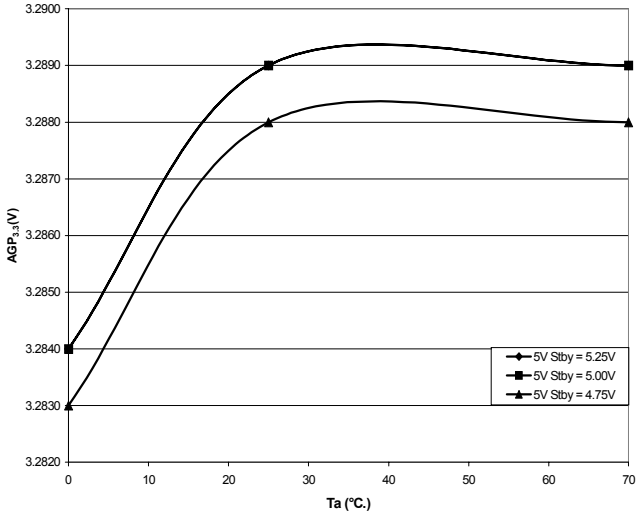
AGP (1.5V) Output Voltage @ Io = 0A vs Ta



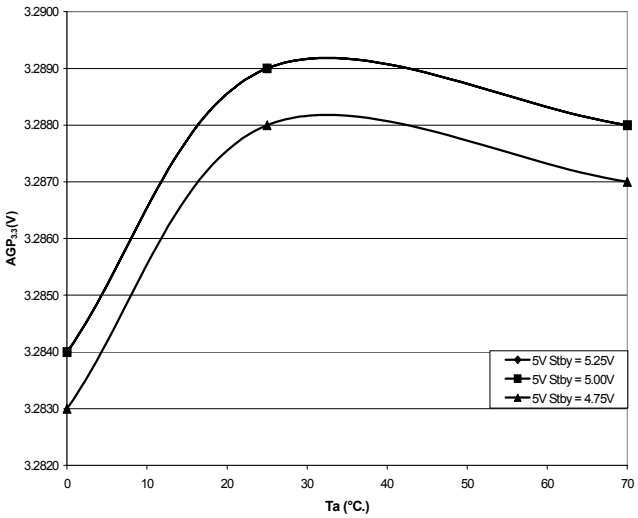
AGP (1.5V) Output Voltage @ Io = 2A vs Ta



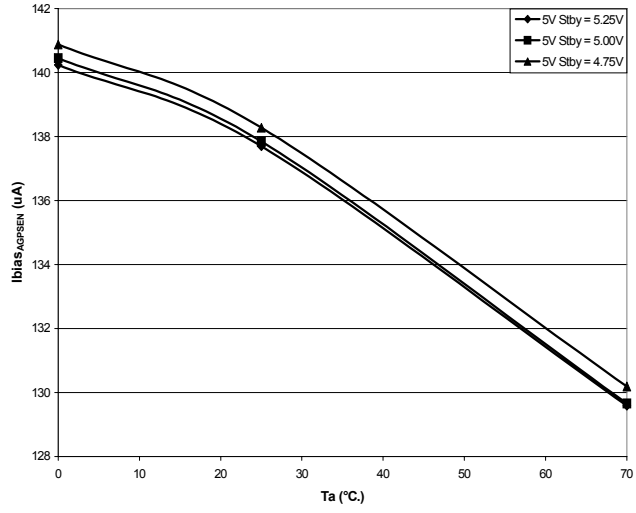
AGP (3.3V) Output Voltage @ Io = 0A vs Ta



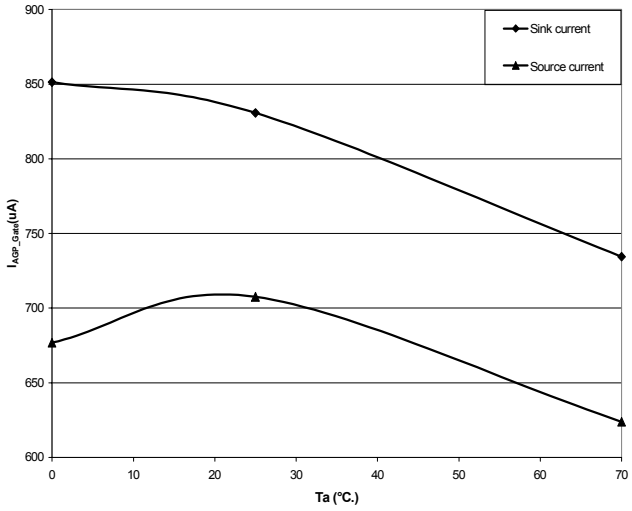
AGP (3.3V) Output Voltage @ Io = 2A vs Ta



AGP Sense Bias current vs Ta

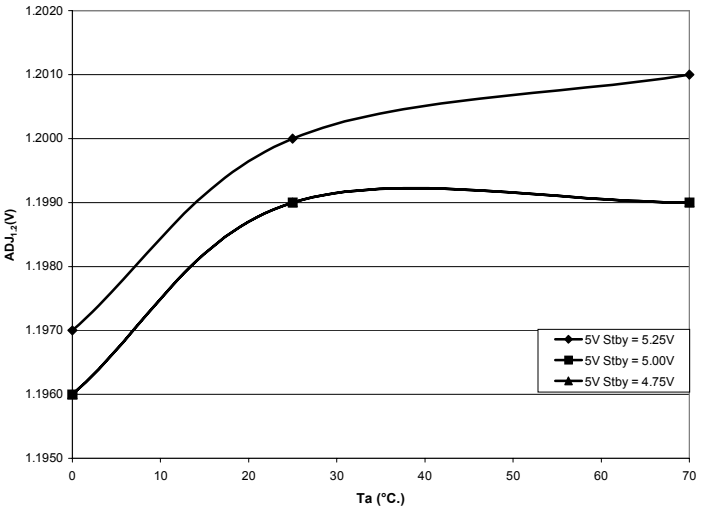


AGP Gate Current @ Vgate = 3V, 5V Stby = 4.75 vs Ta

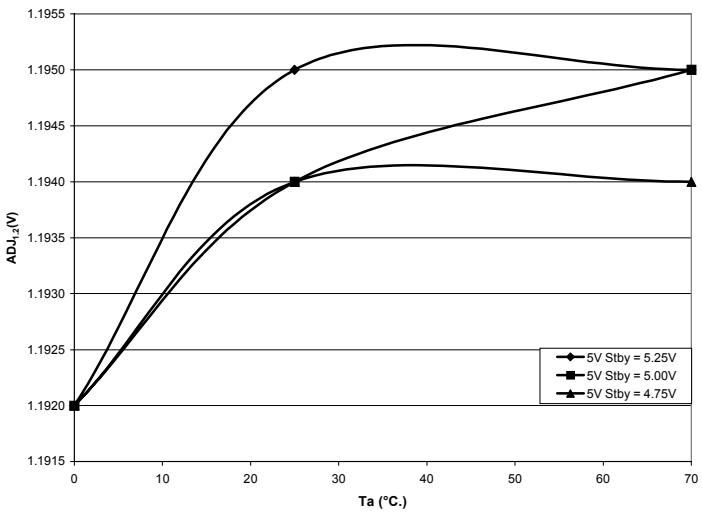


Typical Characteristics (Cont.)

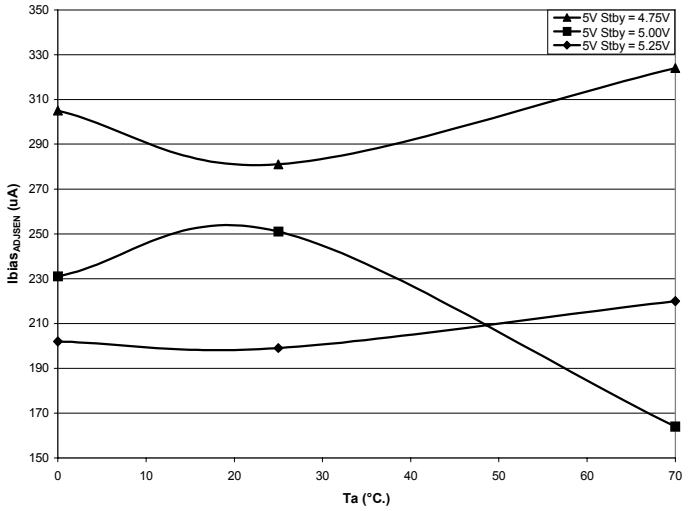
ADJ (1.2V) Output Voltage @ Io = 0A vs Ta



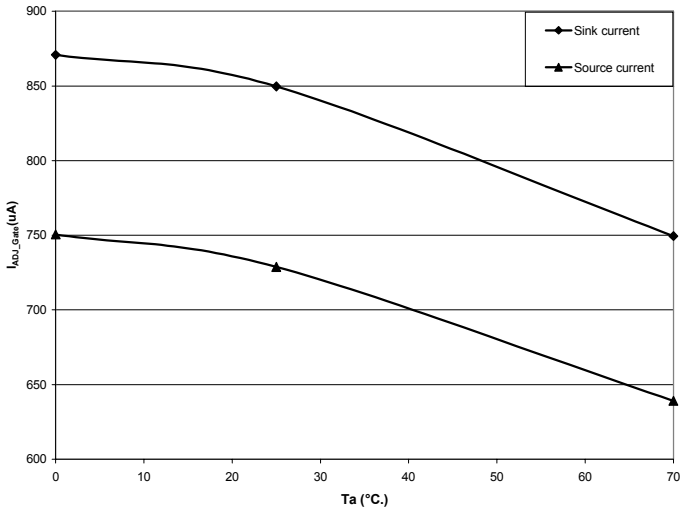
ADJ (1.2V) Output Voltage @ Io = 2A vs Ta



ADJ Sense Bias current vs Ta

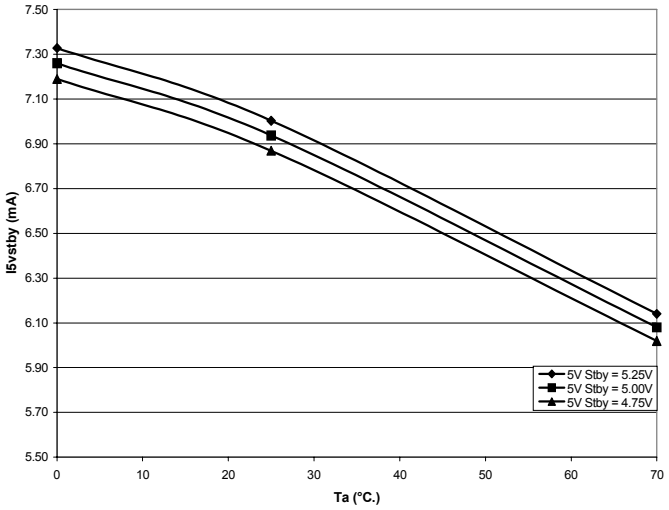


ADJ Gate Current @ Vgate = 3V, 5V Stby = 4.75V vs Ta

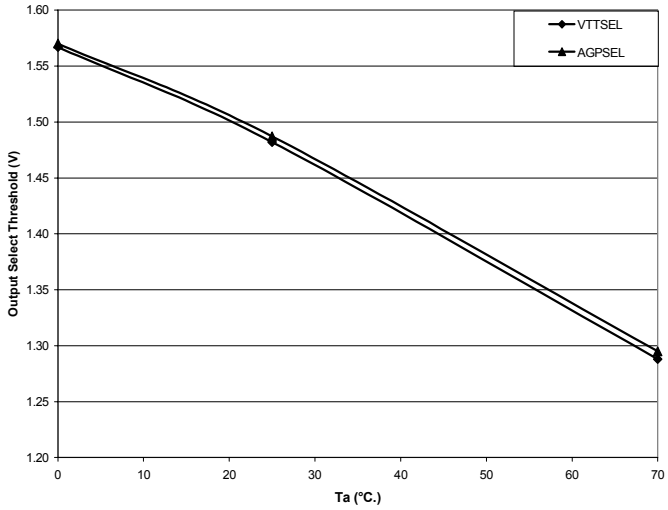


Typical Characteristics (Cont.)

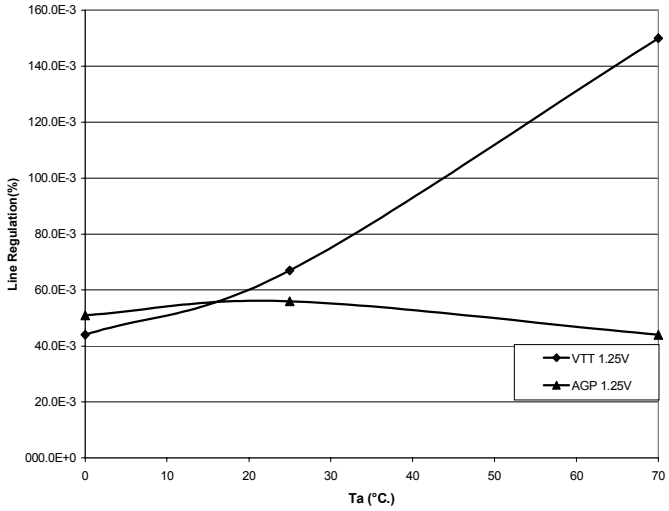
I 5V Stby vs Ta



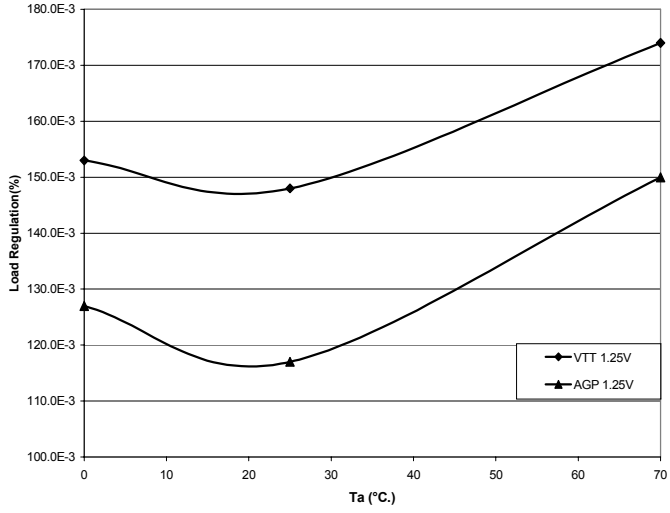
Output Select Threshold vs Ta



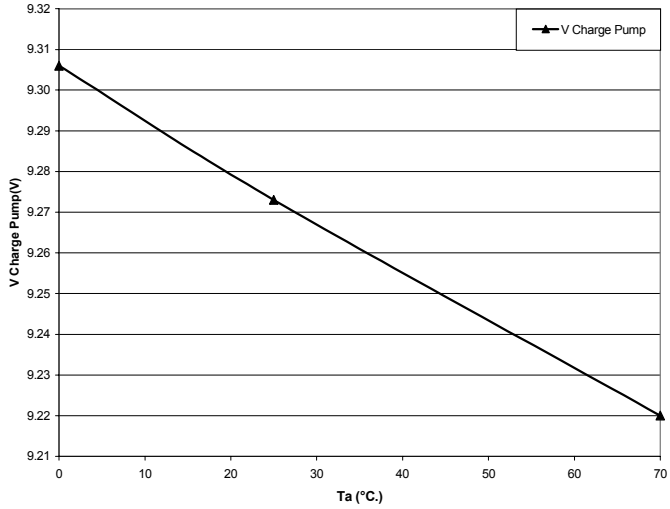
Line Regulation VTTIN = 3.13V to 3.47V Io = 2A vs Ta



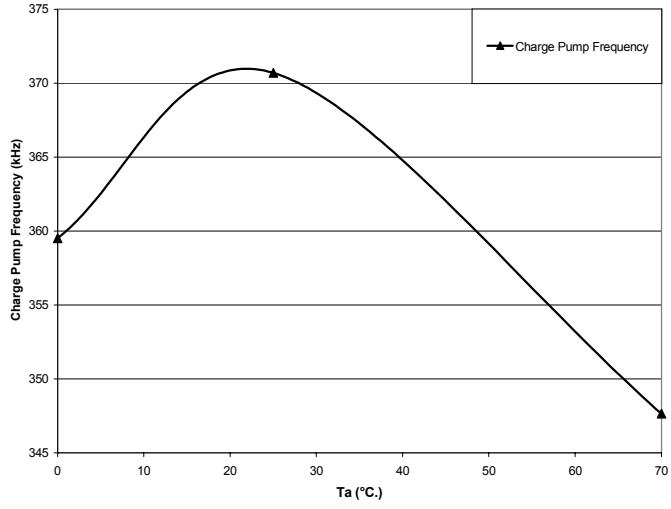
Load Regulation VTTIN = 3.3V Io = 0 to 2A vs Ta



Charge Pump Output Voltage vs Ta

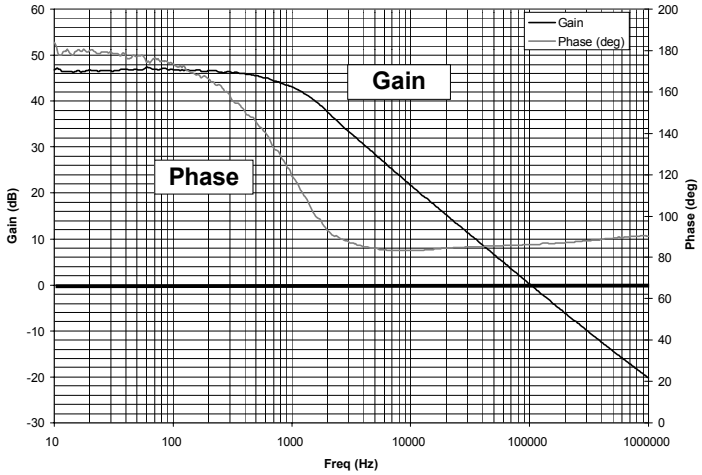


Charge Pump Frequency vs Ta

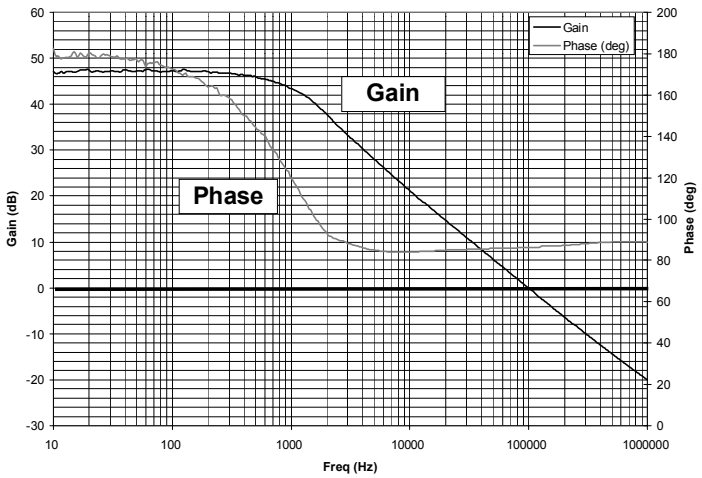


Typical Gain & Phase Margin

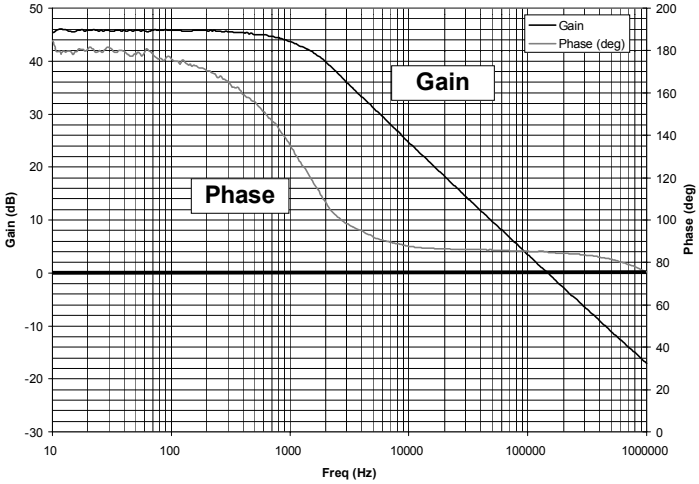
SC1112 Gain / Phase VTT = 1.25V @ 2A



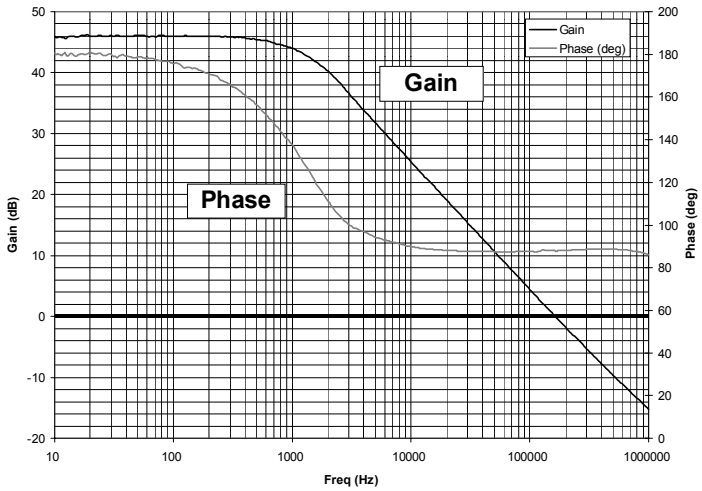
SC1112 Gain / Phase VTT = 1.5V @ 2A



SC1112 Gain / Phase ADJ = 1.2V @ 2A



SC1112 Gain / Phase AGP = 1.5V @ 2A



Theory Of Operation

The SC1112 was designed for the latest high speed mother boards requiring a controlled power up sequencing of the Outputs, and a programmable delay for the Power good signal.

Three Linear controllers have been incorporated into the SC1112. The VTT output can be programmed to either a 1.250V or a 1.500V by applying a LOW or a HIGH control signal to the VTTSEL pin. AGP output can also be programmed via AGPSEL pin to a 1.50V or a 3.30V. The SC1112 also provides an Adjustable output which utilizes a resistive voltage divider.

The +5VSTBY supply will power the internal Reference, Charge Pump, Oscillator, and the Fet controllers. After the +5VSTBY has been established, LDO outputs will track the VTTIN (3.30V) supply as it is applied.

An external capacitor connected to the Delay pin will program the VTT short circuit delay time (SC_{td}), and the PWRGD delay time (PG_{td}).

During power up, an internal short circuit glitch timer will start once the VTT Input Voltage exceeds the $VTTIN_{TH}$ (1.5V). During the glitch timer immunity time, determined by the Delay capacitor (Delay time is approximately equal to (Cdelay*SCTH)/ISC), the short circuit protection is disabled to allow VTT output to rise above the trip threshold (0.7V).

If the VTT output has not risen above the trip threshold after the immunity time has elapsed, the VTT output is latched off and will only be enabled again if either the VTT input voltage or the 5VSTBY is cycled.

PWRGD pin is kept low during the power up, until the VTT output has reached its $PG_{td1.25}$ or $PG_{td1.5}$ level. At that time the PWRGD source current I_{PG} (20uA) is enabled and will start charging the external PWRGD delay capacitor connected to the DELAY pin. Once the capacitor is charged above the PG_{Delay_TH} (1.5V), the PWRGD pin is released from ground. A detailed timing diagram is shown on pages 4 to 5.

Also included is an overcurrent protection circuit that monitors the VTT voltage. If the output voltage drops below 700mV, as would occur during an overcurrent or short condition, the device will pull the drive pin low and latch off the output.

Fixed Output Voltage Options (VTT, AGP)

Please refer to the Application Circuit on Page 1. The VTT and the AGP fixed output voltage can be programed from a Control logic signal. Table below shows the possible voltages:

VTTSEL	AGPSEL	VTT	AGP
0	0	1.25V	1.50V
0	1	1.25V	3.30V
1	0	1.50V	1.50V
1	1	1.50V	3.30V

Once the VTTSEL or the AGPSEL signal is established, an internal resistive divider is used to compare the bandgap reference voltage with the feedback output voltage. The drive pin voltage is then adjusted to maintain the output voltage set by the internal resistor divider. Referring to the block diagram on page 8.

It is possible to adjust the output voltage of the VTT or AGP, by applying an external resistor divider to the sense pin (please refer to Figure 1 on Page 17). Since the sense pin sinks a nominal 100µA, the resistor values should be selected to allow 10mA to flow through the divider. This will ensure that variations in this current do not adversely affect output voltage regulation. Thus a target value for R2 (maximum) can be calculated:

$$R2 \le \frac{V_{OUT\ (FIXED)}}{10mA} \quad \Omega$$

The output voltage can only be adjusted upwards from the fixed output voltage, and can be calculated using the following equation:

$$V_{OUT\ (ADJUSTED)} = V_{OUT\ (FIXED)} \bullet \left(1 + \frac{R1}{R2}\right) + R1 \bullet 100\,\mu A \quad \text{Volts}$$

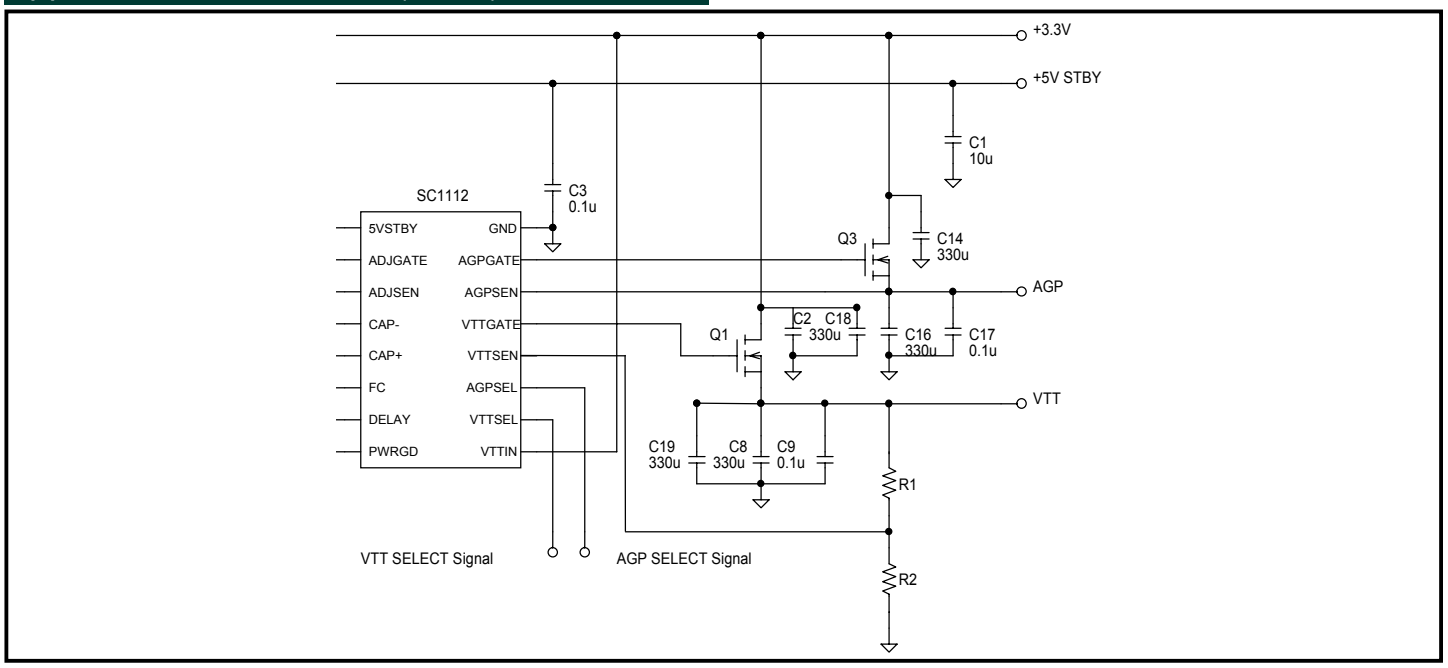


Figure 1: Adjusting The Output Voltage of VTT or AGP

Adjustable Output Voltage Option

The adjustable output voltage option does not have an internal resistor divider. The adjust pin connects directly to the inverting input of the error amplifier, and the output voltage is set using external resistors (please refer to Figure 2). In this case, the adjust pin sources a nominal 0.5µA, so the resistor values should be selected to allow 50µA to flow through the divider. Again, a target value for RB (maximum) can be calculated:

$$RB \leq \frac{1.200\,V}{50\mu A} \quad \Omega$$

The output voltage can be calculated as follows:

$$V_{OUT} = 1.200 \bullet \left(1 + \frac{RA}{RB}\right) - 0.5\mu A \bullet RA$$

The maximum output voltage that can be obtained from the adjustable option is determined by the input supply voltage and the $R_{DS(ON)}$ and gate threshold voltage of the external MOSFET. Assuming that the MOSFET gate threshold voltage is sufficiently low for the output voltage chosen and a worst-case drive voltage of 9V, $V_{OUT(MAX)}$ is given by:

$$V_{OUT(MAX)} = VTTIN_{(MIN)} - I_{OUT(MAX)} \bullet R_{DS(ON)(MAX)}$$

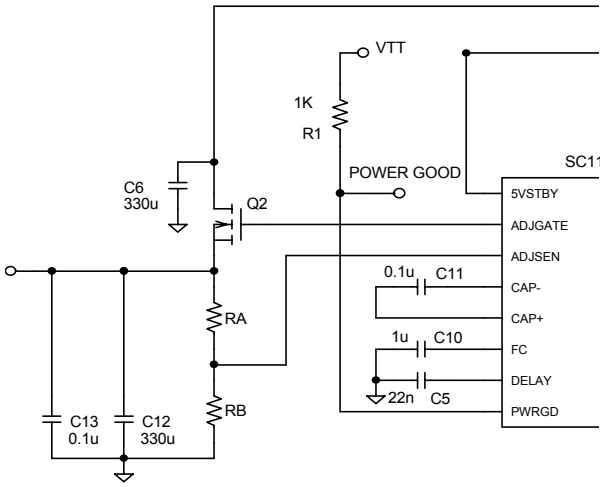


Figure 2

Applications Infomation (Cont.)

Short Circuit Protection

The VTT short circuit protection feature of the SC1112 is implemented by using the $R_{DS(ON)}$ of the MOSFET. As the output current increases, the regulation loop maintains the output voltage by turning the FET on more and more. Eventually, as the $R_{DS(ON)}$ limit is reached, the MOSFET will be unable to turn on any further, and the output voltage will start to fall. When the VTT output voltage falls to approximately 700mV, the LDO controller is latched off, setting output voltage to 0V. Power must be cycled to reset the latch.

To prevent false latching due to capacitor inrush currents or low supply rails, the current limit latch is initially disabled. It is enabled once the short circuit delay time has elapsed. Timing diagram on pages 4 to 5 will show a detailed operation of the Short Circuit protection circuitry.

To be most effective, the MOSFET $R_{DS(ON)}$ should not be selected artificially low. The MOSFET should be chosen so that at maximum required current, it is almost fully turned on. If, for example, a supply of 1.5V at 4A is required from a 3.3V ± 5% rail, the maximum allowable $R_{DS(ON)}$ would be:

$$R_{DS(ON)(MAX)} = \frac{(0.95 \bullet 3.3 - 1.5 \bullet 1.025)}{4} \approx 400\,m\Omega$$

To allow for temperature effects 200mΩ would be a suitable room temperature maximum, allowing a peak short circuit current of approximately 15A for a short time before shutdown.

Capacitor Selection

Output Capacitors: Low ESR aluminum electrolytic or tantalum capacitors are recommended for bulk capacitance, with ceramic bypass capacitors for decoupling high frequency transients.

Input Capacitors: Placement of low ESR aluminum electrolytic or tantalum capacitors at the input to the MOSFET (VTTIN) will help to hold up the power supply during fast load changes, thus improving overall transient response. The +5VSTBY supply should be bypassed with a 10µF ceramic capacitor.

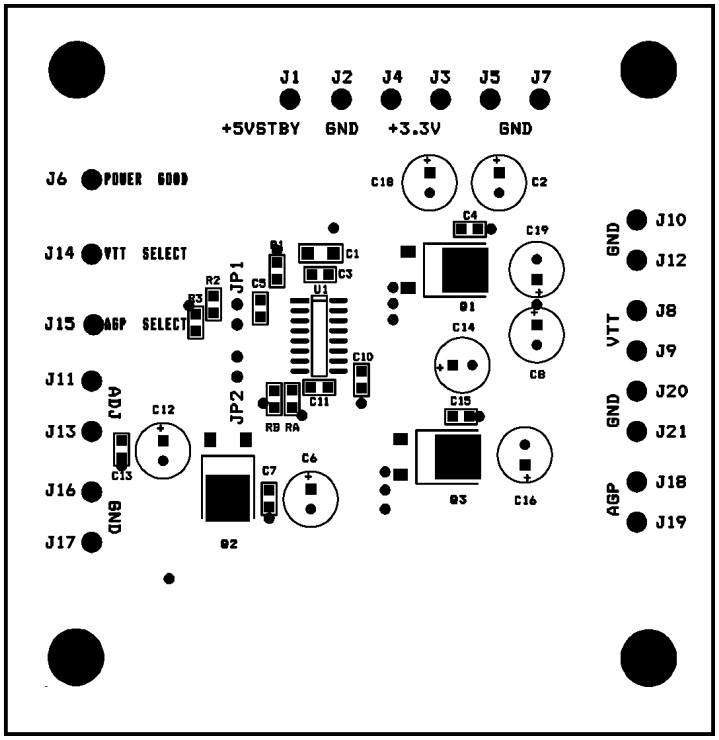
Layout Guidelines

One of the advantages of using the SC1112 to drive an external MOSFET is that the bandgap reference and control circuitry do not need to be located right next to the power device, thus a very accurate output voltage can be obtained since heating effects will be minimal.

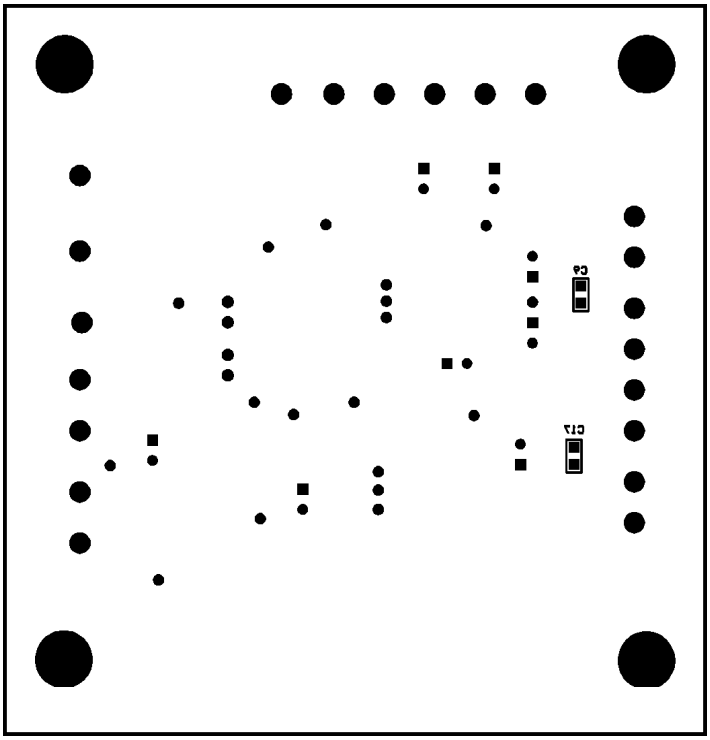
The 0.1µF bypass capacitor should be located close to the +5VSTBY supply pin, and connected directly to the ground plane. The ground pin of the device should also be connected directly to the ground plane. The sense or adjust pin does not need to be close to the output voltage plane, but should be routed to avoid noisy traces if at all possible.

Power dissipation within the device is practically negligible, requiring no special consideration during layout.

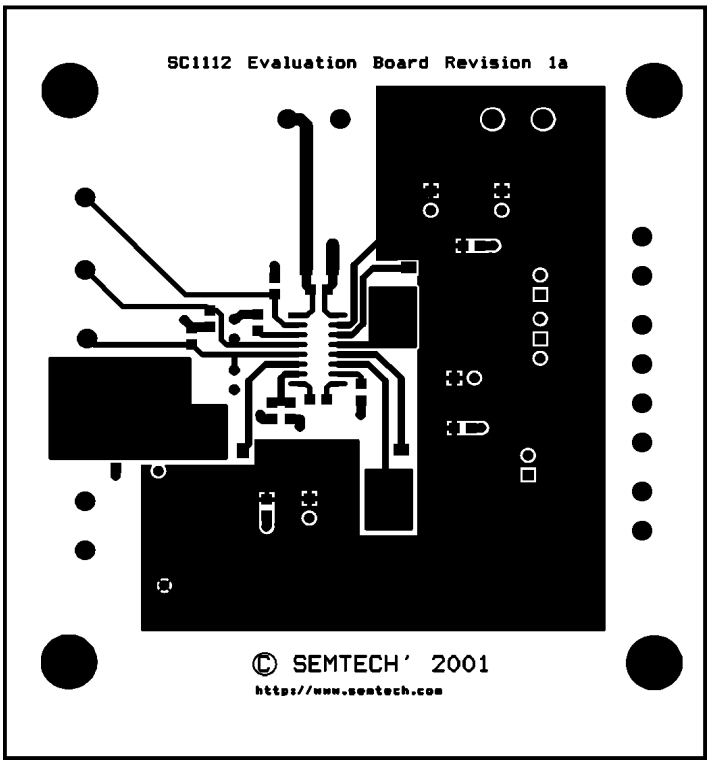
Evaluation Board Gerbers



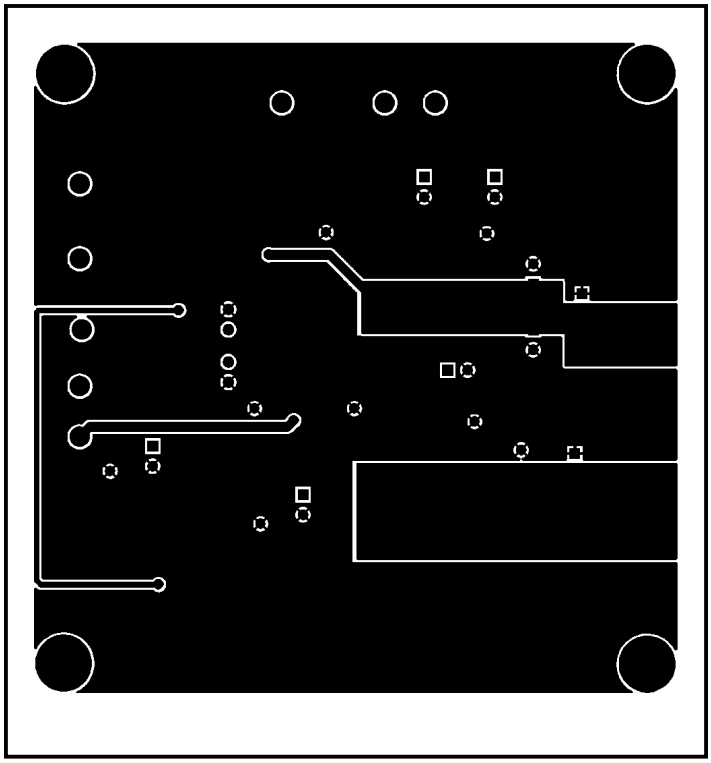
Board Layout Assembly Top



Board Layout Assembly Bottom

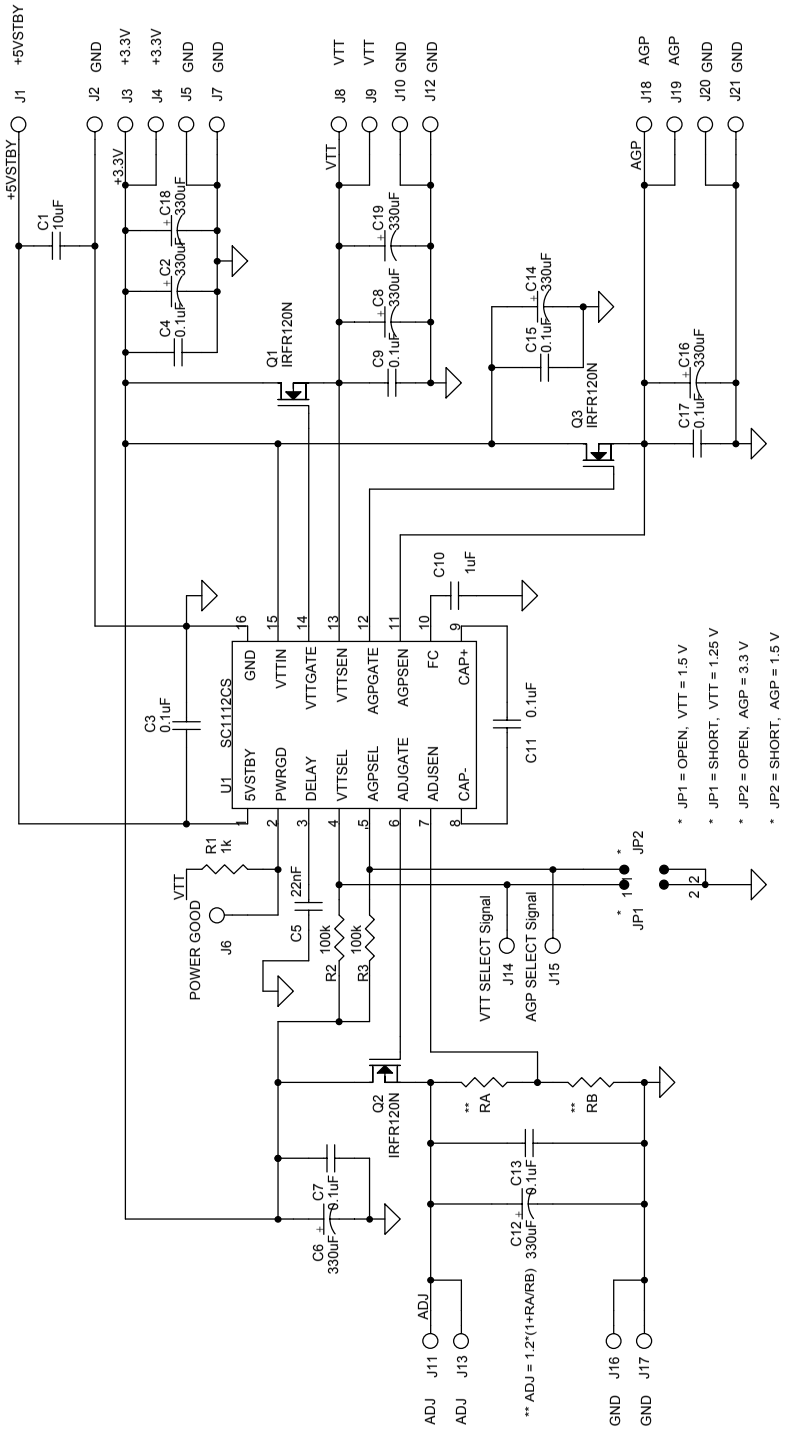


Board Layout Top



Board Layout Bottom

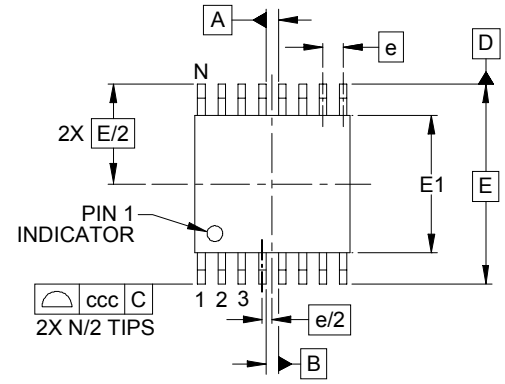
Evaluation Board Schematic



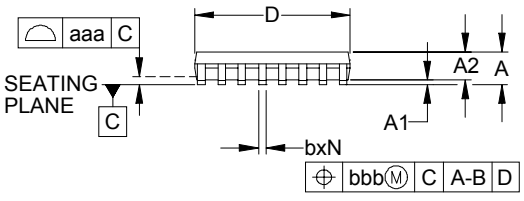
Evaluation Board Bill of Materials

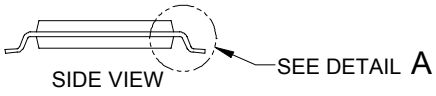
Item	Qty.	Reference	Part	Foot Print
1	1	C1	10uF	1206
2	8	C2,C6,C8,C12,C14,C16,C18,C19	330uF	CPCYL/D.2.75/LS.100/.031
3	8	C3,C4,C7,C9,C11,C13,C15,C17	0.1uF	0805
4	1	C5	22nF	0805
5	1	C10	1uF	0805
6	2	JP1,JP2	TP2	VIA/2P
7	1	J1	+5VSTBY	ED5052
8	9	J2,J5,J7,J10,J12,J16,J17,J20,J21	GND	ED5052
9	2	J3,J4	+3.3V	ED5052
10	1	J6	Power Good	ED5052
11	2	J8,J9	VTT	ED5052
12	2	J11,J12	ADJ	ED5052
13	1	J14	VTT SELECT Signal	ED5052
14	1	J15	AGP SELECT Signal	ED5052
15	2	J18,J19	AGP	ED5052
16	3	Q1,Q2,Q3	IRFR120N	DPAKFET
17	3	R1,RA,RB	1k	0805
18	2	R2,R3	100k	0805
19	1	U1	SC1112STRT	SO-16

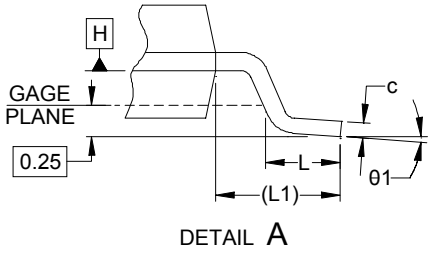
Outline Drawing - TSSOP-16



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.192	.196	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		



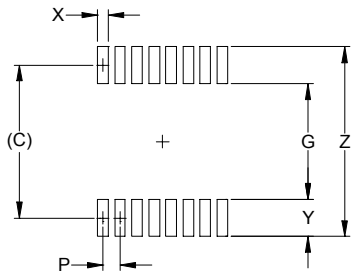




NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AB.

Land Pattern - TSSOP-16

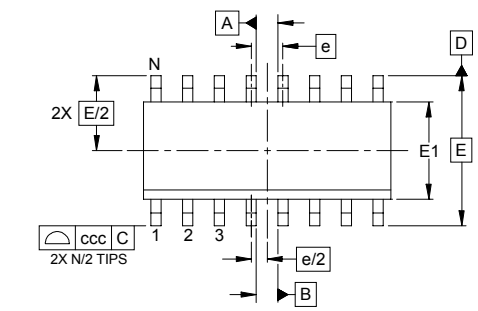


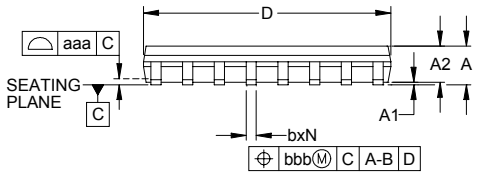
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

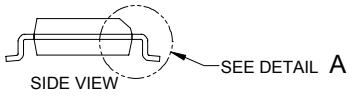
NOTES:

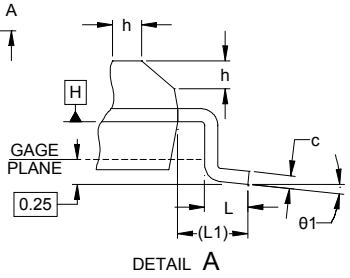
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Outline Drawing - SO-16







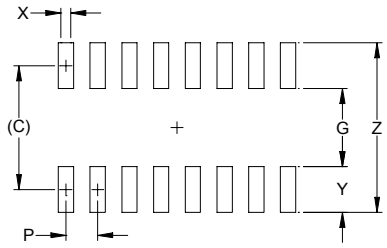


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.386	.390	.394	9.80	9.90	10.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AC.

Minimum Land Pattern - SO-16



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 304A.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804