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### POWER MANAGEMENT

#### Description

The SC1116 is a low cost controller for low power linear DDR power supplies.

The SC1116 comes in a space saving SOT-23 6 pin package.

The SC1116 provides a dual gate drive for the top serial and bottom parallel MOSFETs with internal shoot through protection.

The wide range of input voltages (3V to 15V) allows the chip to work in many various applications.

The variable output voltage is programmable from the outside with an input divider or an external reference.

Wide range of  $V_{DDQ}$ , down to 0.5V

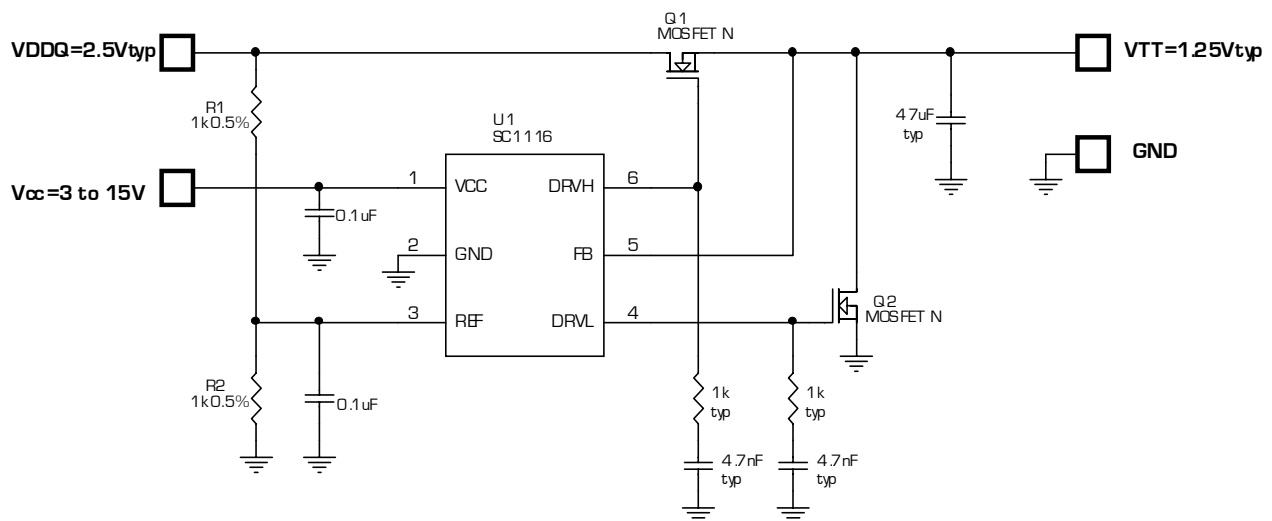
#### Features

- ◆ User can select FETs to optimize system current rating/dropout/cost
- ◆ Low  $V_{DDQ}$ , 0.5V to 2.5V
- ◆ -40°C to +85°C operating temperature
- ◆ External compensation capable for low ESR loads
- ◆ Minimum external components
- ◆ 0.6 mA Quiescent current
- ◆ Guaranteed no shoot through
- ◆ SOT-23 6L small package. Fully WEEE and RoHS compliant

#### Applications

- ◆ DDR supplies
- ◆ SCSI
- ◆ Line termination
- ◆ Source / Sink LDOs

#### Typical Application Circuit



#### Notes:

- (1) Values used for optional compensation are 1K and 4.7nF typical.
- (2) When using 3V as Vcc, use of low threshold FETs is a must.

**POWER MANAGEMENT**
**Absolute Maximum Rating**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	$V_{CC}$	-0.3 to +16.5	V
Operating Ambient Temperature Range	$T_A$	-40 to +85	°C
Operating Junction Temperature Range	$T_J$	-40 to +125	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Thermal Impedance Junction to Ambient	$\theta_{JA}$	95.7	°C/W
Thermal Impedance Junction to Case	$\theta_{JC}$	61.7	°C/W
Power Dissipation at $T_A = 25^\circ\text{C}$	$P_D$	250	mW
Lead Temperature (Soldering) 10 seconds	$T_{LEAD}$	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

**Electrical Characteristics**

Unless otherwise specified,  $V_{CC} = 5V$ ,  $0.5V \leq V_{DDQ} \leq 2.5V$ ,  $R1 = R2 = 1k\Omega \pm 0.1\%$ .

Specifications with standard typeface are for  $T_J = 25^\circ\text{C}$ , and limits in **boldface** type apply over the full operating temperature range ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ).

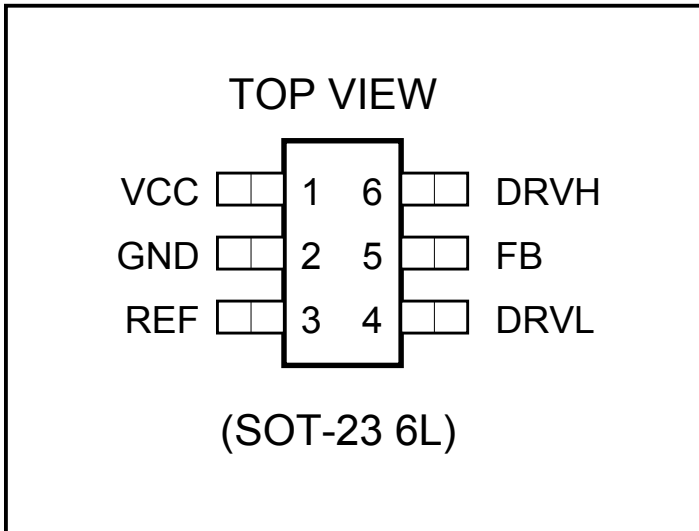
Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage		3		15	V
Load Regulation <sup>(1)</sup>	IL: 0 + 3A IL: 0 - 3A		-1 +1		%
Quiescent Current/Standby Current	$V_{CC} = 15V$ , no load = 0A		600	<b>800</b>	$\mu\text{A}$
FB & REF Input Current	$V_{CC} = 15V$			100	nA
<b>Gate Drive</b>					
Output Low	$I_{SINK} = 2.5\text{mA}$		0.15	<b>0.25</b>	V
Output High	$I_{SOURCE} = 2.5\text{mA}$	<b>Vcc -0.25</b>	Vcc -0.15		V

Note:

(1) For Load Regulation testing use a low duty cycle current pulse, when measuring VTT.

**POWER MANAGEMENT**

**Pin Configuration**



**Ordering Information**

Part Number	Top Mark	Package
SC1116ISKTR <sup>(1)</sup>	AH00	SOT-23 6L
SC1116ISKTRT <sup>(1)(2)</sup>		

**Notes:**

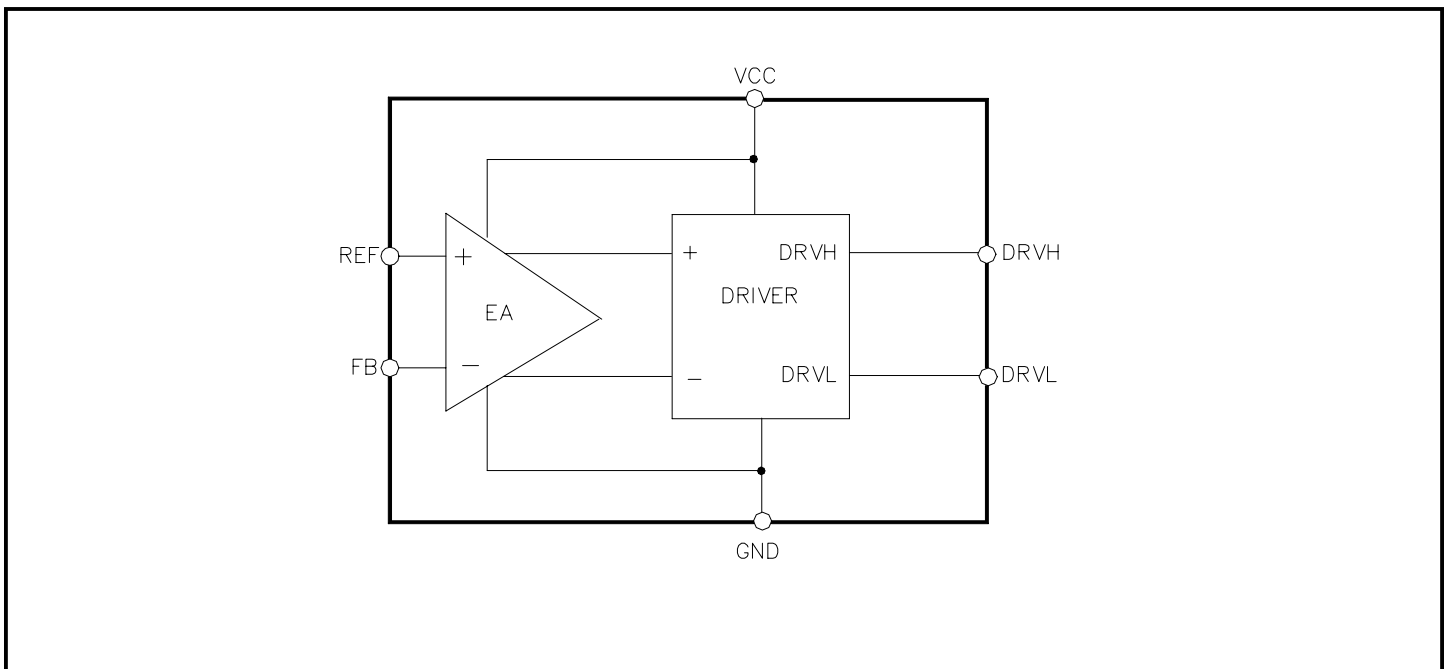
(1) Only available in tape and reel packaging. A reel contains 3000 devices.

(2) Lead free option. Fully WEEE and RoHS compliant.

**Pin Descriptions**

Pin #	Pin Name	Pin Function
1	VCC	Supply pin, connect a 3V to 15V supply and decouple to ground with a 0.1µF ceramic capacitor.
2	GND	Power and signal ground.
3	REF	Reference input. Output voltage will be regulated to this voltage.
4	DRVL	Low side FET drive output.
5	FB	Feedback pin.
6	DRVH	High side FET drive output.

**Block Diagram**



**POWER MANAGEMENT**

**Application Information**

**Overview**

The SC1116 linear controller is designed to meet the JEDEC specifications for termination of DDR-SDRAM. Double Data Rate (DDR) memory is clocked at the same speed as older SDRAM (synchronous dynamic random access memory), yet handles twice the amount of data by using the rising and falling edge of the clock signal for data transfers. Another difference is that DDR memory requires 2.5V instead of 3.3V used by standard SDRAM. The other feature that separates DDR memory from a conventional type is employment of the  $V_{TT}$  - termination voltage. Main requirements for the  $V_{TT}$  are that it must track variations of  $V_{DDQ}$  and be able to supply (source) current, and absorb (sink) current.

The SC1116 controller offers a low cost solution for DDR termination voltage regulation by using external pass elements (MOSFETs). Having the flexibility of choosing the MOSFETs allows for optimization on the basis of cost/size/performance of the specific application.

**Test Circuit & Waveforms**

The test circuit is shown below in Figure 1. Note that  $V_{REF}$  voltage is supplied externally to eliminate inaccuracy caused by resistor divider.

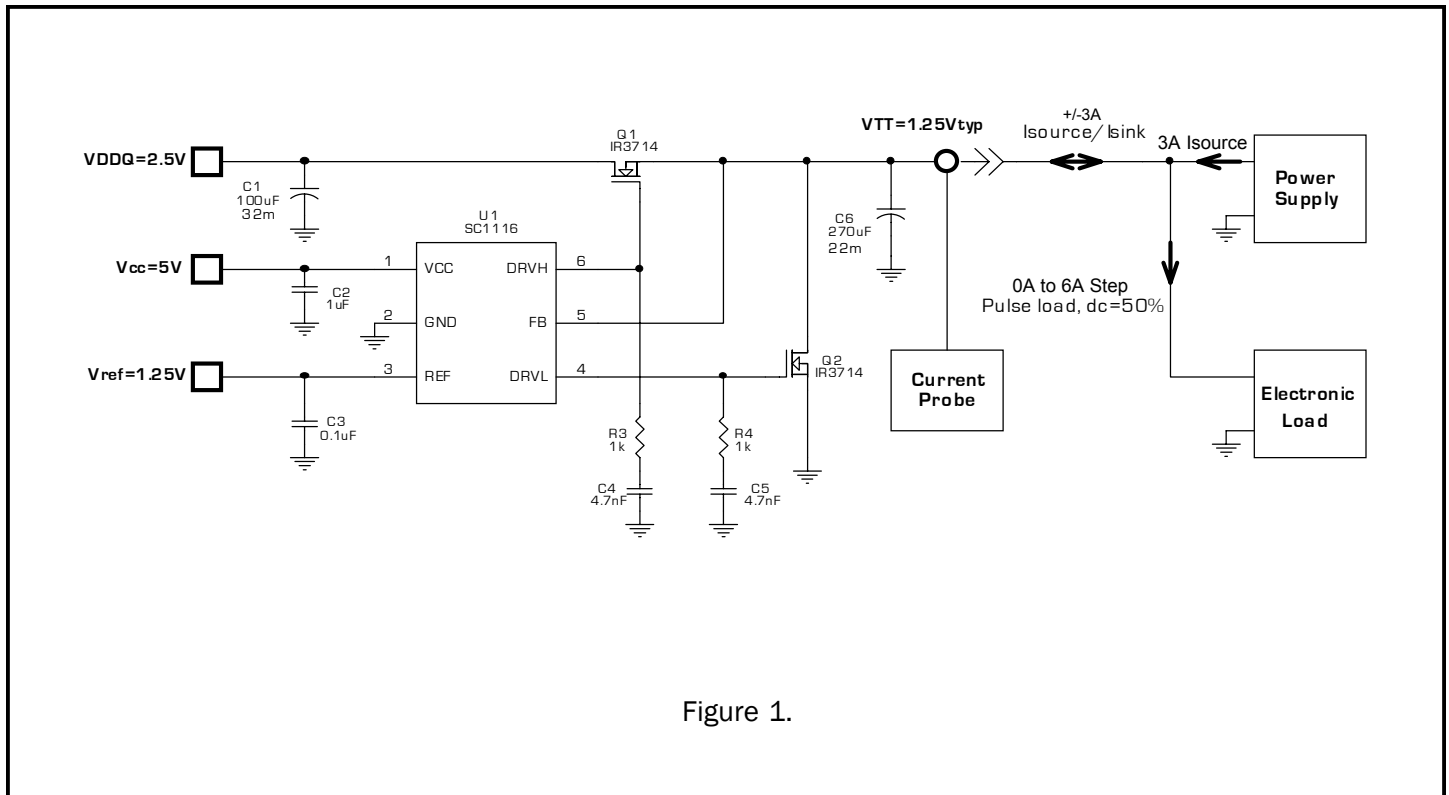
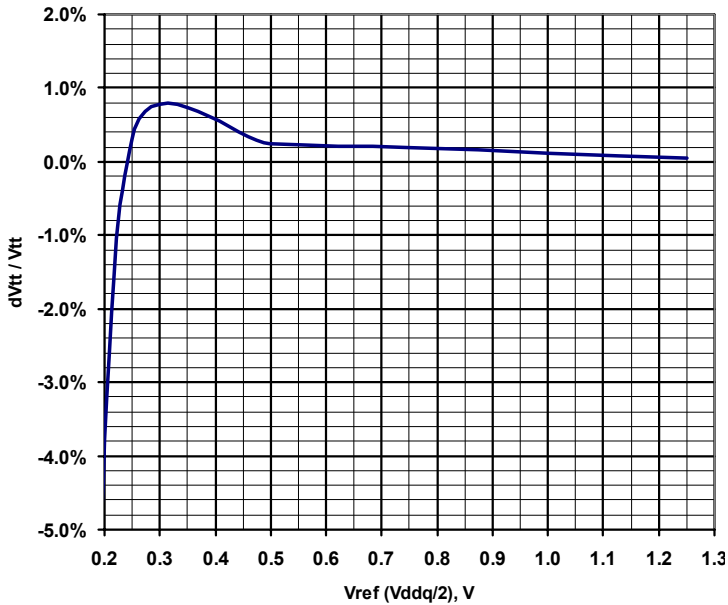
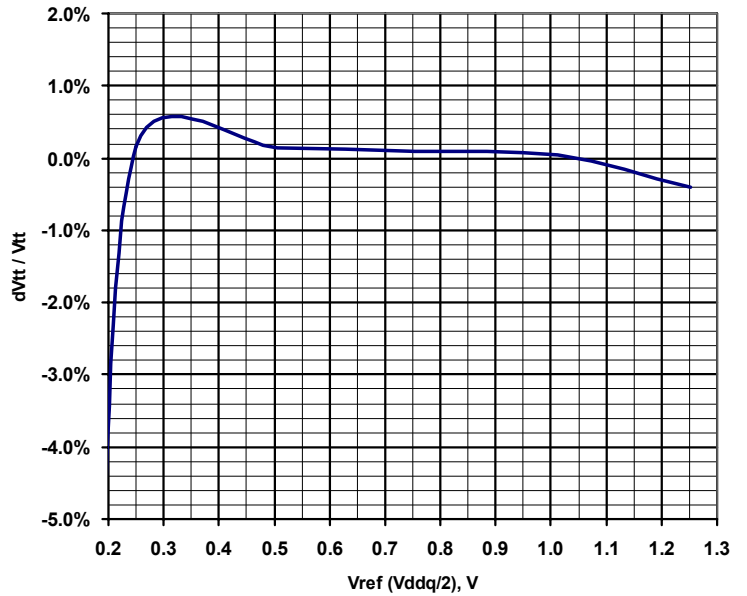
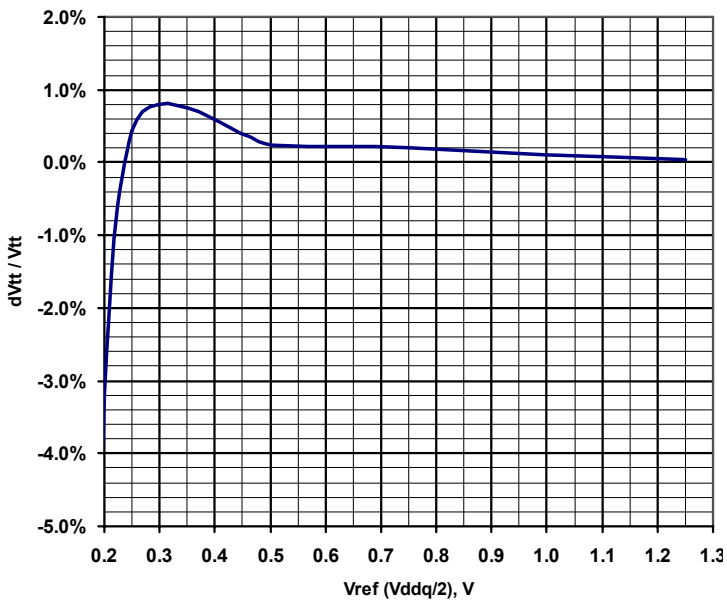
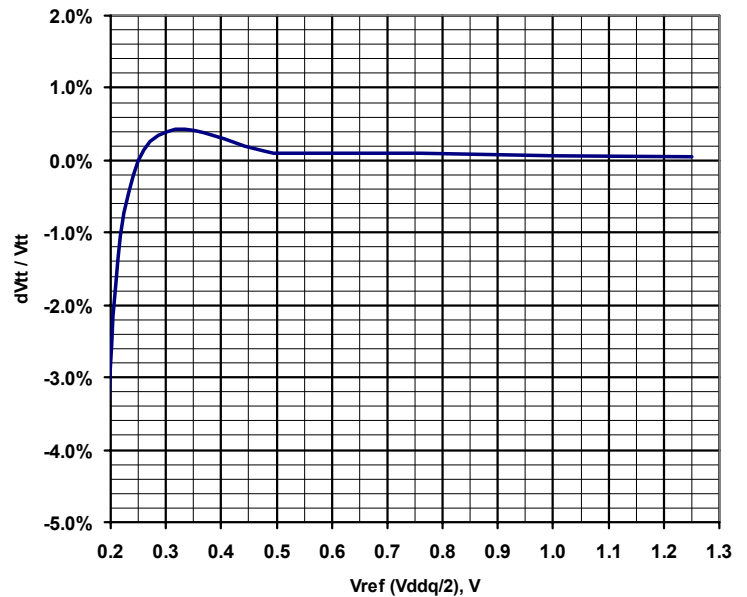
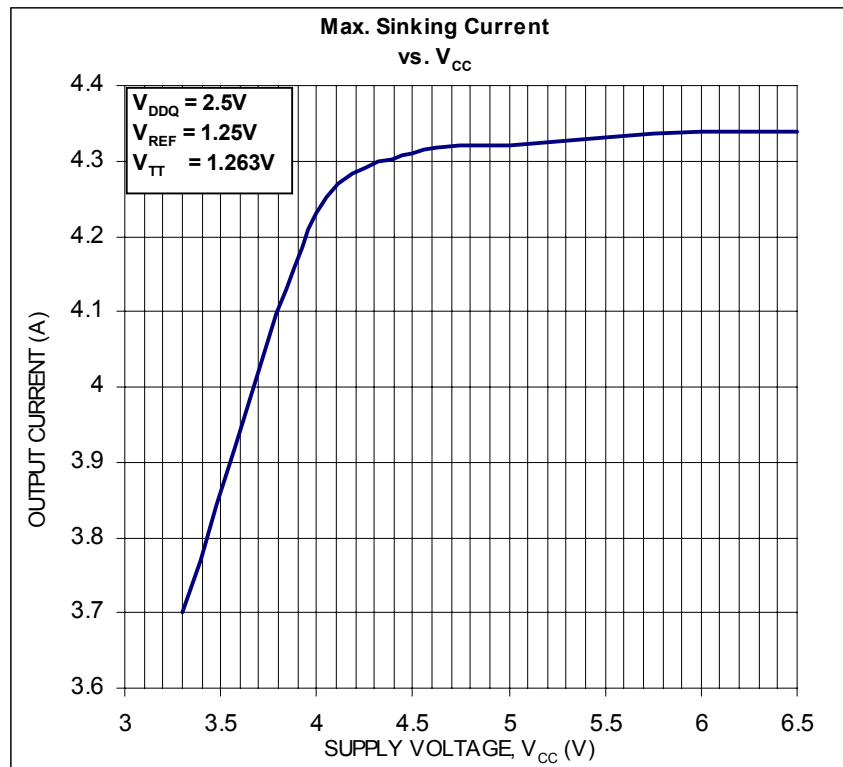
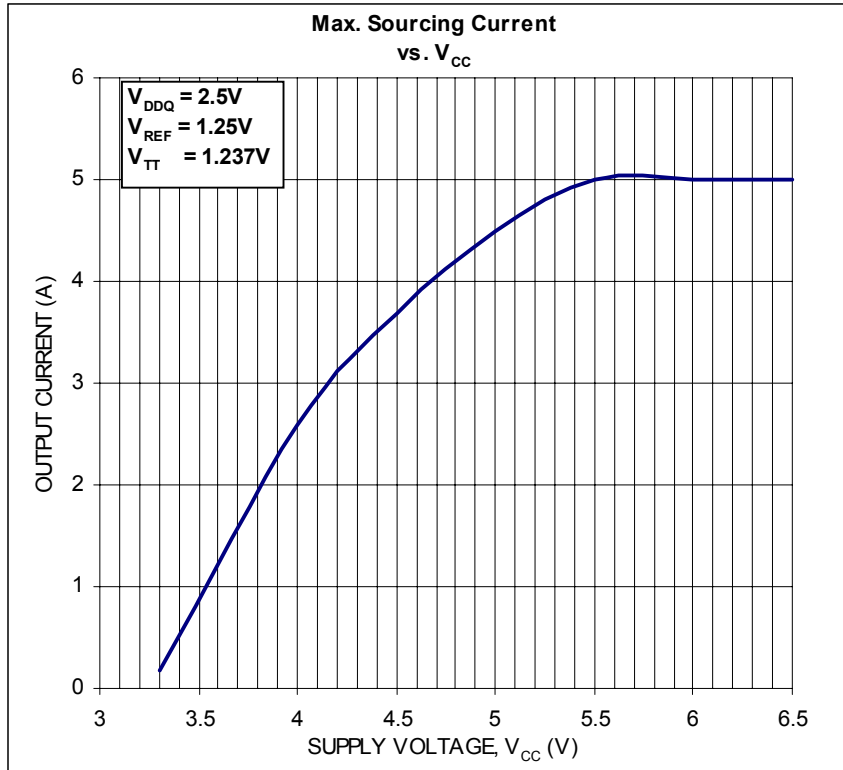


Figure 1.

**POWER MANAGEMENT**
**Typical Characteristics**
**Regulation V<sub>tt</sub> vs. V<sub>ref</sub> @ I<sub>s</sub>/s=1A; V<sub>cc</sub>=5V**

**Regulation V<sub>tt</sub> vs. V<sub>ref</sub> @ I<sub>s</sub>/s=5A; V<sub>cc</sub>=5V**

**Regulation V<sub>tt</sub> vs. V<sub>ref</sub> @ I<sub>s</sub>/s=1A; V<sub>cc</sub>=12V**

**Regulation V<sub>tt</sub> vs. V<sub>ref</sub> @ I<sub>s</sub>/s=5A; V<sub>cc</sub>=12V**


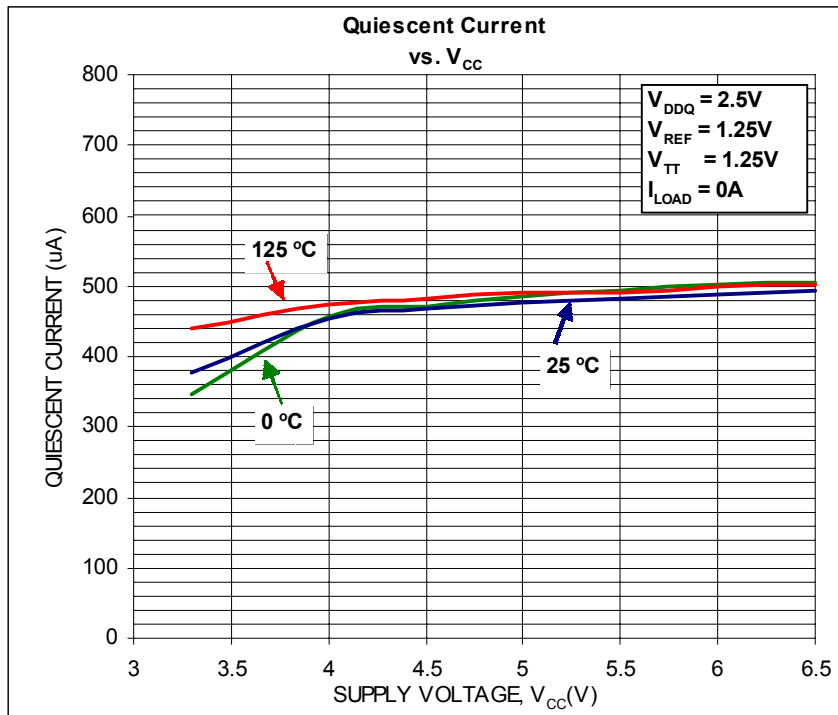
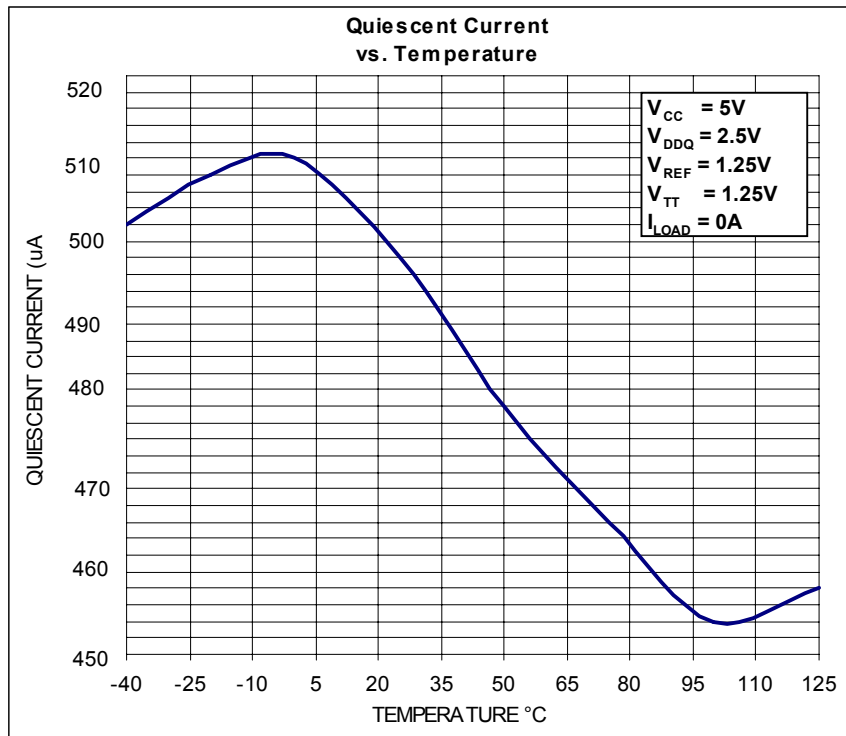
POWER MANAGEMENT

Typical Characteristics (Cont.)



POWER MANAGEMENT

Typical Characteristics (Cont.)

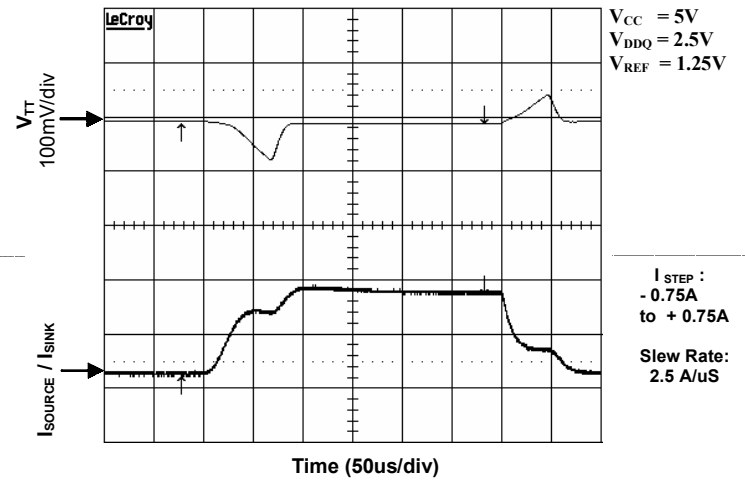
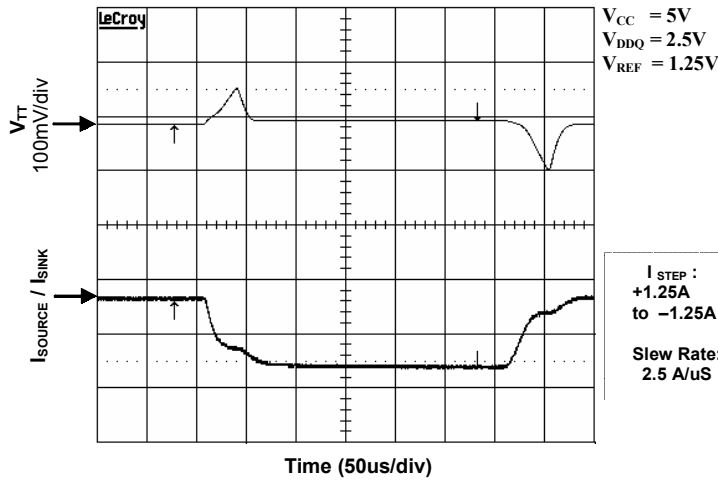
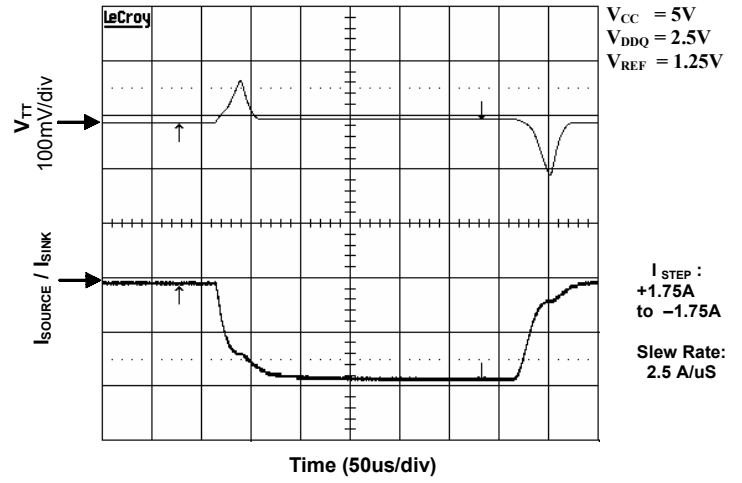
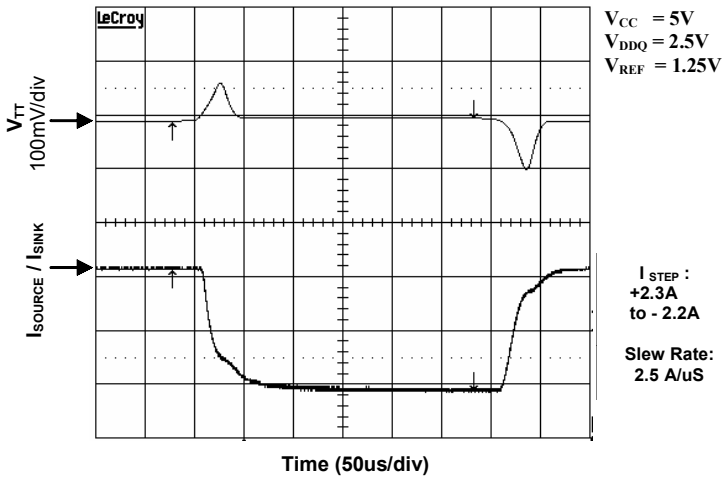




POWER MANAGEMENT

Test Waveforms

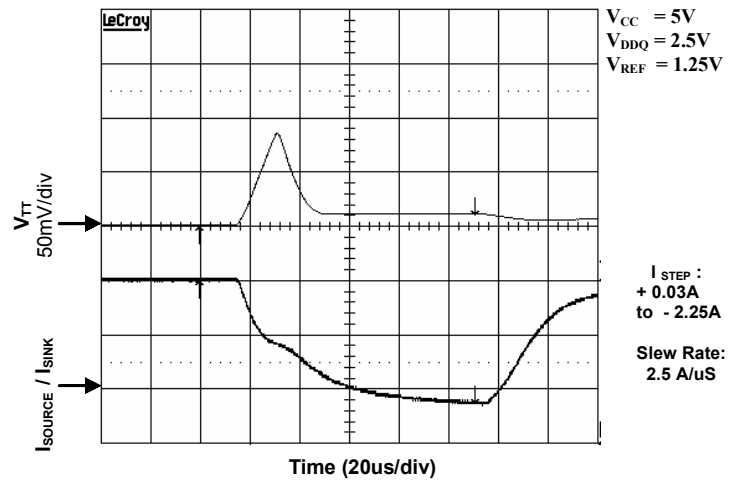
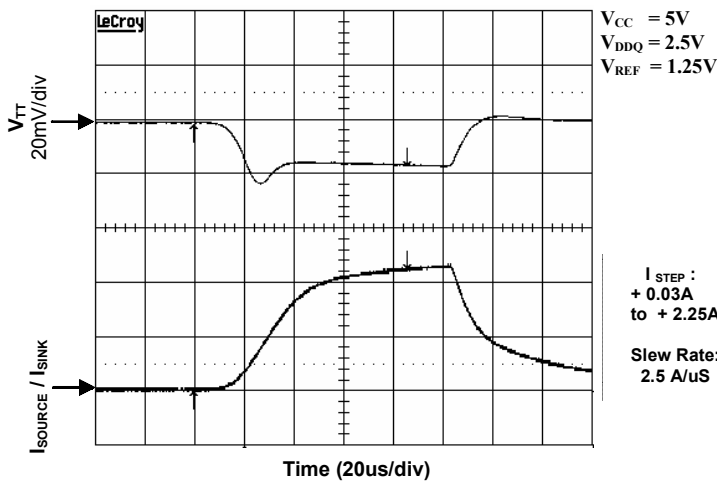
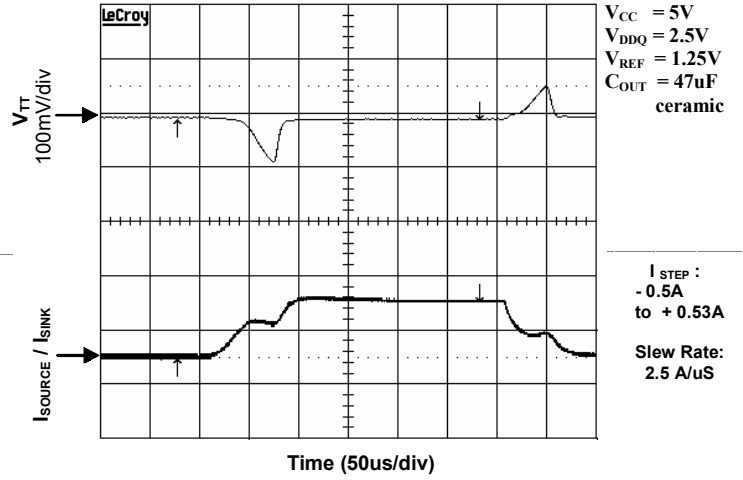
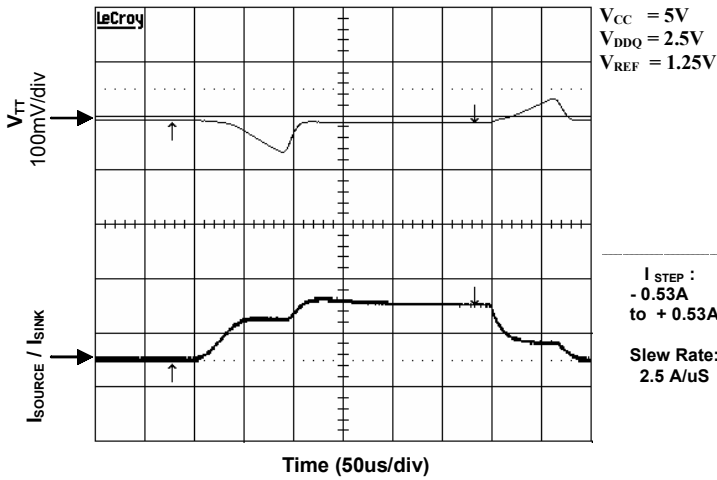
$V_{TT}$  Transient Response



**POWER MANAGEMENT**

**Test Waveforms (Cont.)**

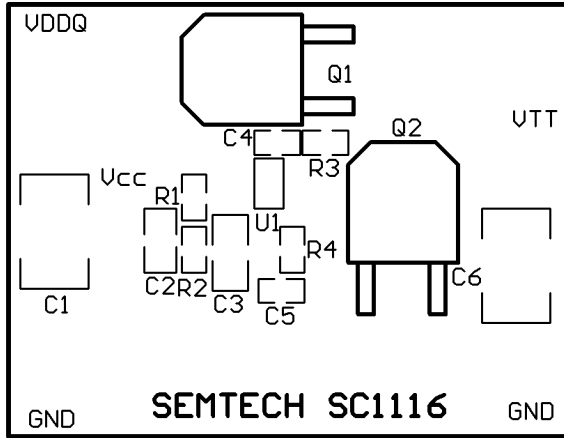
**V<sub>TT</sub> Transient Response**



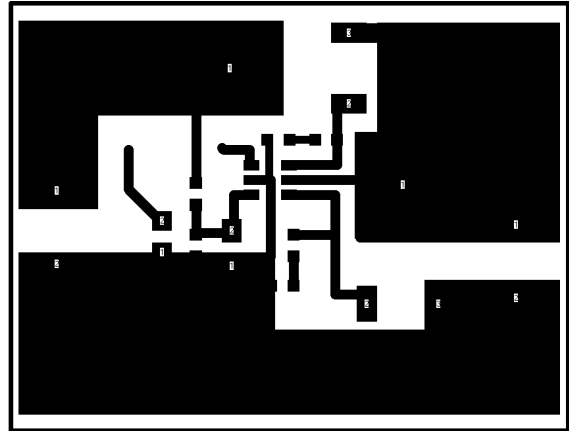
**POWER MANAGEMENT**

**Evaluation Board**

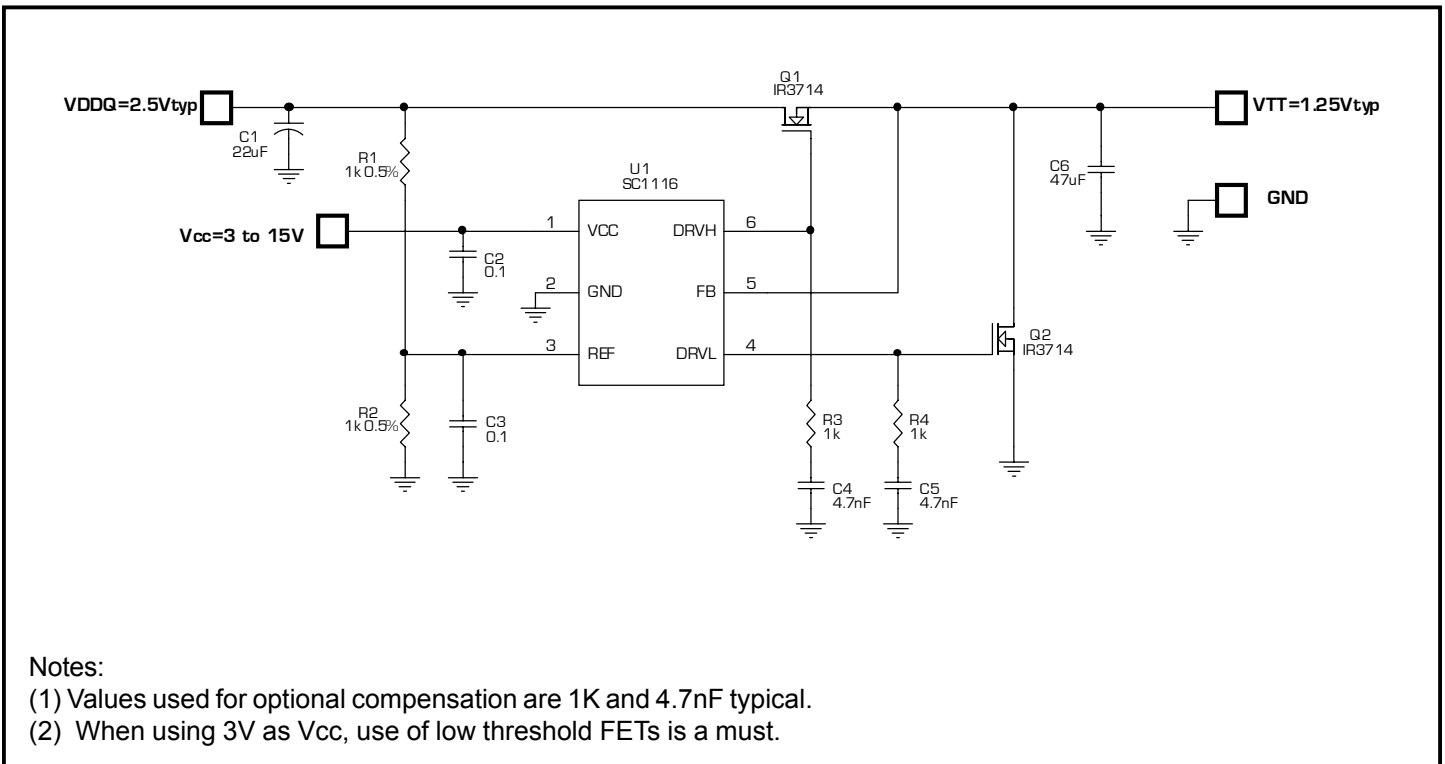
**Top View**



**Top Layer**

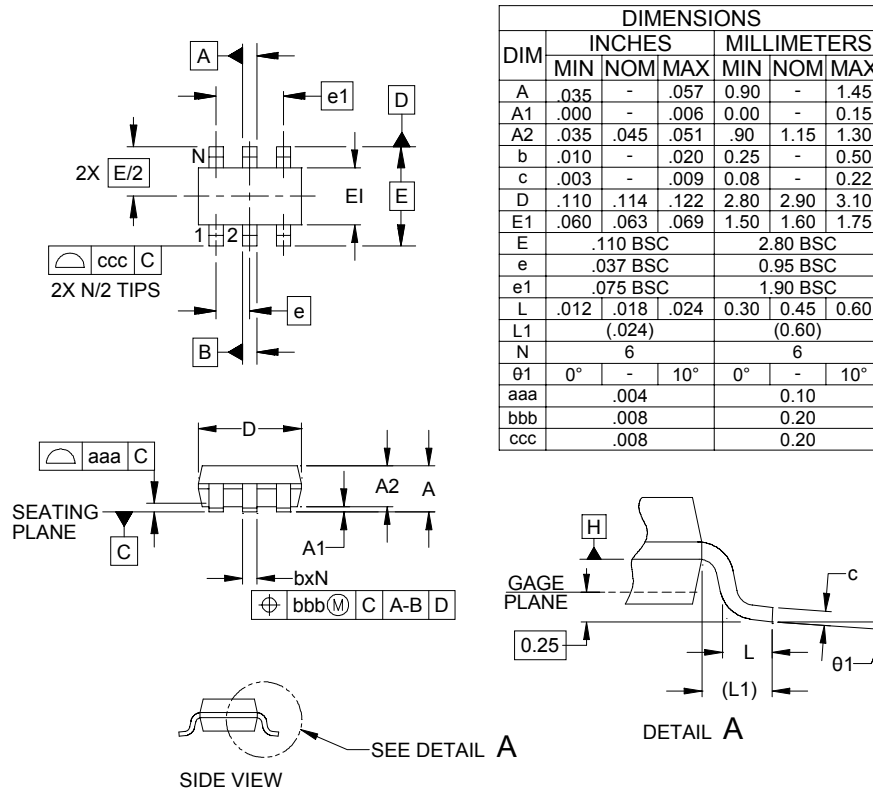


**Evaluation Board Schematic**



**POWER MANAGEMENT**

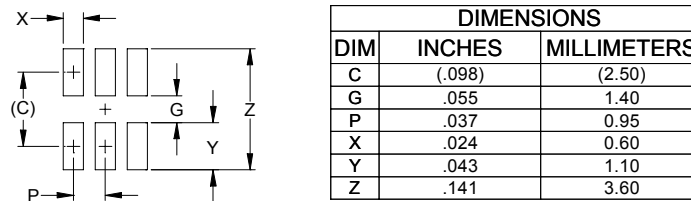
**Outline Drawing - SOT-23-6**



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

**Minimum Land Pattern - SOT-23-6**



NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

**Contact Information**

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